**MB86831 PROCESSOR**

Features 32-bit RISC processing for embedded applications

The MB86831 is a member of the SPARClite Series of RISC processors which offers high performance and high integration for a wide range of embedded applications. The processor is based on the SPARC architecture and is upward code compatible with all other SPARClite implementations. At 66 MHz and 80 MHz, the processor executes with 66 MIPS and 80 MIPS peak respectively.
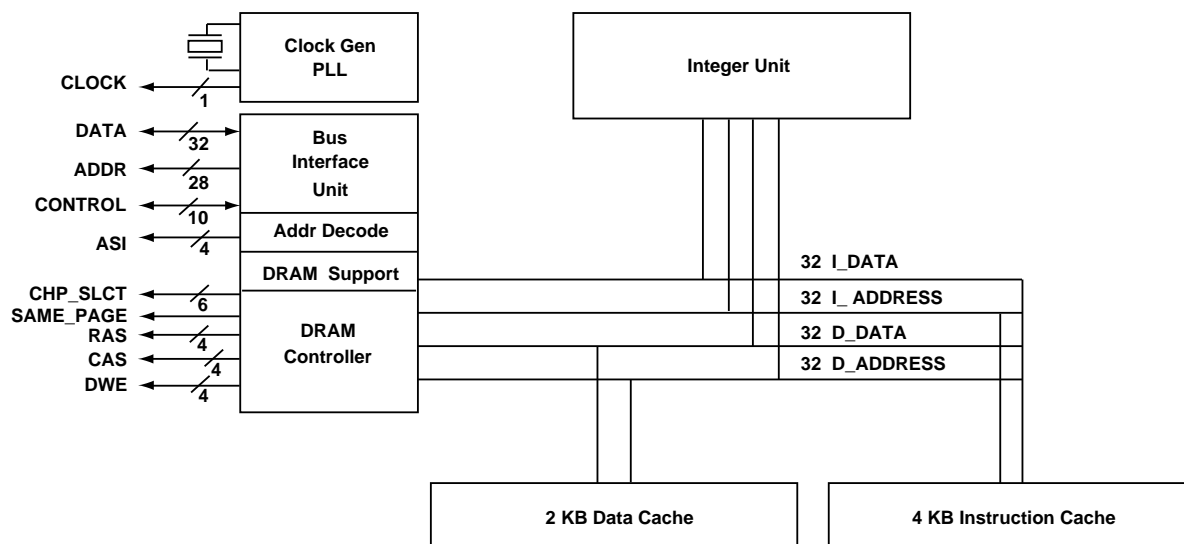
MB86831 Block Diagram

Special features and benefits

MB86930 SUPERSET	*High performance, higher integration.*
66 AND 80 MHZ OPERATION	*Core can run at x1, x2, x3 and x4 frequency of the bus interface unit.*
4 KB INSTRUCTION, 2 KB DATA CACHES	*Fast local processing.*
BURST-MODE CACHE FILLS	*Faster access to memory.*
CONFIGURABLE DATA BUS	*Supports 8-, 16- or 32-bit memories read/write.*
INTERRUPT CONTROLLER	*Fast interrupt response time, with programmable priority.*
DRAM CONTROLLER	*With fast page-mode DRAM and EDO DRAM support.*
FOUR DEEP BUFFERED WRITES AND ONE DEEP INSTRUCTION PRE-FETCHING	*Prevents pipeline stalls.*
GLUELESS INTERFACE TO ROM, EEPROM	*Minimizes system design cost.*
SLEEP MODE	*Supports power down mode, CPU can resume operation.*
0.35µ CMOS	*2 level metal technology.*
3.3V INTERNAL/5V I/O OPERATION	*Low-cost packaging.*

Family features and benefits

FAST INTEGER UNIT	*Performance approaches 1 CPI.*
32-BIT HARDWARE MULTIPLIER	*Improved imaging and DSP-like manipulations.*
136 REGISTERS, 8 WINDOWS	*Very fast interrupt response.*
CACHE LOCKING	*Deterministic, flexible handling of critical code.*
SEPARATE DATA AND ADDRESS BUSES	*Higher performance, no demux logic.*
ADVANCED BUS CONTROLLER	*Simple interface to memory.*
PROGRAMMABLE CHIP SELECTS	*Reduced system chip count.*
SPARC V8/V8E COMPATIBLE	*Object code compatible with all SPARClite 930 Series devices.*