CY7C1339

128K x 32 Synchronous-Pipelined Cache RAM

Features

- **Supports 100-MHz bus for Pentium® and PowerPC™ operations with zero wait states**
- **Fully registered inputs and outputs for pipelined operation**
- **128K by 32 common I/O architecture**
- **3.3V core power supply**
- **2.5V / 3.3V I/O operation**
- **Fast clock-to-output times**
  - **— 3.5 ns (for 166-MHz device)**
  - **— 4.0 ns (for 133-MHz device)**
  - **— 5.5 ns (for 100-MHz device)**
- **User-selectable burst counter supporting Intel® Pentium interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **JEDEC-standard 100 TQFP pinout**
- **"ZZ" Sleep Mode option and Stop Clock option**

Functional Description

The CY7C1339 is a 3.3V, 128K by 32 synchronous-pipelined cache SRAM designed to support zero wait state secondary cache with minimal glue logic.

The CY7C1339 I/O pins can operate at either the 2.5V or the 3.3V level; the I/O pins are 3.3V tolerant when V_{DDQ}=2.5V.

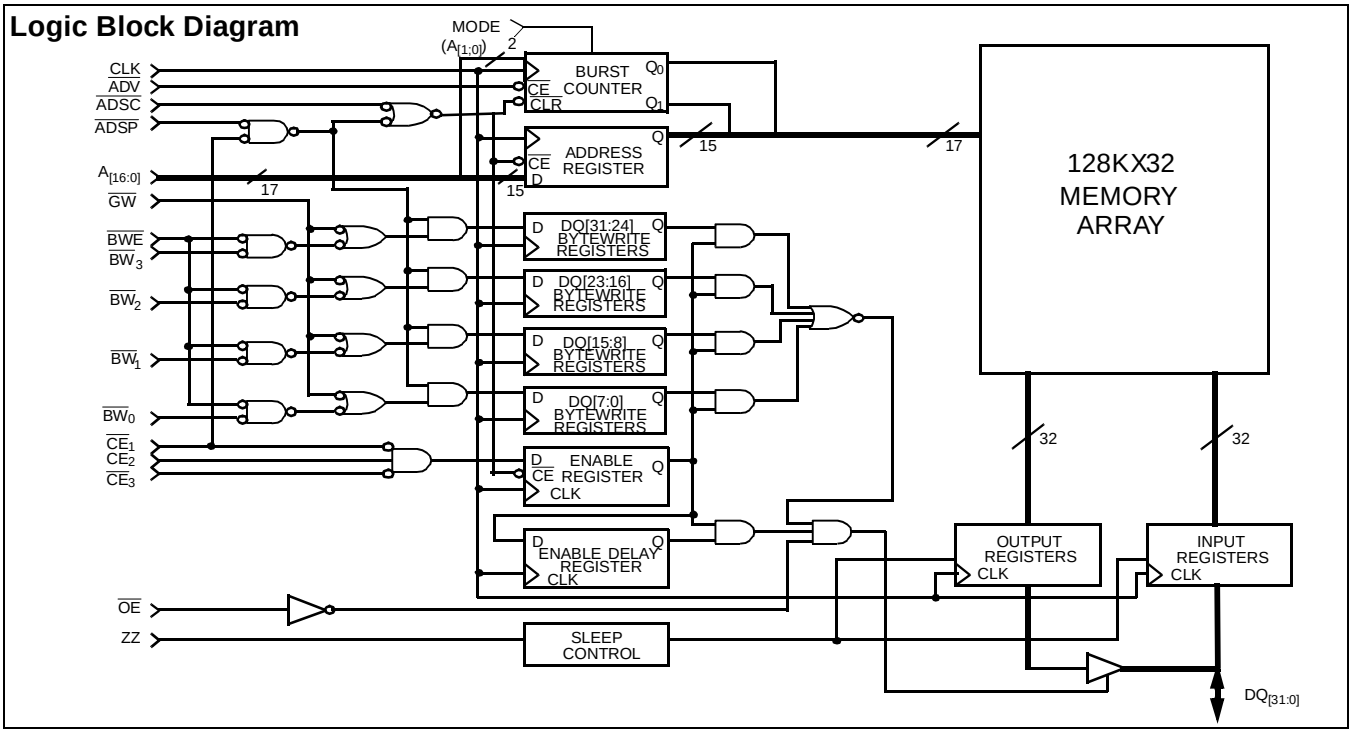
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 3.5 ns (166-MHz device).

The CY7C1339 supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$) at clock rise. Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{[3:0]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.

Logic Block Diagram



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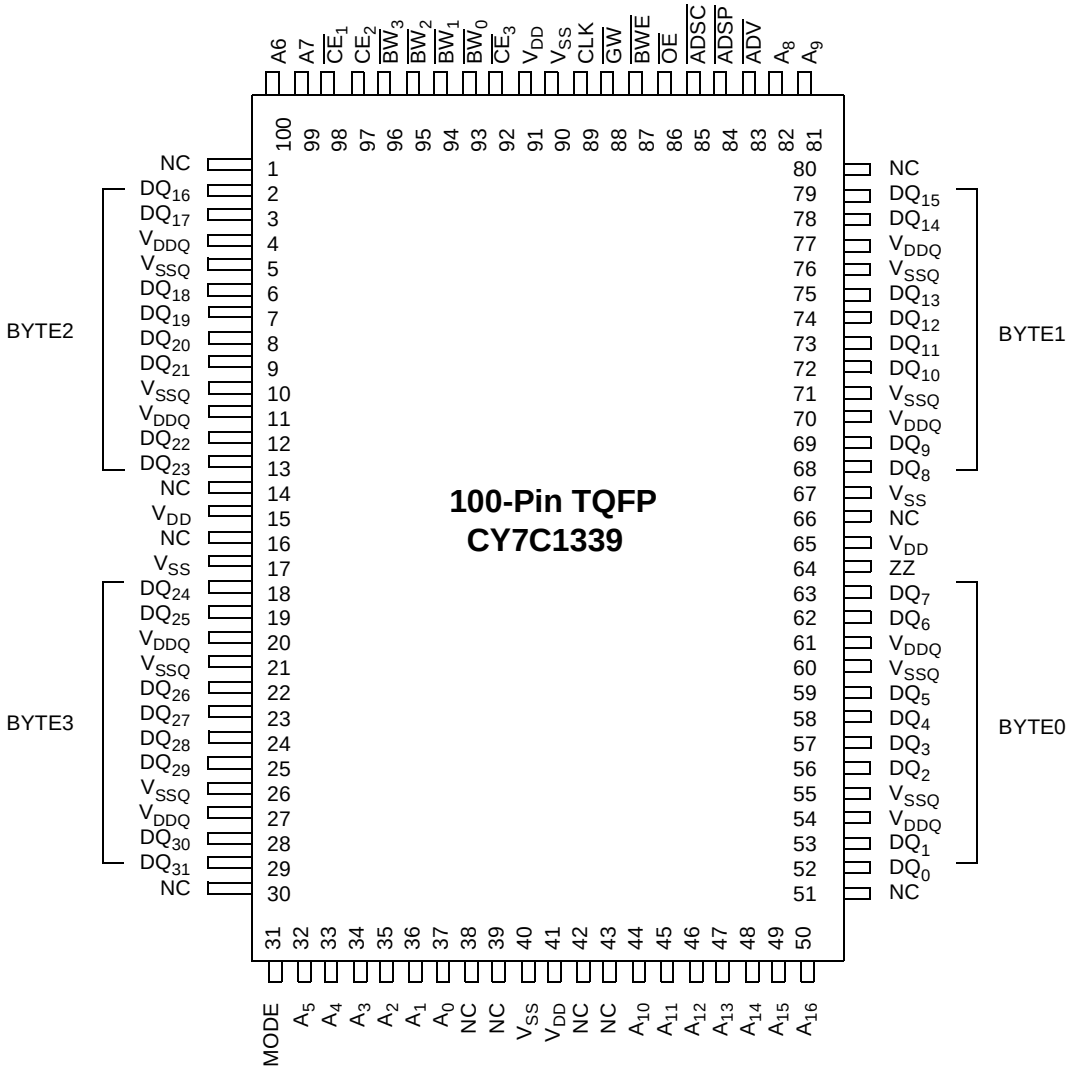
Pin Configuration



Selection Guide

		7C1339-166	7C1339-133	7C1339-100
Maximum Access Time (ns)		3.5	4.0	5.5
Maximum Operating Current (mA)	Commercial	420	375	325
Maximum CMOS Standby Current (mA)	Commercial	10	10	10

Pin Definitions

Pin Number	Name	I/O	Description
50–44, 81, 82, 99, 100, 32–37	$A_{[16:0]}$	Input-Synchronous	Address Inputs used to select one of the 64K address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
96–93	$\overline{BW}_{[3:0]}$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[3:0]}$ and $\overline{BWE}$).
87	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	CLK	Input-Clock	Clock input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
98	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.
97	CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
86	$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
83	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, $A_{[16:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deserted HIGH.
85	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[16:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
64	ZZ	Input-Asynchronous	ZZ “sleep” Input. This active HIGH input places the device in a non-time-critical “sleep” condition with data integrity preserved. Leaving ZZ floating or NC will default the device into an active state. ZZ has an internal pull down.
29, 28, 25-22, 19, 18,13,12, 9–6, 3, 2, 79, 78, 75–72, 69, 68, 63, 62 59–56, 53, 52	$DQ_{[31:0]}$	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[16:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, $DQ_{[31:0]}$ are placed in a three-state condition.
15, 41, 65, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
17, 40, 67, 90	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 3.3V or 2.5V power supply.
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.
31	MODE	Input-Static	Selects burst order. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. When left floating or NC, defaults to interleaved burst order. Mode pin has an internal pull up.
1, 14, 16, 30, 38, 39, 42, 43, 51, 66, 80	NC	-	No Connects.

Introduction

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.5 ns (166-MHz device).

The CY7C1339 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{[3:0]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs ($A_{[16:0]}$) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.5 ns (166-MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will three-state immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to $A_{[16:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[3:0]}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$-triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the $DQ_{[31:0]}$ inputs is written into the corresponding address location in the RAM core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}_{[3:0]}$ signals. The CY7C1339 provides byte write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW}_{[3:0]}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1339 is a common I/O device, the Output Enable ($\overline{OE}$) must be deserted HIGH before presenting data to the $DQ_{[31:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[31:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deserted HIGH, (3) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[3:0]}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$- triggered write accesses require a single clock cycle to complete. The address presented to $A_{[16:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the $DQ_{[31:0]}$ is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1339 is a common I/O device, the Output Enable ($\overline{OE}$) must be deserted HIGH before presenting data to the $DQ_{[31:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[31:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1339 provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		3	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Cycle Descriptions[1, 2, 3]

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	CE_2	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
ZZ “Sleep”	None	H	X	X	X	X	X	X	X	Hi-Z	X

Note:
1. X=”Don't Care,” 1=HIGH, 0=LOW.
2. Write is defined by $\overline{BWE}$, $\overline{BW}_{[3:0]}$, and $\overline{GW}$. See Write Cycle Descriptions table.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

Write Cycle Descriptions[4, 5, 6]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{BW_1}$	$\overline{BW_0}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 - $DQ_{[7:0]}$	1	0	1	1	1	0
Write Byte 1 - $DQ_{[15:8]}$	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - $DQ_{[23:16]}$	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - $DQ_{[31:24]}$	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[7] ..... –0.5V to V_{DD} + 0.5V

DC Input Voltage[7]..... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[8]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V –5%/+10%	2.5V –5% 3.3V /+10%
Ind'l	–40°C to +85°C	3.3V –5%/+10%	2.5V –5% 3.3V /+10%

Note:

4. X="Don't Care," 1=Logic HIGH, 0=Logic LOW.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[3:0]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ=High-Z when $\overline{OE}$ is inactive or when the device is deselected, and DQ=data when $\overline{OE}$ is active.
7. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
8. T_A is the case temperature.

Electrical Characteristics Over the Operating Range

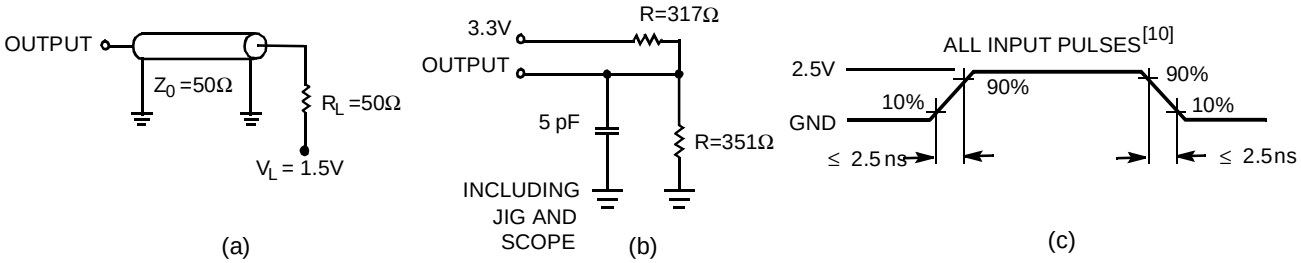
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage	3.3V –5%/+10%		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	2.5V –5% to 3.3V +10%		2.375	3.6	V
V_{OH}	Output HIGH Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OH} = –2.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OL} = 2.0 mA			0.7	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[7]	V_{DDQ} = 3.3V		–0.3	0.8	V
V_{IL}	Input LOW Voltage[7]	V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DDQ}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DDQ}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		420	mA
			7.5-ns cycle, 133 MHz		375	mA
			10-ns cycle, 100 MHz		325	mA
I_{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		150	mA
			7.5-ns cycle, 133 MHz		125	mA
			10-ns cycle, 100 MHz		115	mA
I_{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speeds		10	mA
I_{SB3}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		125	mA
			7.5-ns cycle, 133 MHz		95	mA
			10-ns cycle, 100 MHz		85	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0			18	mA

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V. V_{DDQ} = 3.3V	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

Note:
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[11,12,13]

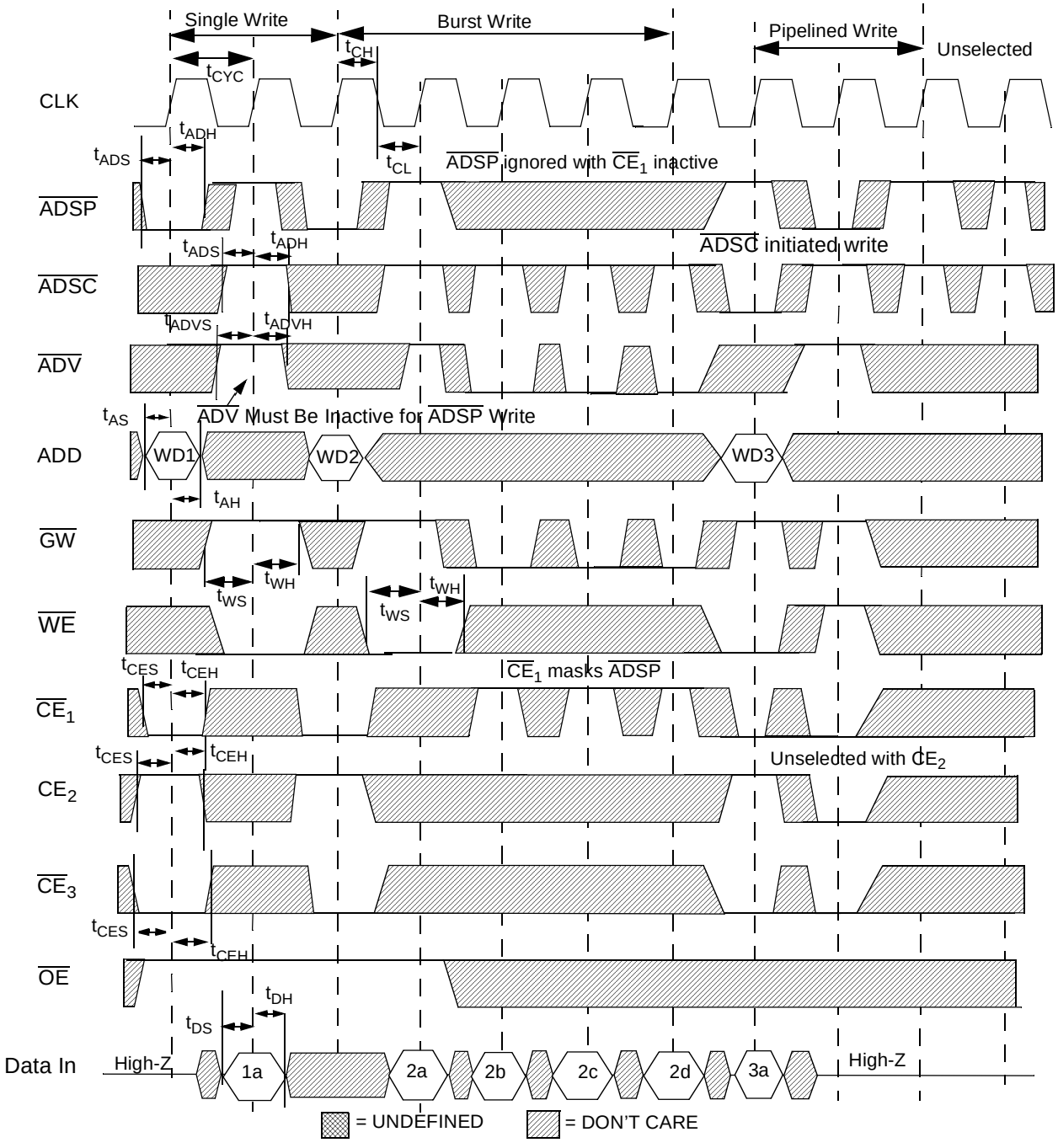
Parameter	Description	-166		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	6.0		7.5		10		ns
t_{CH}	Clock HIGH	1.7		1.9		3.5		ns
t_{CL}	Clock LOW	1.7		1.9		3.5		ns
t_{AS}	Address Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		3.5		4.0		5.5	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5		2.0		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}$[3:0] Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{WEH}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}$[3:0] Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CES}	Chip Select Set-Up	2.0		2.5		2.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[12]		3.5		3.5		3.5	ns
t_{CLZ}	Clock to Low-Z[12]	0		0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[12, 13]		3.5		3.5		5.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[12, 13]	0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[12]		3.5		4.0		5.5	ns

Notes:

10. Input waveform should have a slew rate of 1 V/ns.
11. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
12. t_{CHZ}, t_{CLZ}, t_{EOV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mf from steady-state voltage.
13. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ}.

Switching Waveforms

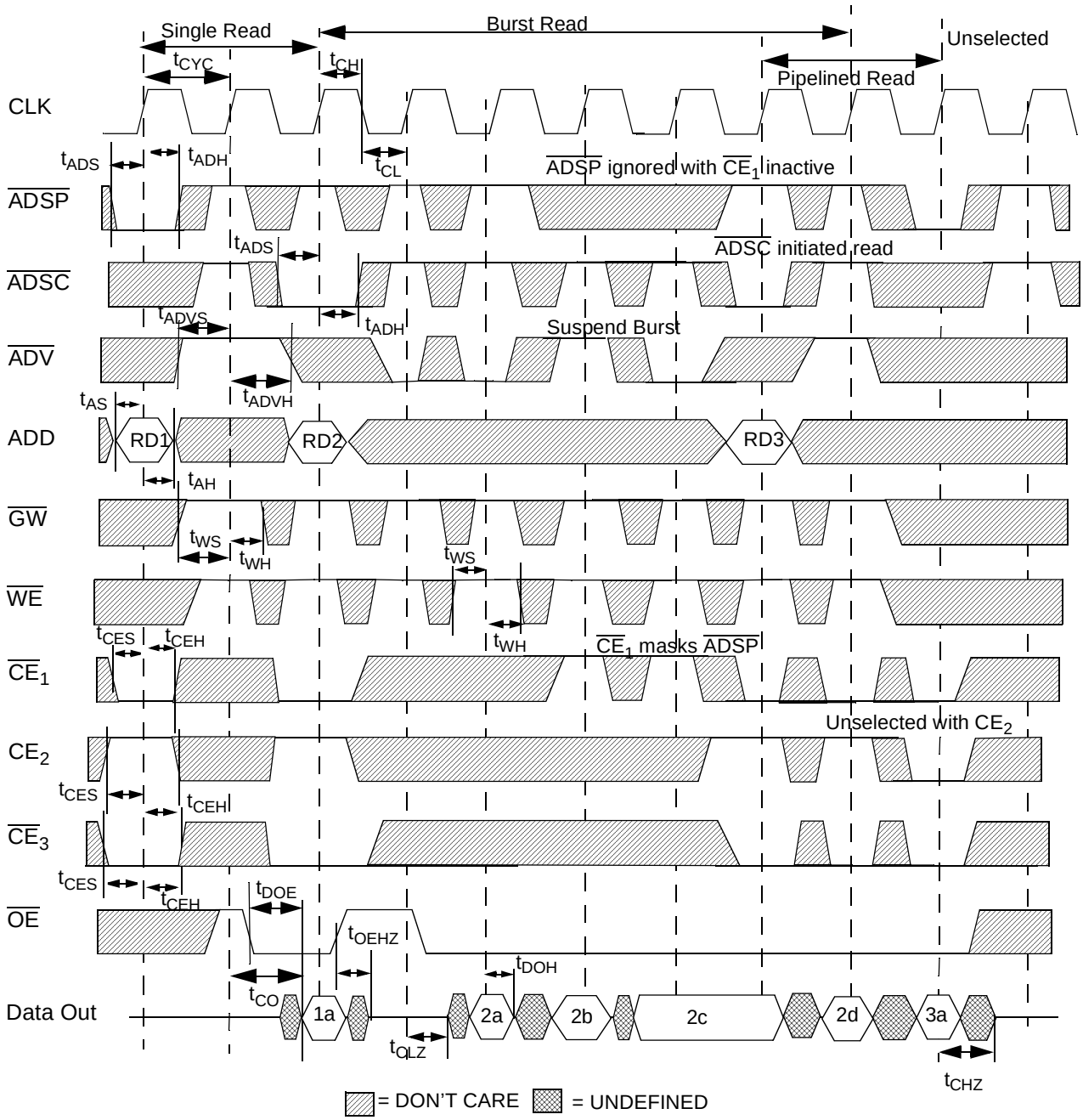
Write Cycle Timing[14, 15]



Notes:
14. $\overline{WE}$ is the combination of $\overline{BWE}$, $\overline{BW}_{[3:0]}$, and $\overline{GW}$ to define a write cycle (see Write Cycle Descriptions table).
15. WDx stands for Write Data to Address X.

Switching Waveforms (continued)

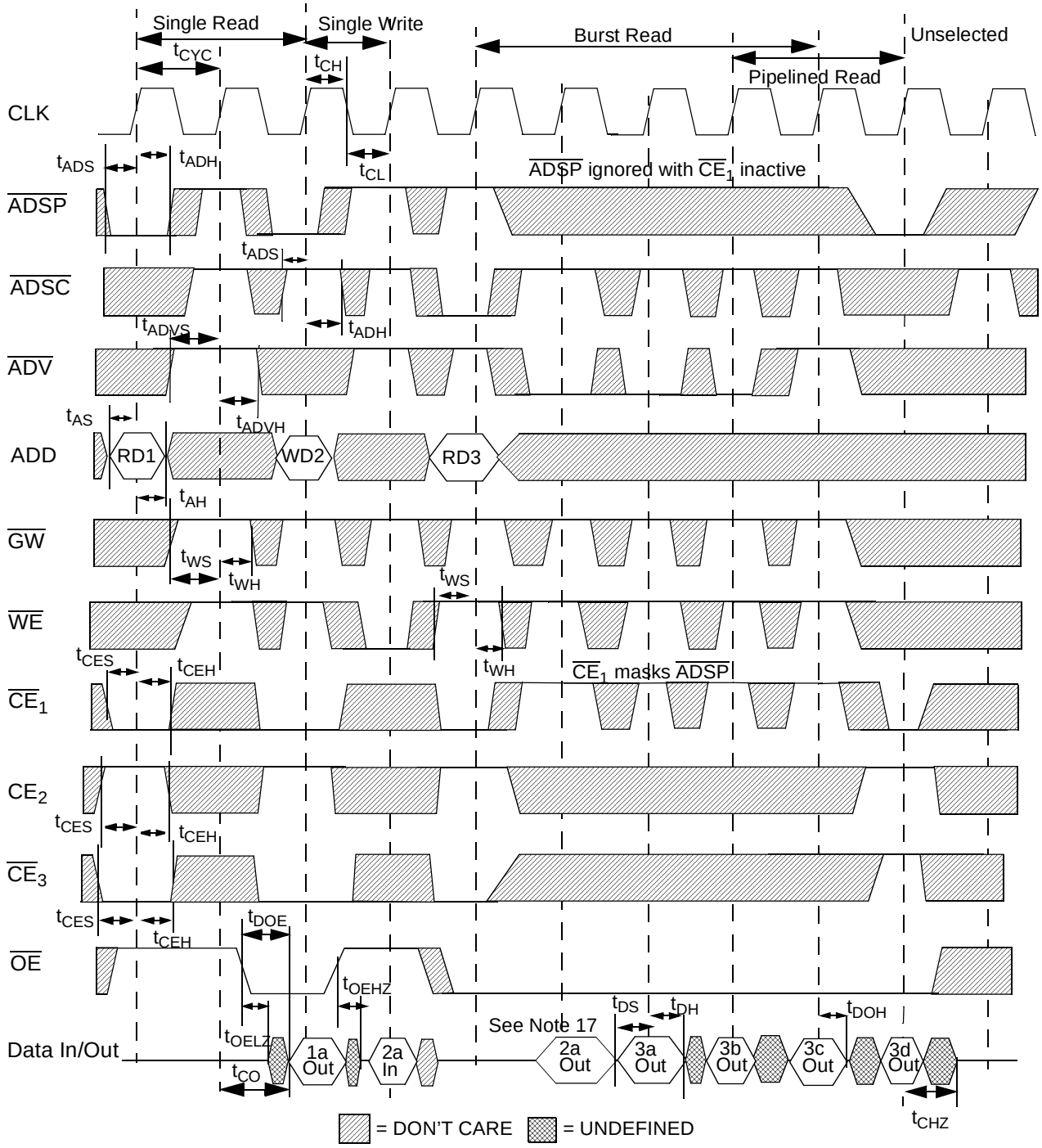
Read Cycle Timing[14, 16]



Note:
16. RDx stands for Read Data from Address X.

Switching Waveforms (continued)

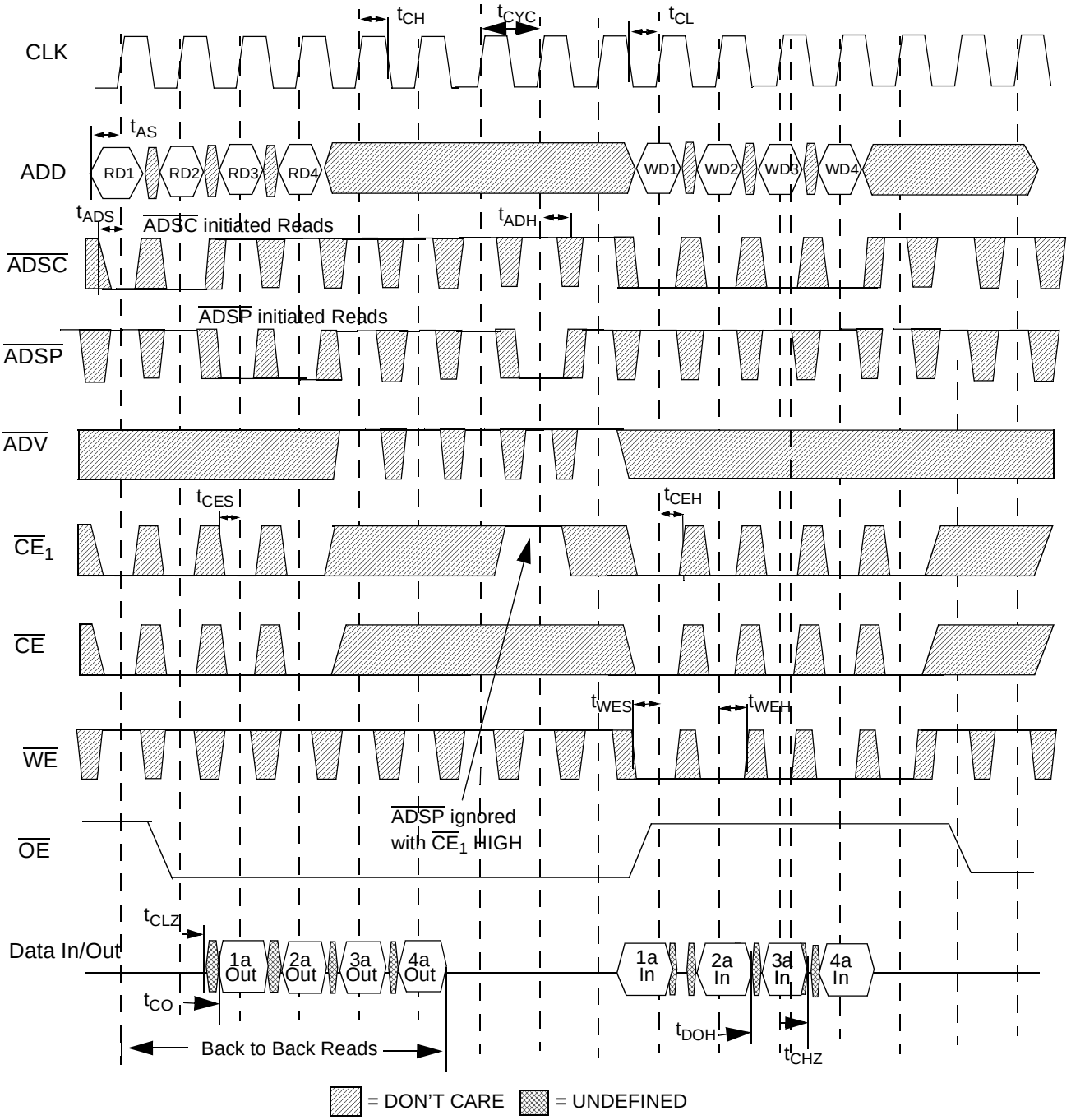
Read/Write Cycle Timing[14, 15, 16, 17]



Note:
17. Data bus is driven by SRAM, but data is not guaranteed.

Switching Waveforms (continued)

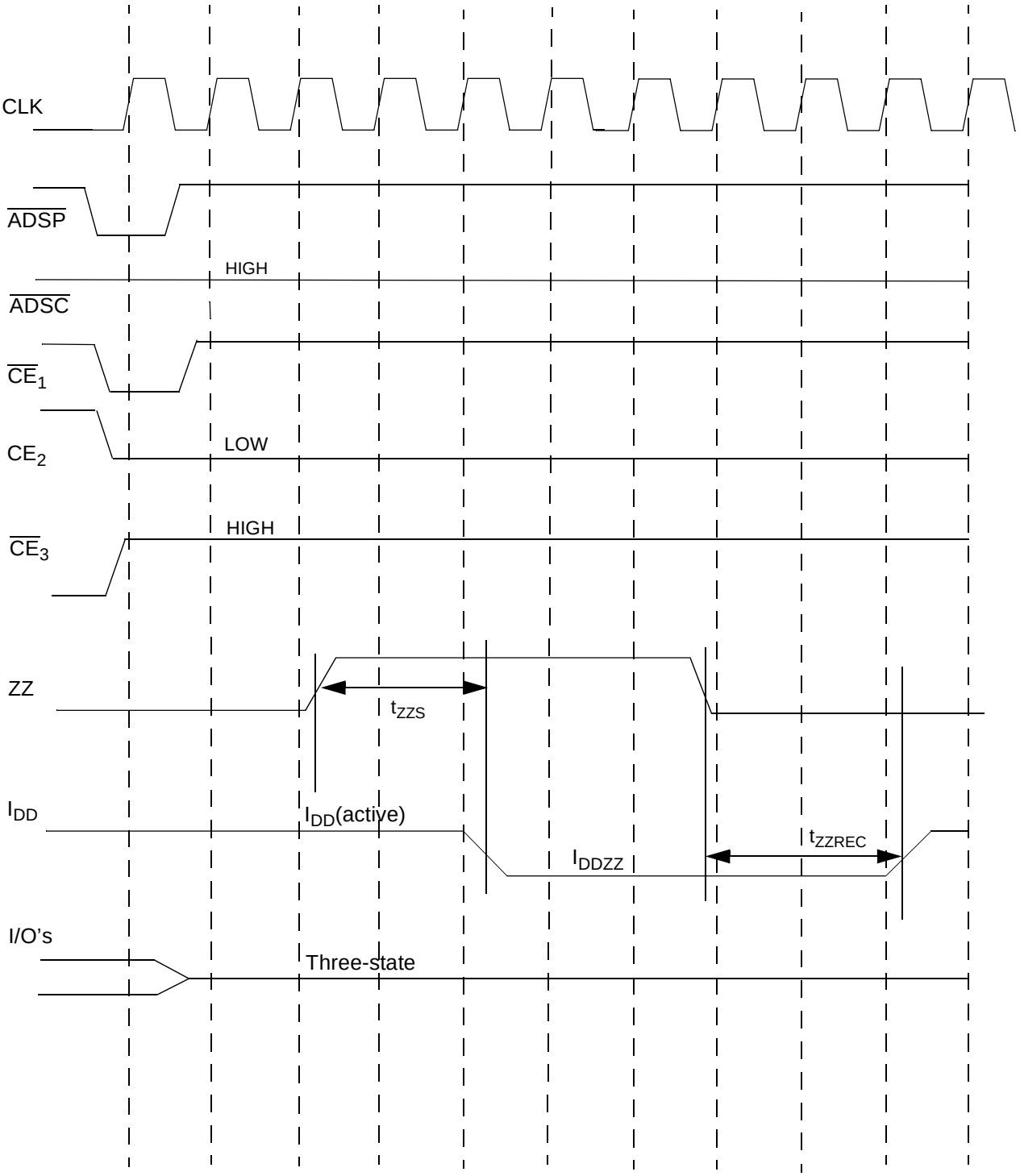
Pipeline Timing[18, 19]



Notes:
18. Device originally deselected.
19. $\overline{CE}$ is the combination of CE_2 and $\overline{CE}_3$. All chip selects need to be active in order to select the device.

Switching Waveforms (continued)

ZZ Mode Timing [20, 21]



Note:
20. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
21. I/Os are in three-state when exiting ZZ sleep mode.

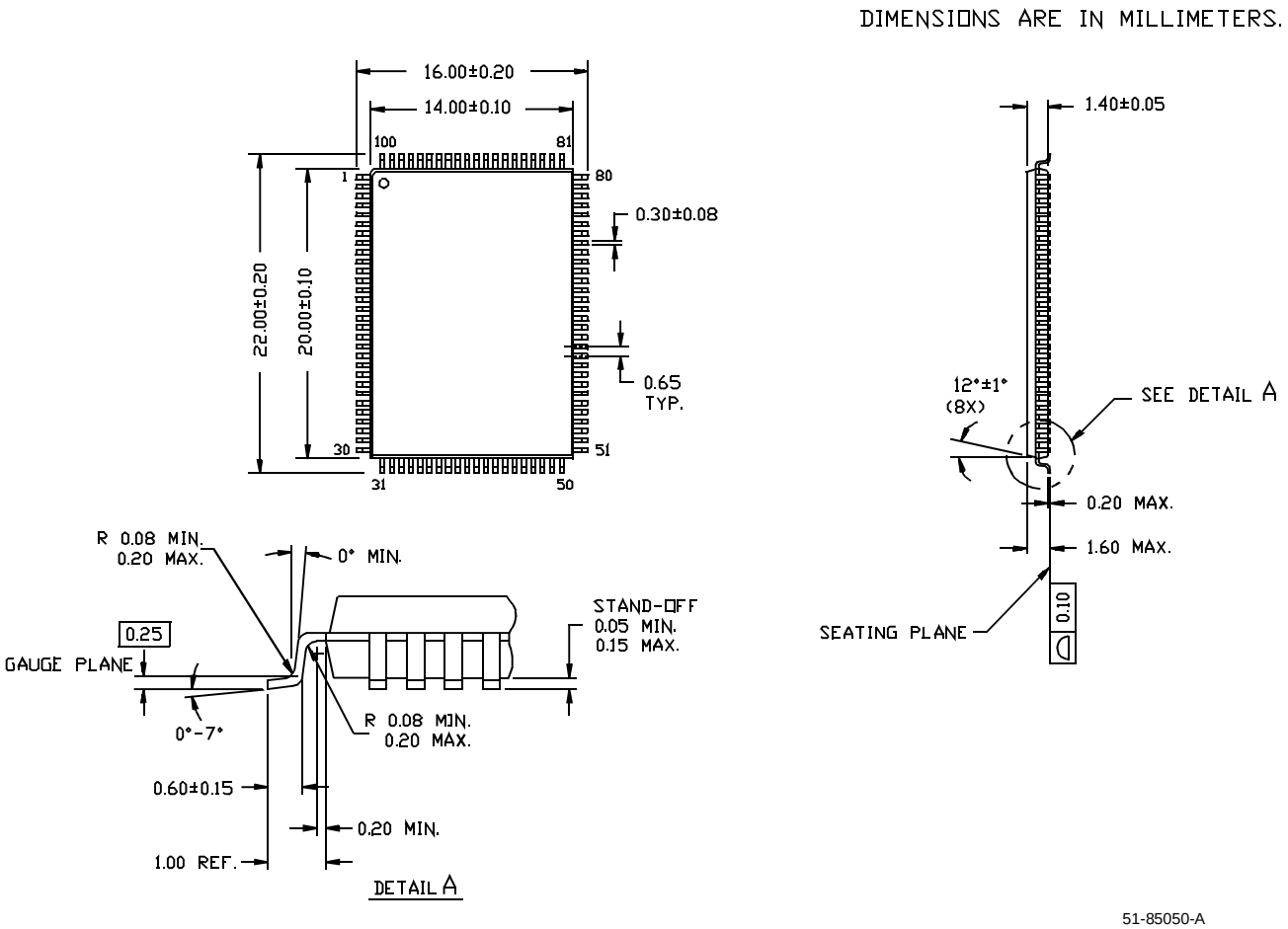
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C1339-166AC	A101	100-Lead Thin Quad Flat Pack	Commercial
133	CY7C1339-133AC			
100	CY7C1339-100AC			
133	CY7C1339-133AI			Industrial

Document #: 38-00723-C

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, D-TYPE LATCHES, CASCADABLE, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, advanced low-power Schottky TTL, D-type latches, bistable logic microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types shall be as follows:

Device type	Circuit
01	Octal D-type transparent latch with 3-state outputs, cascadable
02	Octal D-type transparent latch with inverted 3-state outputs, cascadable
03	Dual 4-bit D-type transparent latch with 3-state outputs, cascadable
04	Dual 4-bit D-type transparent latch with inverted 3-state outputs, cascadable

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
K	F-6 (24-lead, 3/8" x 5/8"), flat package
L	D-9 (24-lead, 1/4" x 1 1/4"), dual-in-line package
R	D-8 (20-lead, 1/4" x 1 1/16"), dual-in-line package
S	F-9 (20-lead, 1/4" x 1/2"), flat package
2	C-2 (20 terminal, .350" x .350") square chip carrier package
3	C-4 (28-terminal, .450" x .450") square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to 7.0 V dc
Storage temperature	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/:	
Device types 01 and 02	148.5 mW
Device types 03 and 04	170.5 mW
Lead temperature (soldering, 10 seconds)	300°C

1/ Must withstand the added P_D due to short-circuit test (e.g., I_O).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
FSC 5962

Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, R, S	(See MIL-M-38510, appendix C)
Cases 2, 3	60°C/W 2/
Junction temperature (T_J) 3/	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input set-up time, $t_{(setup)}$:	
Device types 01, 02, 03, and 04	10 ns minimum
Input hold time, $t_{(hold)}$:	
Device types 01 and 03	7 ns minimum
Device types 02 and 04	10 ns minimum
Input pulse width, (t_p):	
Device types 01 and 03 (Enable)	10 ns minimum
Device types 02 and 04 (Enable)	15 ns minimum
Device type 03 (Clear)	15 ns minimum
Device type 04 (Preset)	15 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and logic diagrams. The terminal connections and logic diagrams shall be as specified on figures 1 and 2 respectively.

2/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening methods per method 5004 of MIL-STD-883.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$		Device type	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = 1.0 mA V_{IH} = 2.0 V		All	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 12 mA V_{IL} = 0.8 V		All		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA T_C = +25°C		All		-1.5	V
Low-level input current	I_{IL}	V_{CC} = 5.5 V V_{IL} = 0.4 V		All	0	-200	µA
High-level input current	I_{IH1}	V_{CC} = 5.5 V V_{IH} = 2.7 V		All		20	µA
	I_{IH2}	V_{CC} = 5.5 V V_{IH} = 7.0 V		All		110	µA
Output current 1/	I_O	V_{CC} = 5.5 V V_O = 2.25 V		01	-15	-112	mA
				02,03,04	-15	-110	
Output current, high level, outputs off	I_{OZH}	V_{CC} = 5.5 V V_{OH} = 2.7 V		All		20	µA
Output current, low level, outputs off	I_{OZL}	V_{CC} = 5.5 V V_{OH} = 0.4 V		All		-20	µA
Supply current, outputs high	I_{CCH}	V_{CC} = 5.5 V	V_{IN} = 5.0 V	01		19	mA
				03		21	
			V_{IN} = 0 V	02		17	
				04		21	
Supply current, outputs low	I_{CCL}	V_{CC} = 5.5 V	V_{IN} = 0 V	01		24	mA
				03		29	
			V_{IN} = 5.0 V	02		24	
				04		29	
Supply current, outputs disabled	I_{CCZ}	V_{CC} = 5.5 V V_{OC} = 5.0 V	V_{IN} = 0 V	01		27	mA
				03		31	
			V_{IN} = 5.5 V	02		27	
				04		31	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Device type	Limits Min	Limits Max	Unit
Propagation delay time to low level (clear or preset to output)	t_{PHL1}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_L = 500Ω	03,04	6	24	ns
Propagation delay time to high level (enable to output)	t_{PLH2}		01	8	27	ns
			02,03	8	29	
			04	8	31	
Propagation delay time to low level (enable to output)	t_{PHL2}		01	8	20	ns
			02,03, 04	8	22	
Propagation delay time to high level (data to output)	t_{PLH3}		01,03	2	15	ns
			02	3	21	
			04	3	23	
Propagation delay time to low level (data to output)	t_{PHL3}		01,03	2	15	ns
			02,04	3	15	
Output control on to high-level output	t_{PZH}		All	4	21	ns
Output control on to low-level output	t_{PZL}		All	4	21	ns
High-level output to output control off	t_{PHZ}		01	2	12	ns
			02,03,04	2	10	
Low-level output to output control off	t_{PLZ}		01	3	18	ns
			02,04	3	15	
			03	2	15	

1/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

3.2.2 Truth tables. The truth tables shall be as specified on figure 3.

3.2.3 Schematic circuits. Schematic circuits shall be submitted to the preparing activity prior to inclusion of a manufacturer's device in the specification and shall be submitted to the qualifying activity and agent activity (DESC-ECS) as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained by the agent activity and will be available upon request.

3.2.4 Case outlines. The case outlines shall be as specified in MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical tests (method 5004)	1*,2,3,7, 9,10,11	1*,2,3,7, 9
Group A test requirements (method 5005)	1,2,3,7, 8,9,10,11	1,2,3,7, 9
Group B electrical tests (method 5005) subgroup 5	1,2,3,9, 10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1,2,3
Additional electrical subgroups for group C periodic inspections	N/A	10,11
Group D end-point electrical parameters (method 5005)	1,2,3	1,2,3

*PDA applies to subgroup 1 (see 4.2c).

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 10 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and MIL-STD-883, methods 5005 and 5007, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883.

(1) Test condition D or E, using the circuit shown on figure 4, or equivalent.

(2) T_A = +125°C minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical test parameters prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.

c. Steady-state life test (see method 1005 of MIL-STD-883):

(1) Test condition D or E, using the circuit shown on figure 4, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510, and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

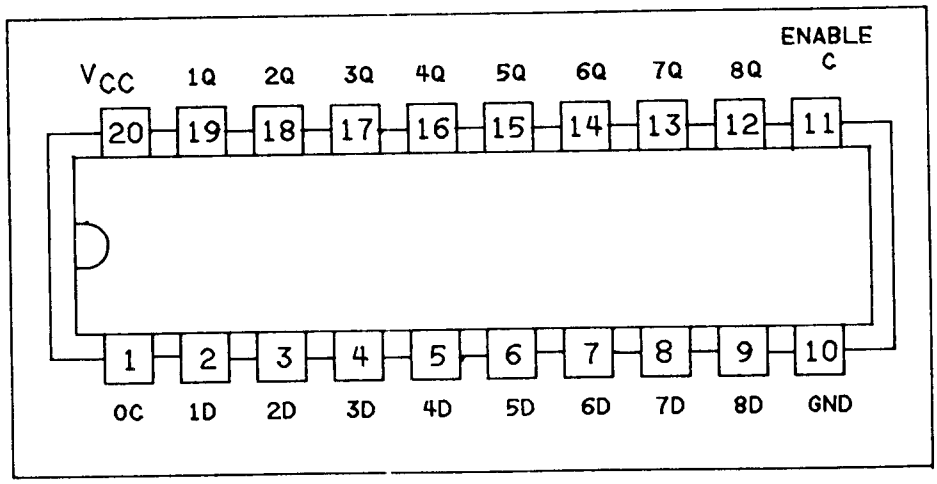
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be as specified in MIL-M-38510.

Device type 01

Cases R and S



Device type 01

Case 2

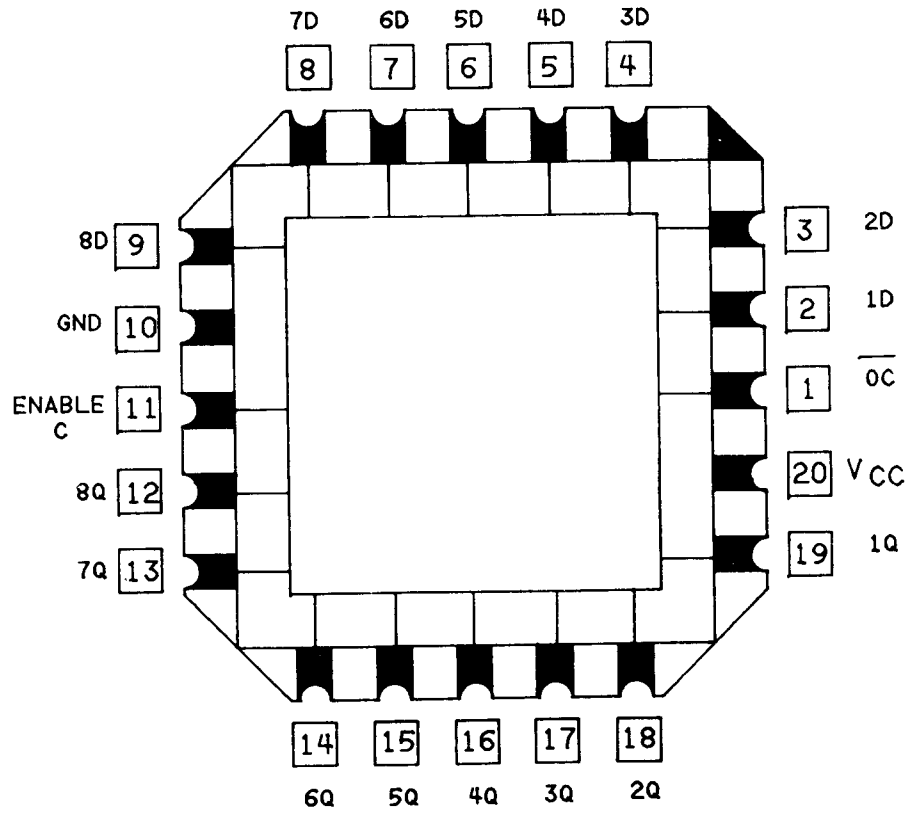
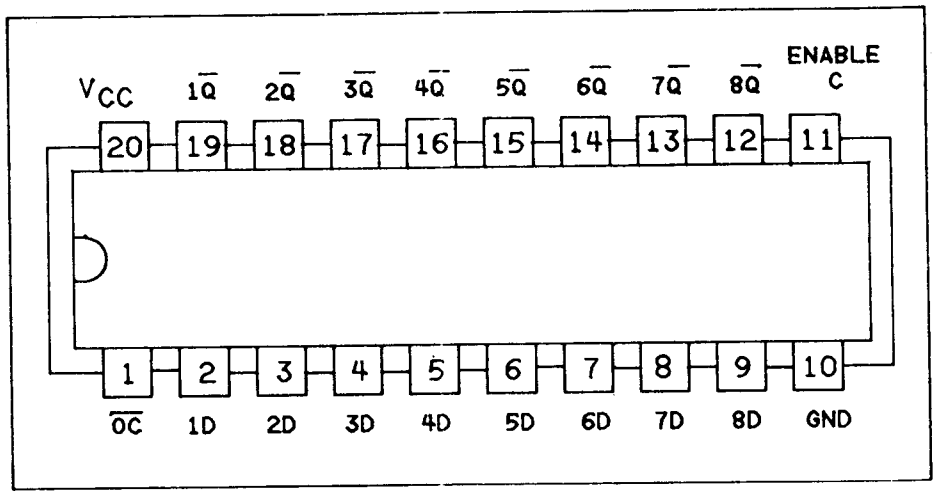


FIGURE 1. Terminal connections.

Device type 02

Cases R and S



Device Type 02

Case 2

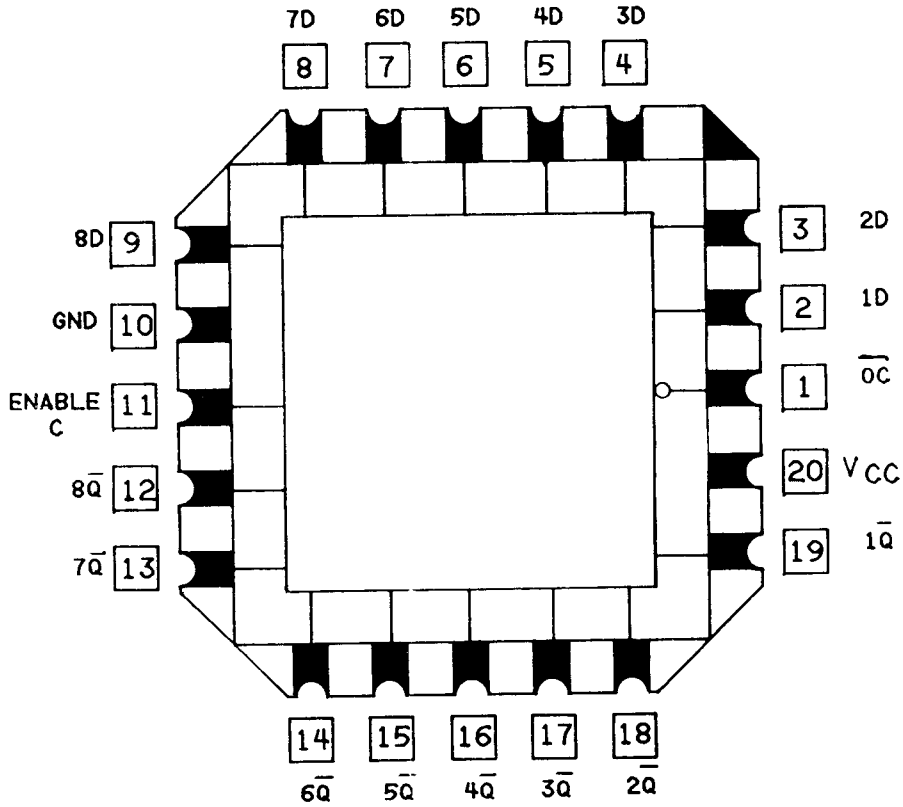
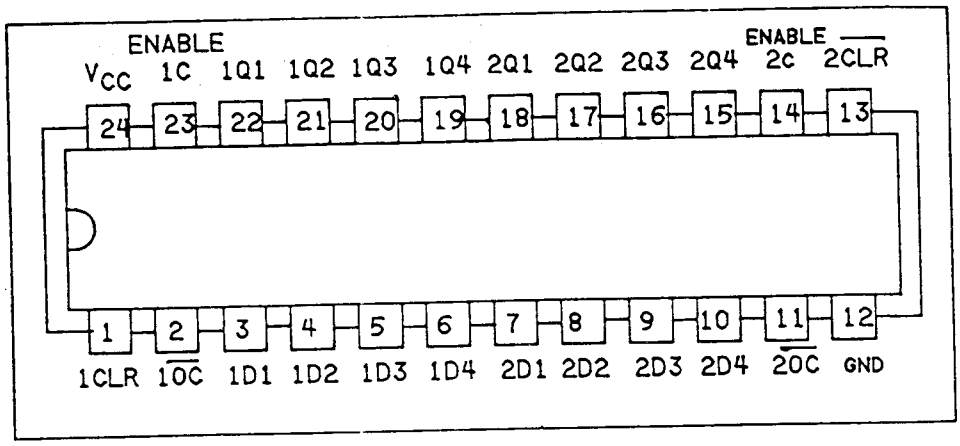


FIGURE 1. Terminal connections - Continued.

Device type 03

Cases K and L



Device type 03

Case 3

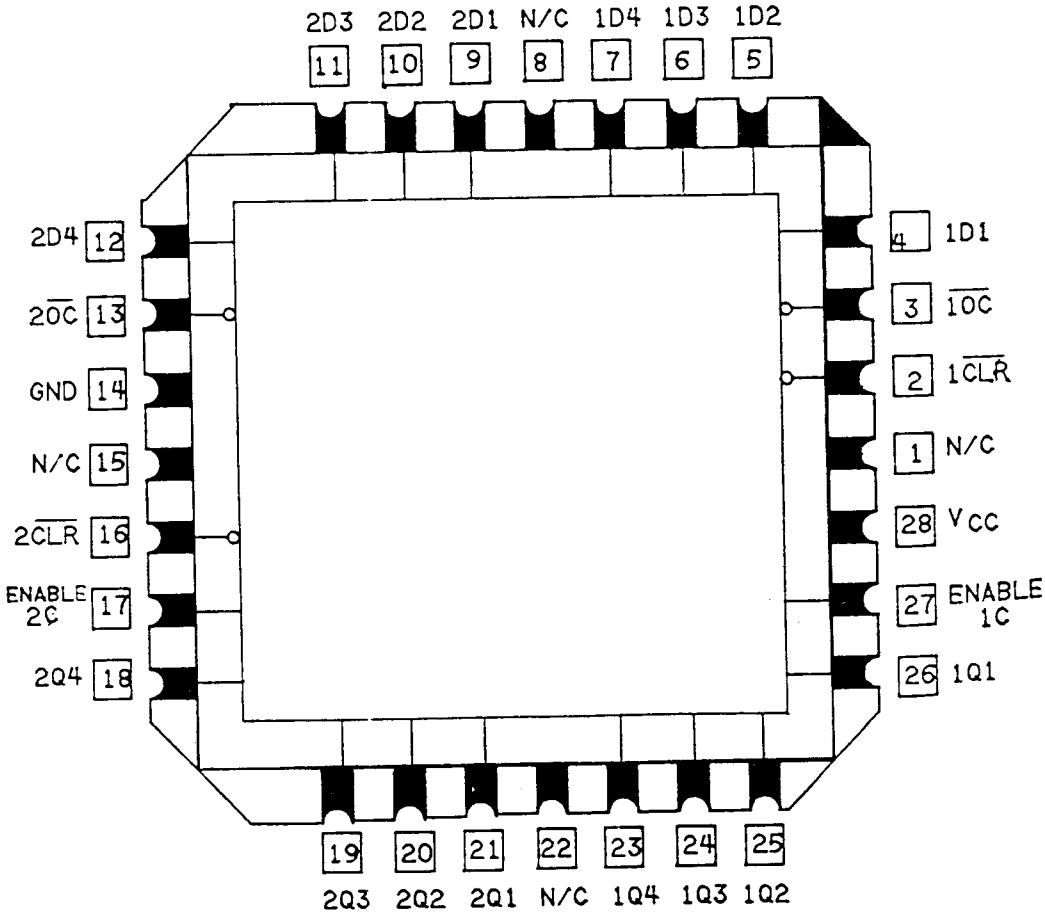
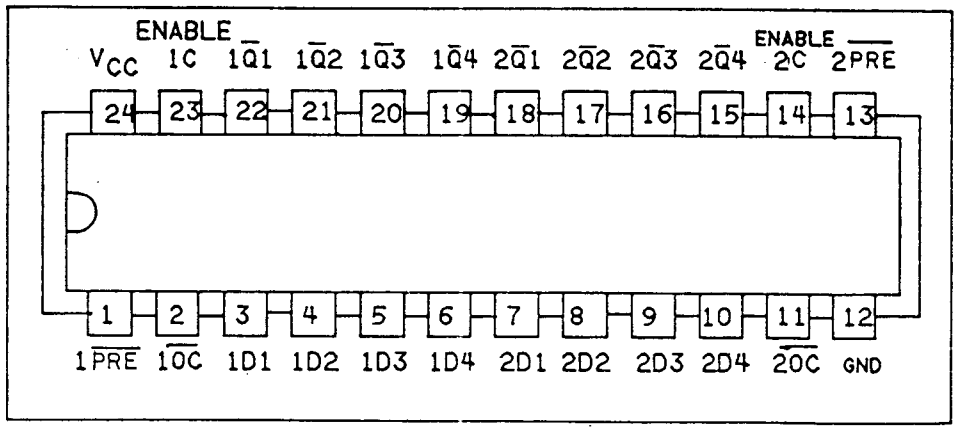


FIGURE 1. Terminal connections - Continued.

Device type 04

Cases K and L



Device type 04

Case 3

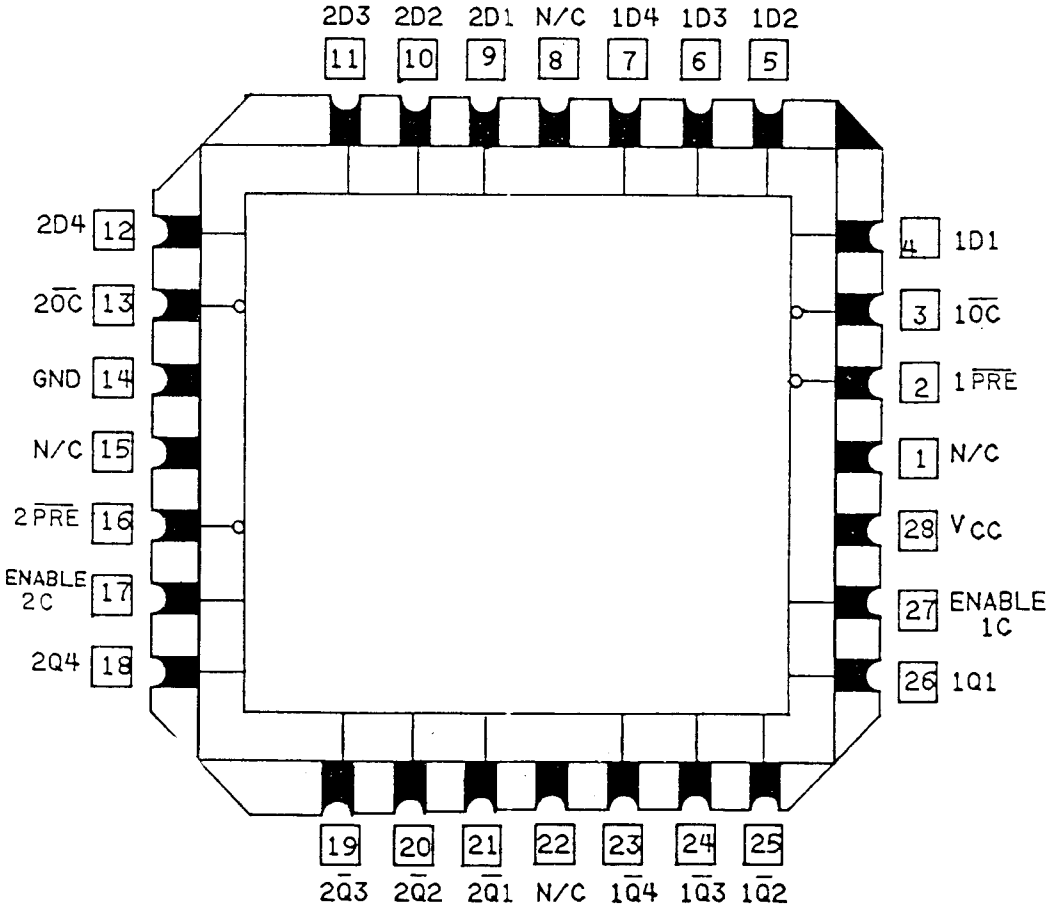


FIGURE 1. Terminal connections - Continued.

Device type 01

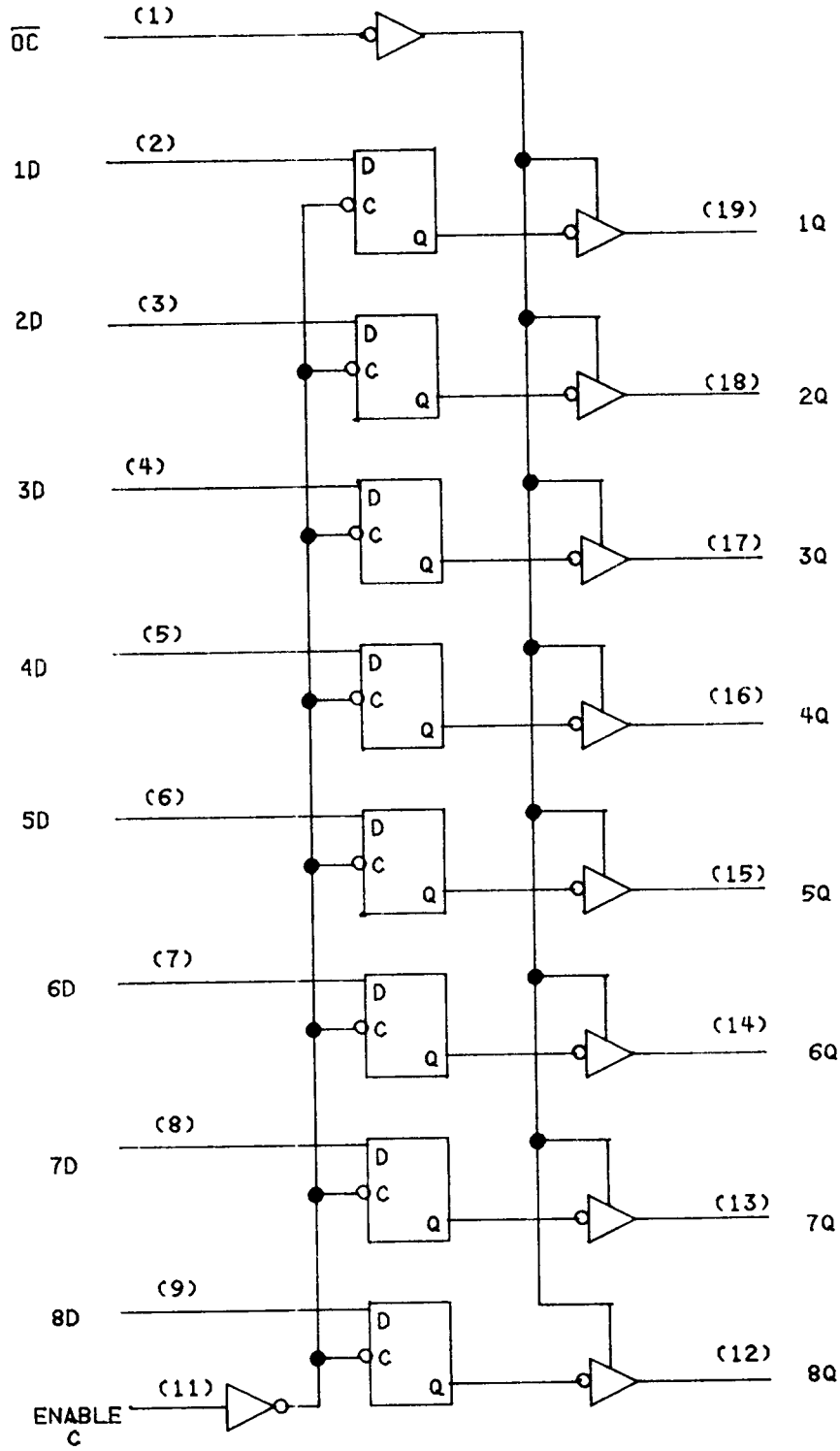


FIGURE 2. Logic diagrams.

Device type 02

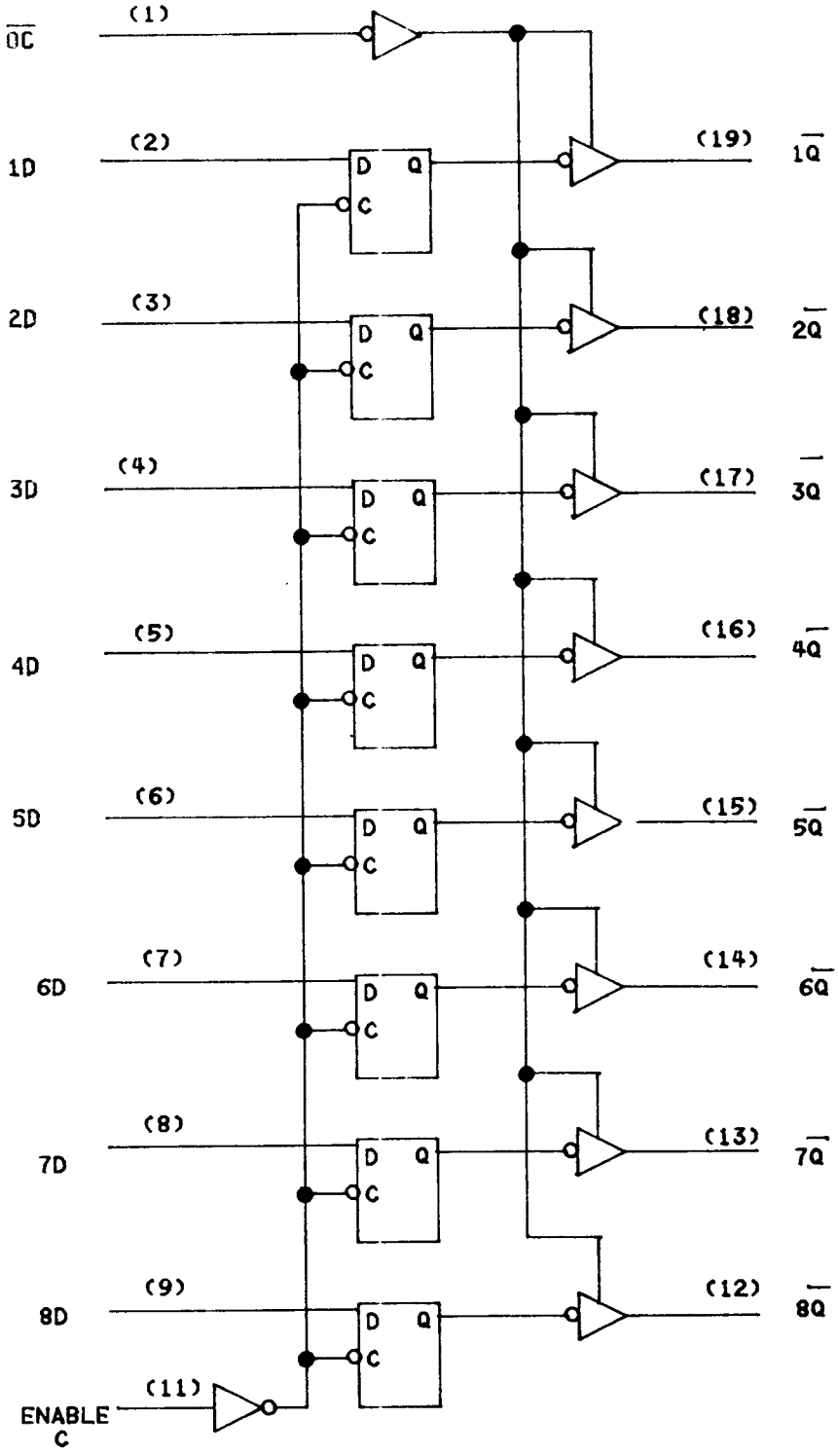


FIGURE 2. Logic diagrams - Continued.

Device type 03

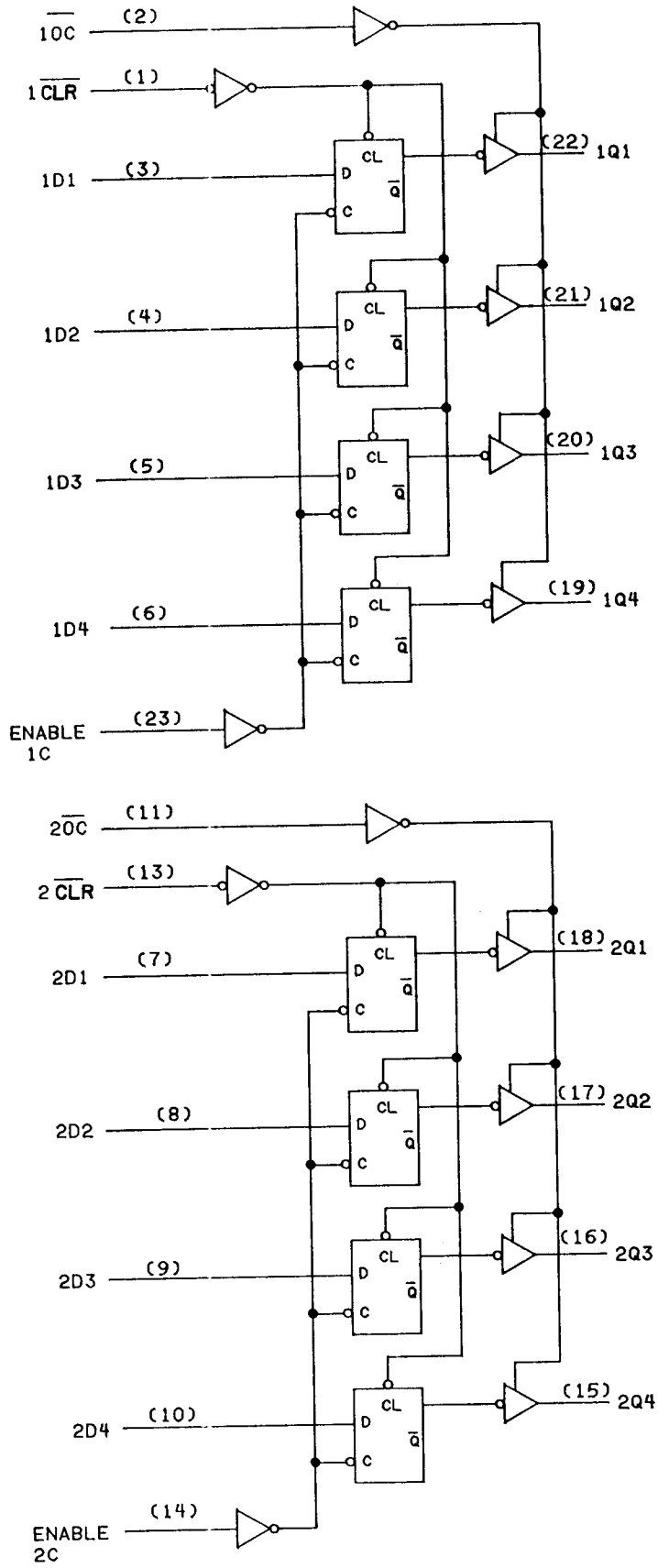


FIGURE 2. Logic diagrams - Continued.

Device type 04

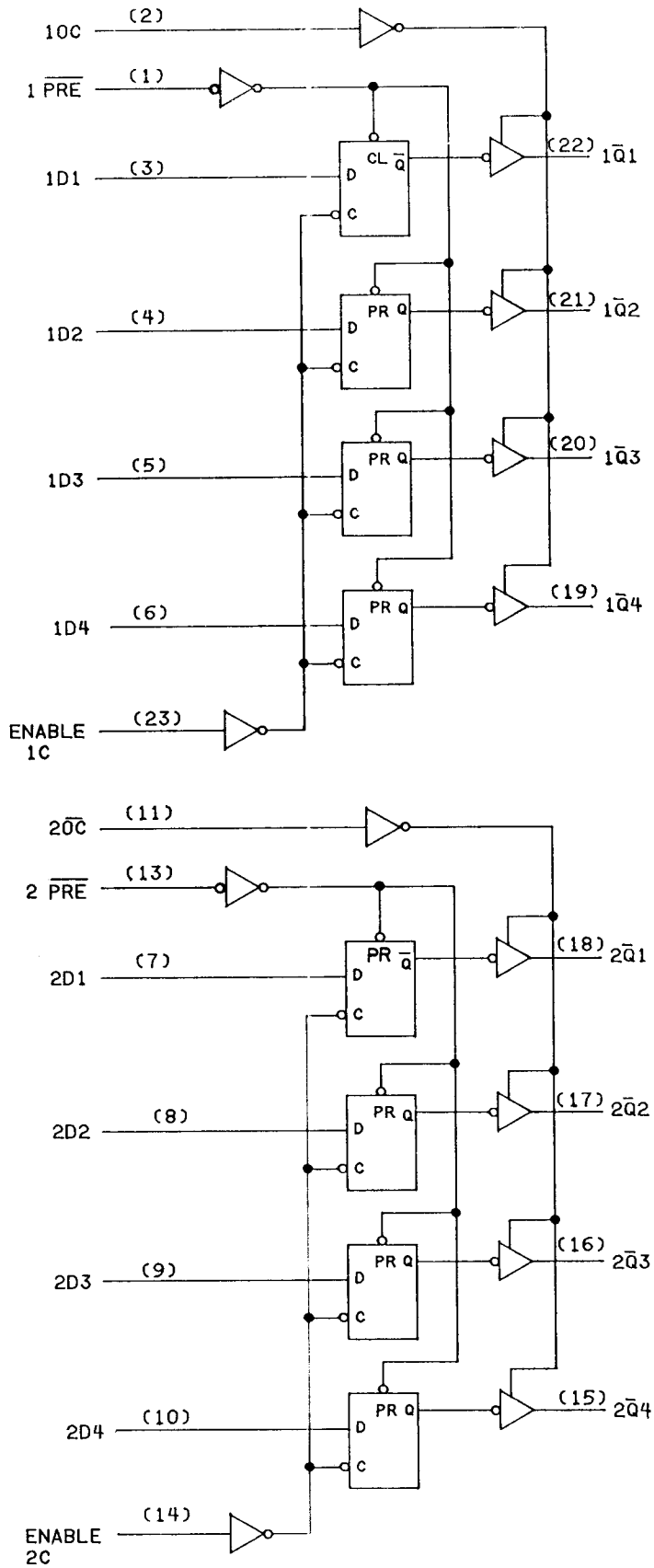


FIGURE 2. Logic diagrams - Continued.

Device type 01

Output control	Enable	Data	Output
$\overline{OC}$	EN C	D	Q
H	X	X	Z
L	L	X	Q_0
L	H	L	L
L	H	H	H

Device type 02

Output control	Enable	Data	Output
$\overline{OC}$	EN C	D	$\overline{Q}$
H	X	X	Z
L	L	X	$\overline{Q}_0$
L	H	L	H
L	H	H	L

Device type 03

Output control	Clear	Enable	Data	Output
$\overline{OC}$	$\overline{CLR}$	EN C	D	Q
H	X	X	X	Z
L	L	X	X	L
L	H	L	X	Q_0
L	H	H	L	L
L	H	H	H	H

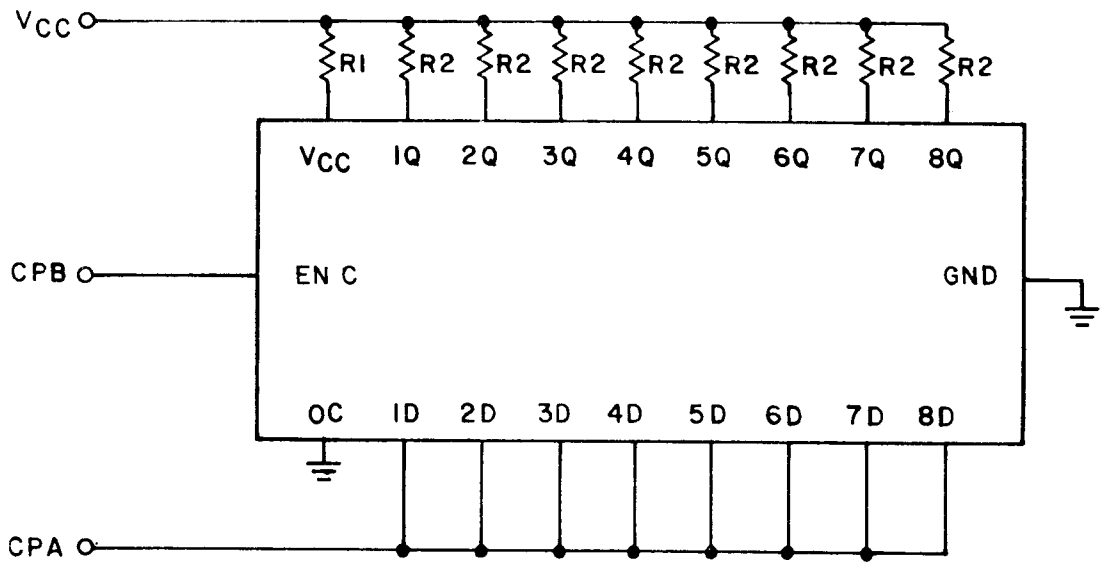
Device type 04

Output control	Preset	Enable	Data	Output
$\overline{OC}$	$\overline{PRE}$	EN C	D	$\overline{Q}$
H	X	X	X	Z
L	L	X	X	L
L	H	L	X	Q_0
L	H	H	L	H
L	H	H	H	L

H = High level (steady state)
L = Low level (steady state)
Z = High impedance state
X = Irrelevant
Q_0 = The level of Q or $\overline{Q}$ before the indicated input conditions were established.

FIGURE 3. Truth tables.

Device type 01



Device type 02

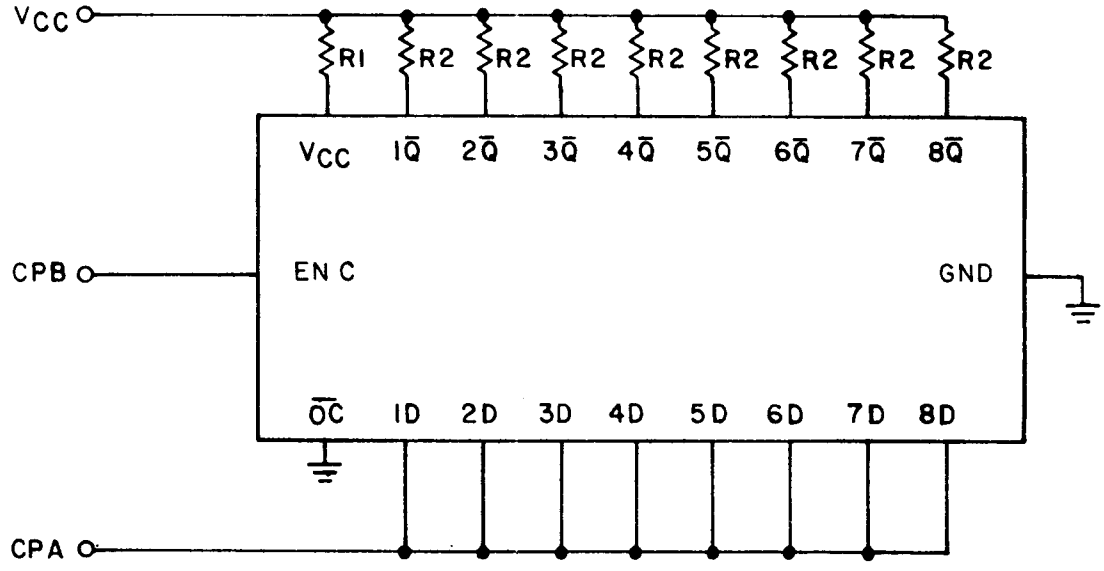
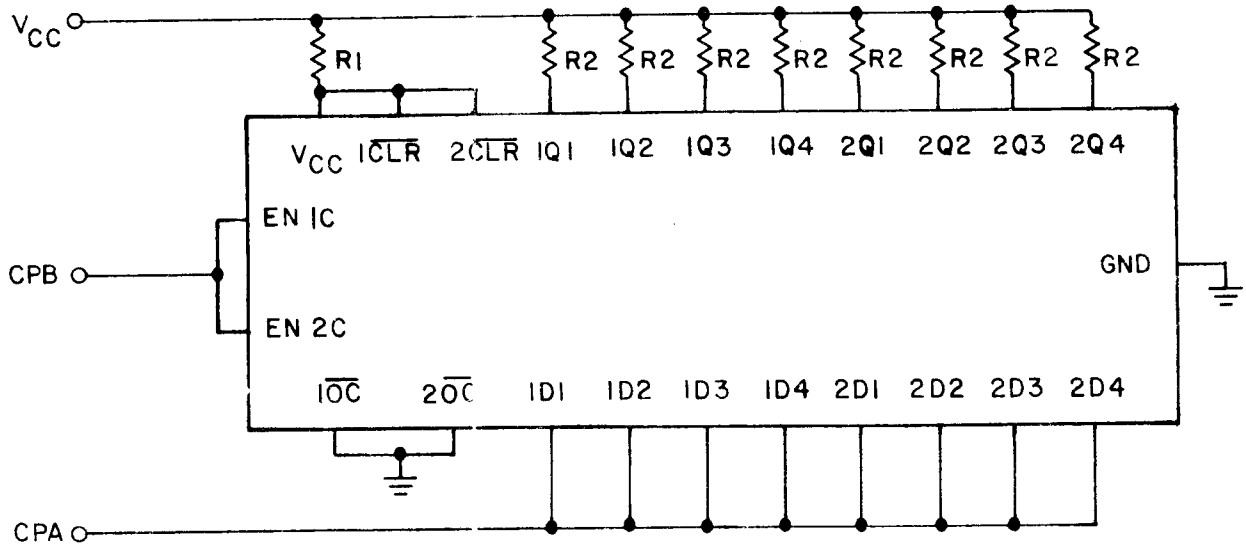
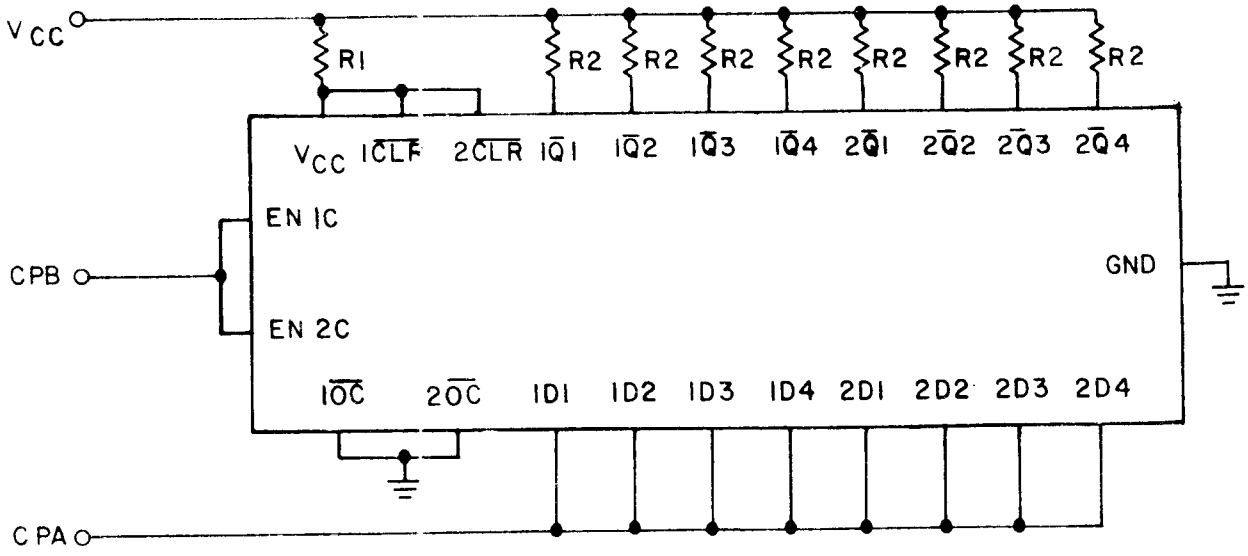


FIGURE 4. Burn-in and life test circuits.

Device type 03

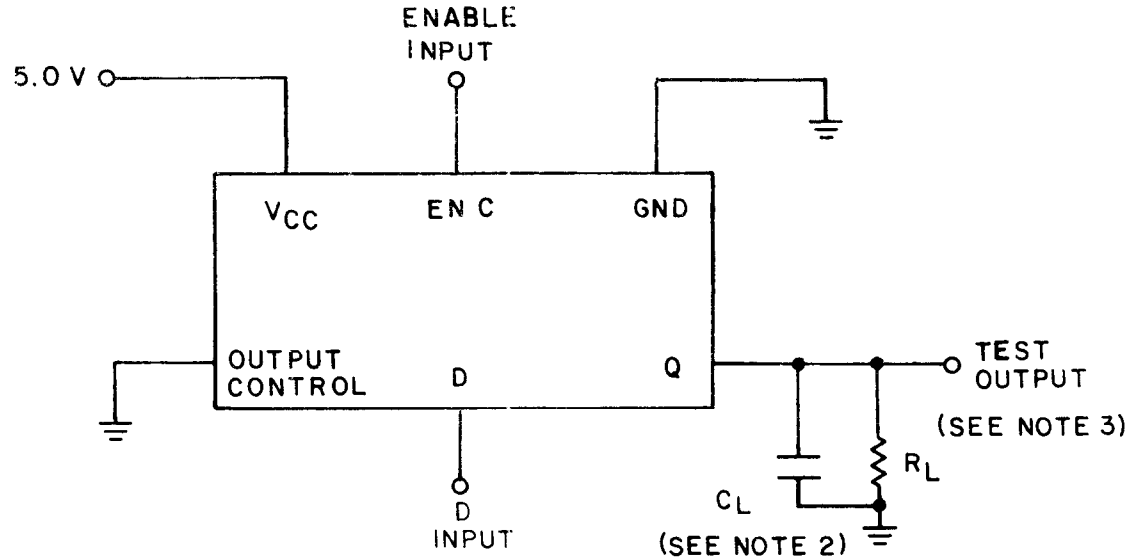


Device type 04

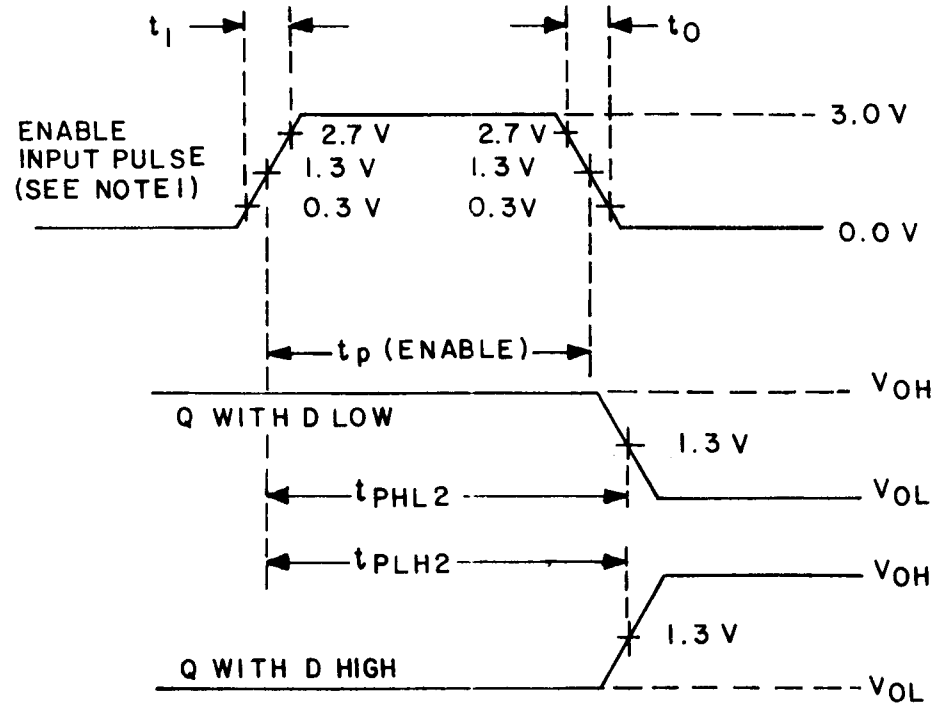


NOTES:
1. CPA = 100 kHz 50% square wave; duty cycle = 50 ±15%; V_{IL} = -0.5 V minimum to 0.7 V maximum; V_{IH} = 2.0 V minimum to 5.5 V maximum.
2. CPB is same as CPA, synchronized with CPA, except 50 kHz ±50% square wave.
3. R2 = 470Ω ±5%.
4. R_1 and V_{CC} shall be chosen to insure 5.0 V minimum is present at device V_{CC} terminal.

FIGURE 4. Burn-in and life test circuits - Continued.



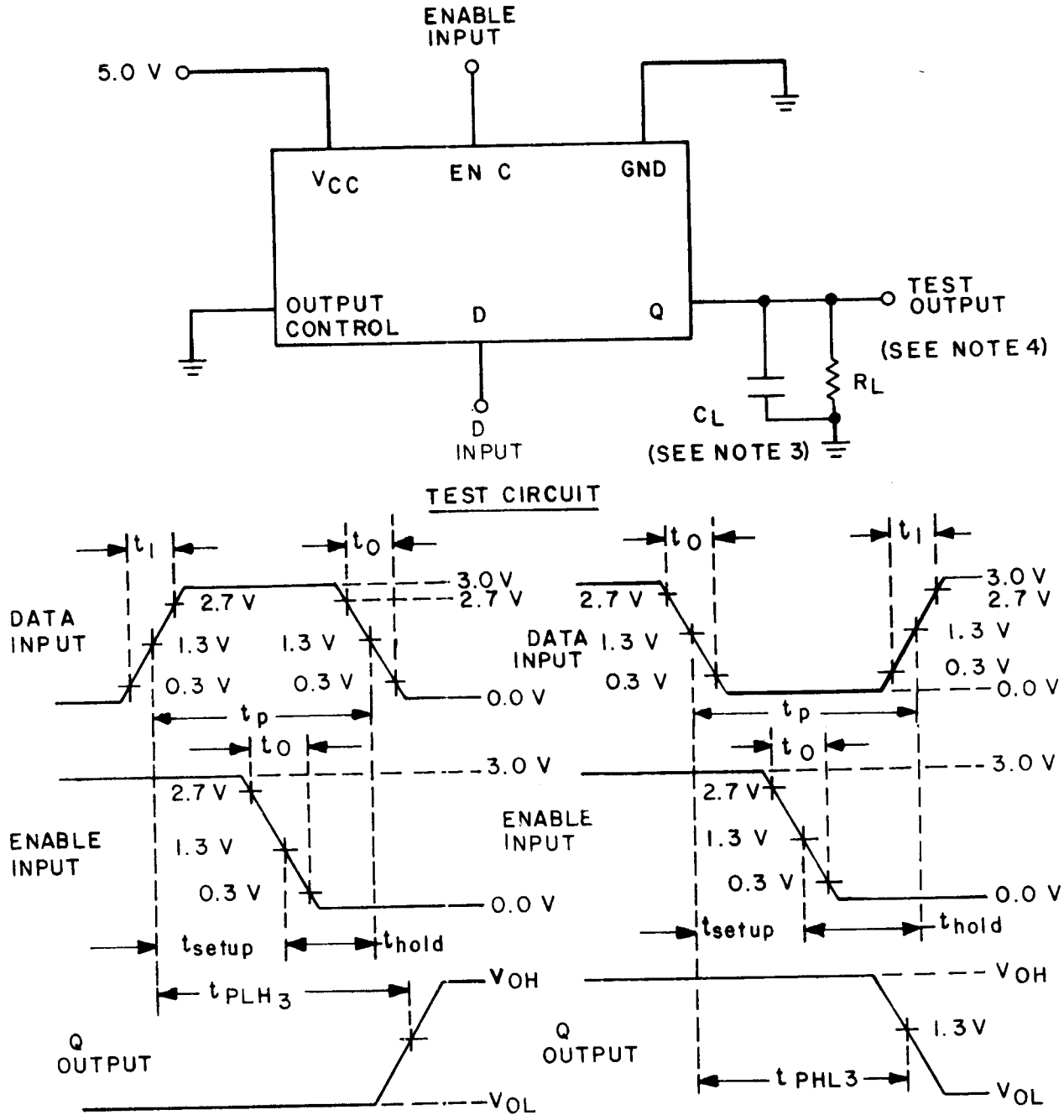
TEST CIRCUIT



VOLTAGE WAVEFORMS

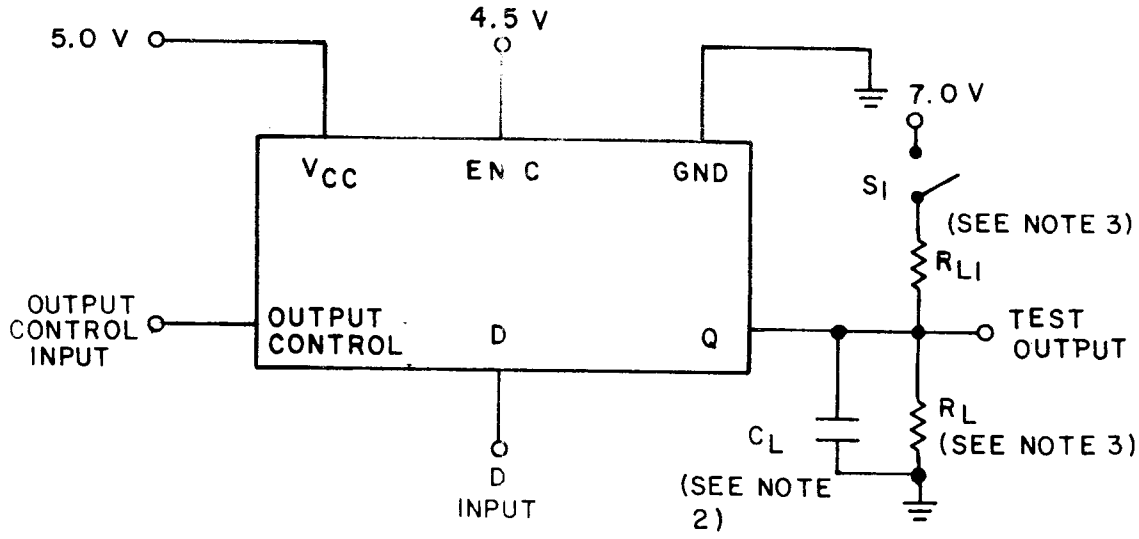
NOTES:
1. Enable input pulse characteristics: $t_1 = t_0 = 6 \pm 1.5$ ns; t_p (enable) = 10 ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. C_L = 50 pF ±10% (including jig and probe capacitance).
3. R_L = 499Ω ±1%.

FIGURE 5. Enable switching test circuit and waveforms (device type 01).

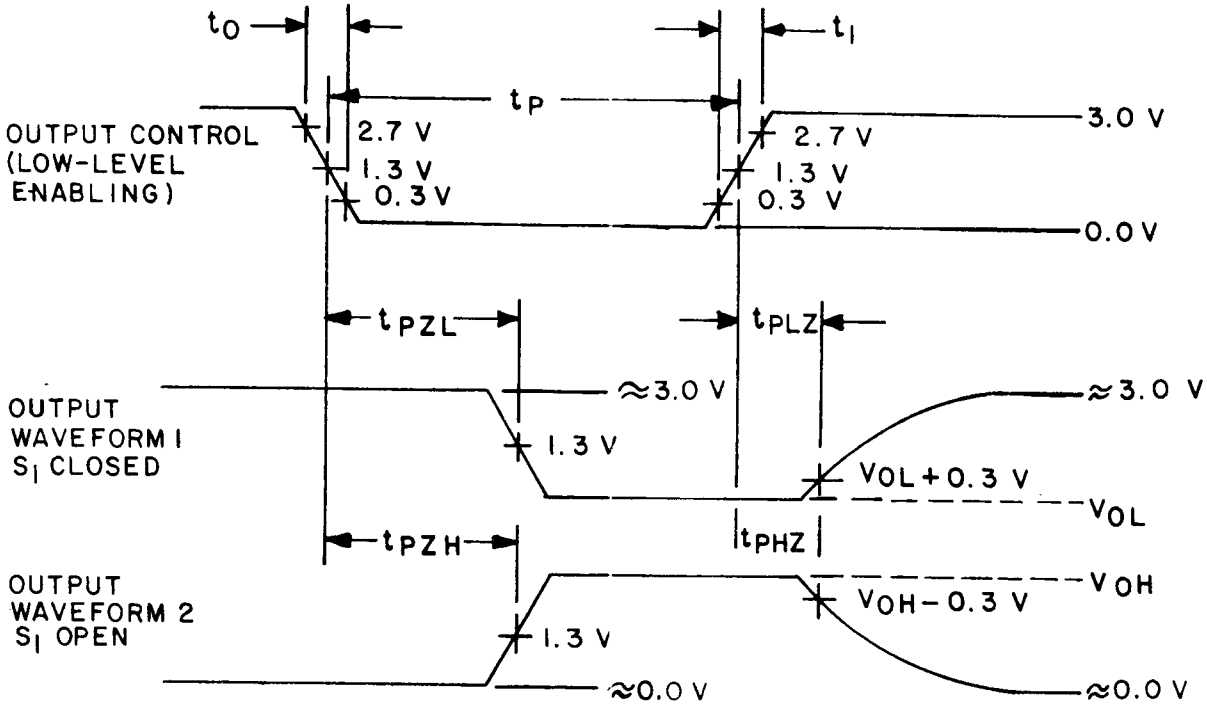


NOTES:
1. Enable input pulse characteristics: t_0 = 6 ±1.5 ns; PRR ≤ 1 MHz; Z_{OUT} ≅ 50Ω.
2. D input pulse characteristics: $t_1 = t_0$ = 6 ±1.5 ns; t_{setup} = 10 ns; t_{hold} = 7 ns; t_p = 17 ns; Z_{OUT} ≅ 50Ω.
3. C_L = 50 pF 10% (including jig and probe capacitance).
4. R_L = 499Ω ±1%.

FIGURE 5. Data switching test circuit and waveforms (device type 01).



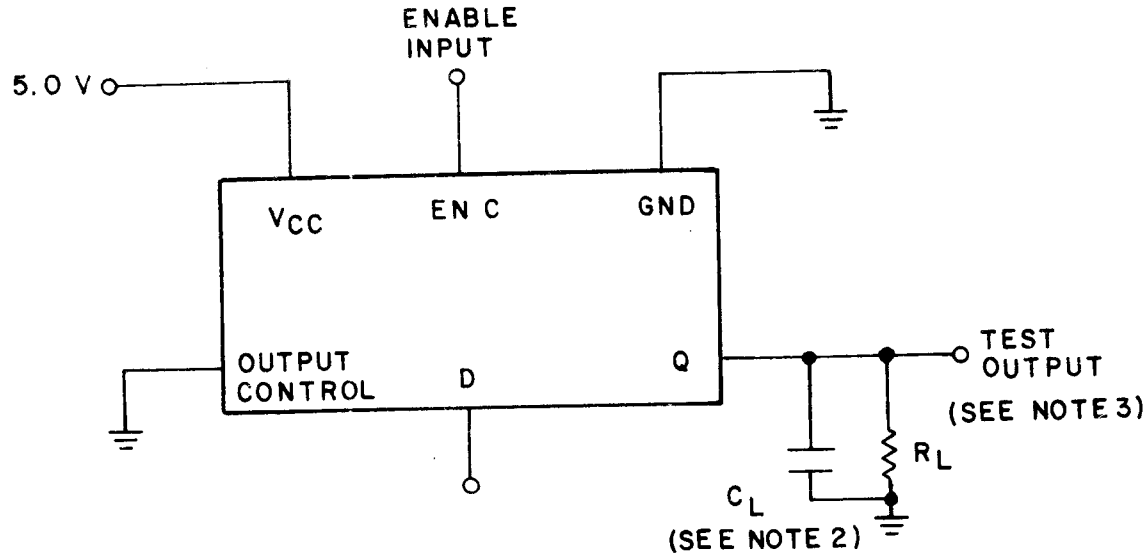
TEST CIRCUIT



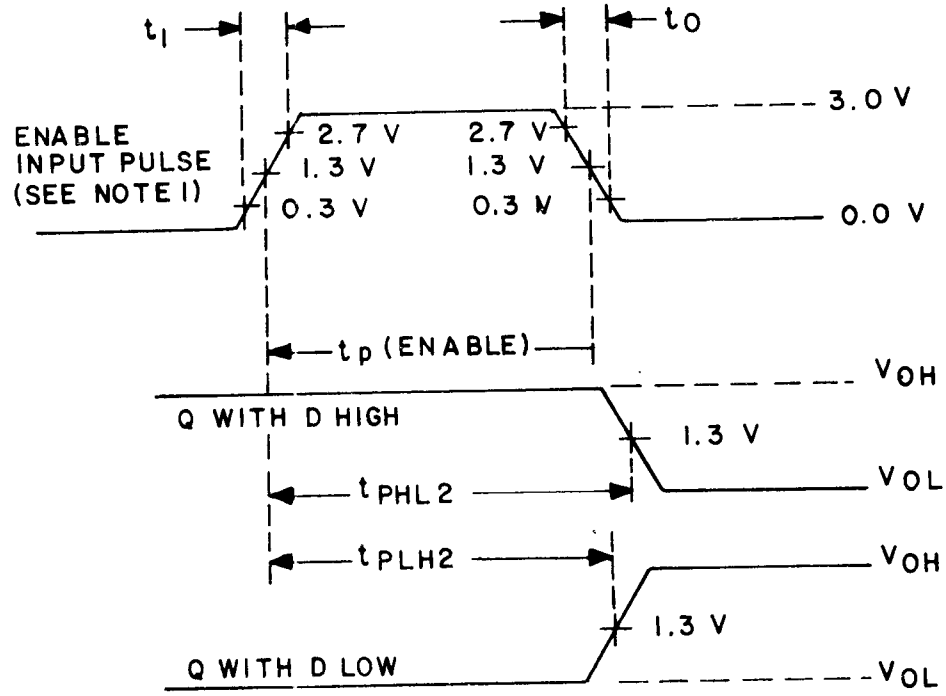
VOLTAGE WAVEFORMS

NOTES:
1. Output control input pulse characteristics: $t_0 = t_1 = 6 \pm 1.5$ ns; $t_p \geq 200$ ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. $C_L = 50$ pF ±10% (including jig and probe capacitance).
3. $R_L = R_{L_1} = 499\Omega$ ±1%.

FIGURE 5. Tri-state switching test circuit and waveforms for device type 01.



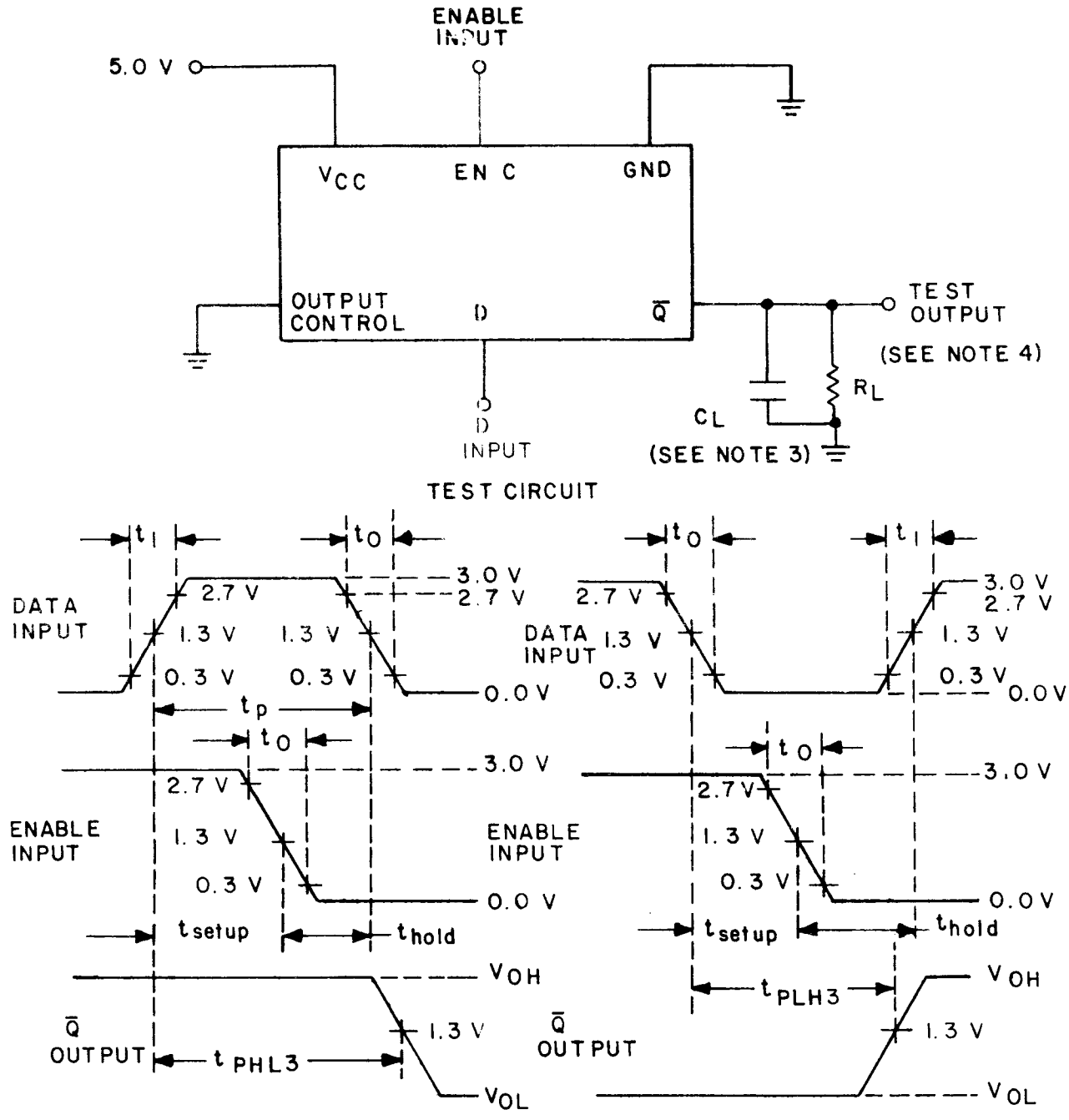
TEST CIRCUIT



VOLTAGE WAVEFORMS

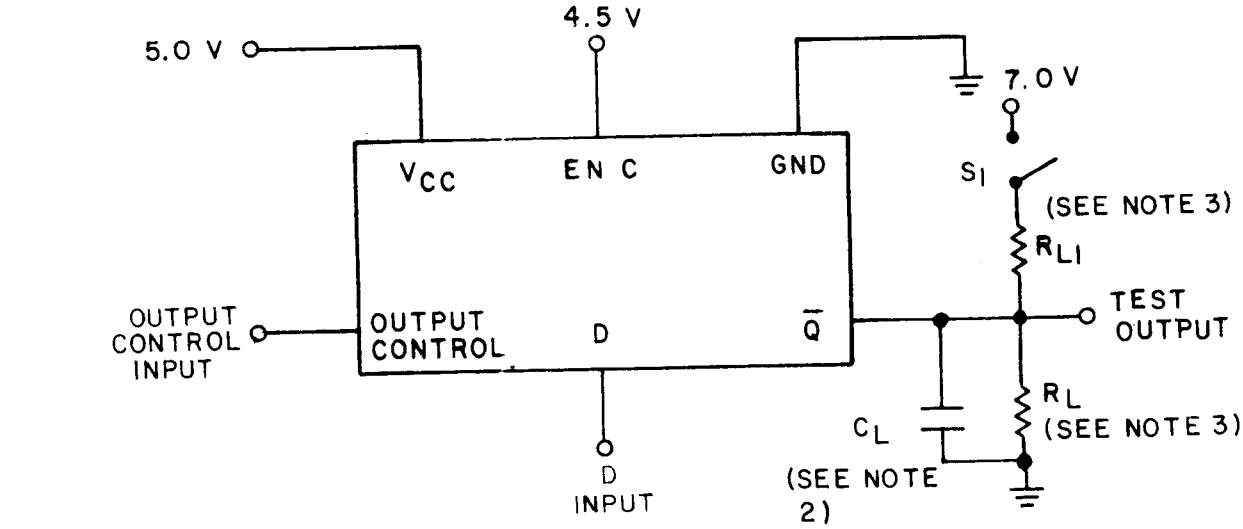
NOTES:
1. Enable input pulse characteristics: $t_1 = t_0 = 6 \pm 1.5$ ns; t_p (enable) = 15 ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. $C_L = 50$ pF ±10% (including jig and probe capacitance).
3. $R_L = 499\Omega \pm 1\%$.

FIGURE 5. Enable switching test circuit and waveforms (device type 02).

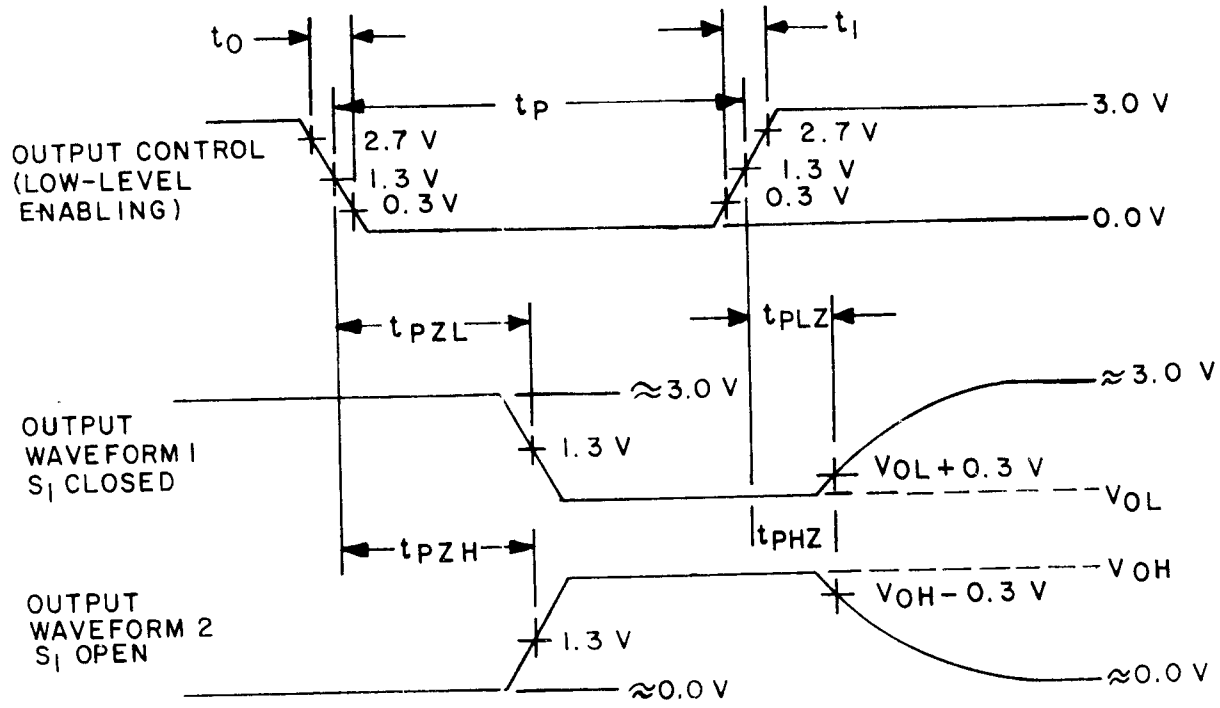


NOTES:
1. Enable input pulse characteristics: t_0 = 6 ±1.5 ns; t_p = 15 ns; PRR ≤ 1 MHz, Z_{OUT} ≅ 50Ω.
2. D input pulse characteristics: $t_1 = t_0$ = 6 ±1.5 ns; t_{setup} = 10 ns; t_{hold} = 10 ns; t_p 20 ns; PRR is 50% of enable PRR, Z_{OUT} ≅ 50Ω.
3. C_L = 50 pF ±10% (including jig and probe capacitance).
4. R_L = 499Ω ±1%.

FIGURE 5. Data switching test circuit and waveforms (device type 02).



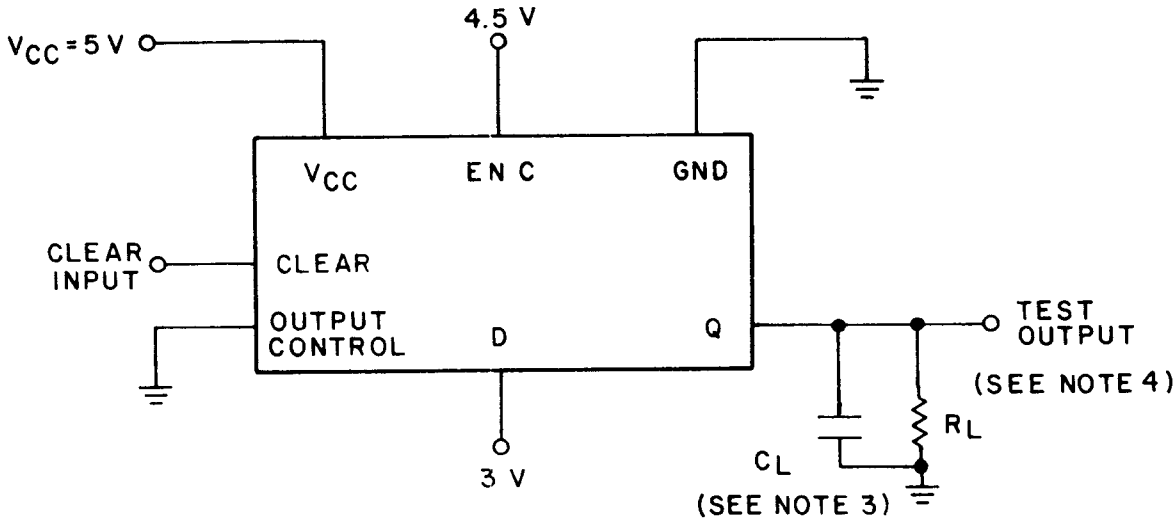
TEST CIRCUIT



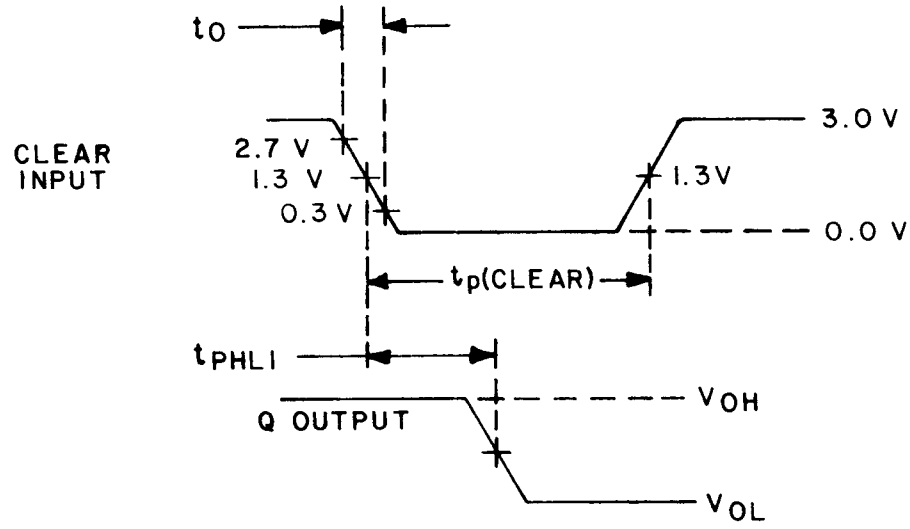
VOLTAGE WAVEFORMS

NOTES:
1. Output control input pulse characteristics: $t_0 = t_1 = 6 \pm 1.5$ ns; $t_p \geq 200$ ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. $C_L = 50$ pF ±10% (including jig and probe capacitance).
3. $R_L = R_{L_1} = 499\Omega \pm 1\%$.

FIGURE 5. Tri-state switching test circuit and waveforms for device type 02.



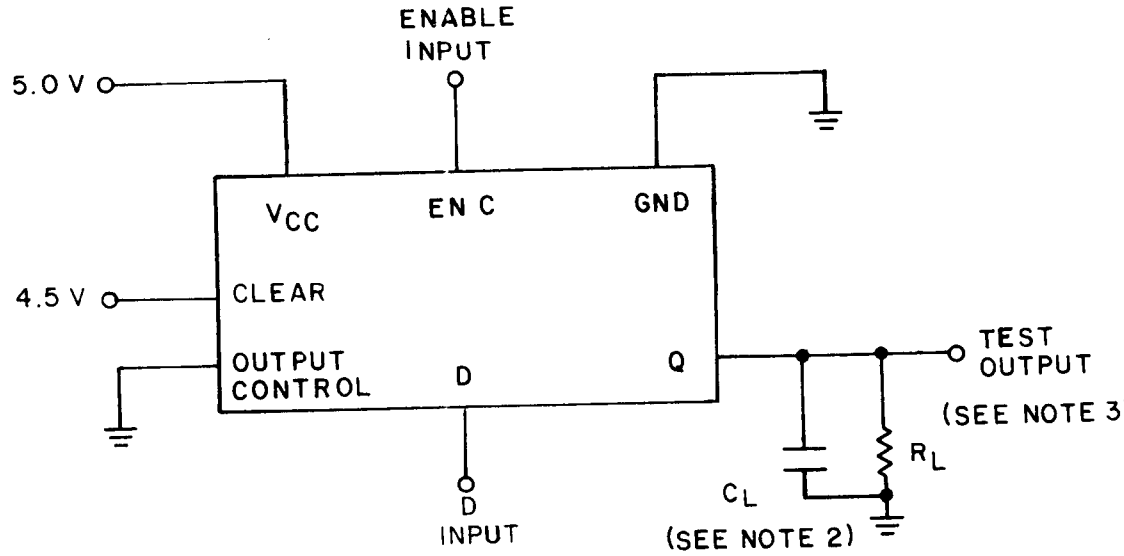
TEST CIRCUIT



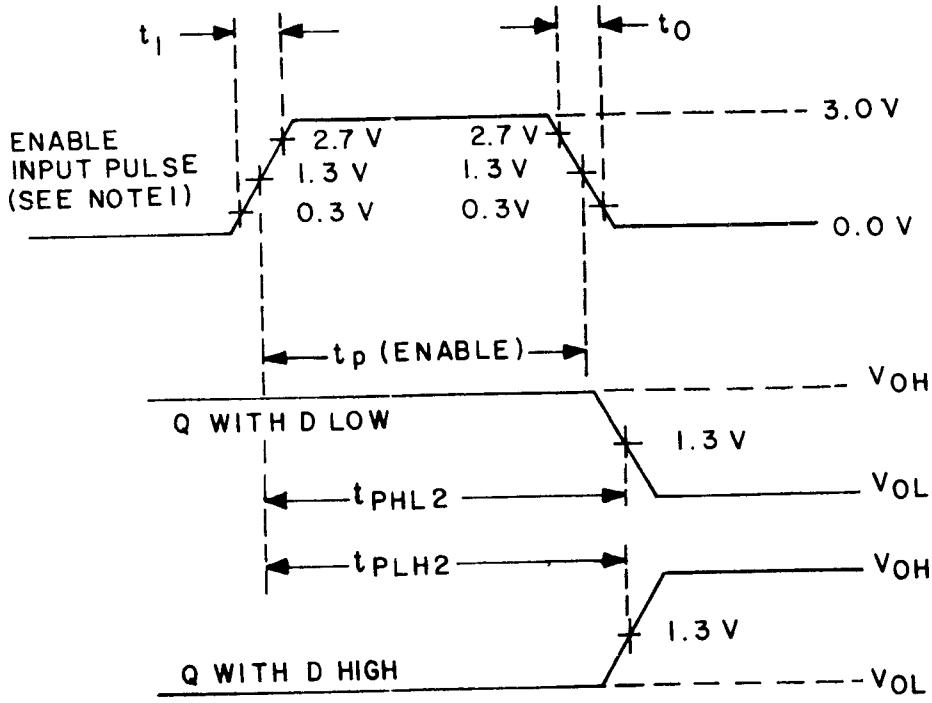
VOLTAGE WAVEFORM

NOTES:
1. Clear input dominates regardless of state of D input.
2. Clear input pulse characteristics: $t_1 = t_0 = 6 \pm 1.5$ ns; t_p (clear) = 15 ns; PRR $\leq$ 1 MHz, $Z_{OUT} \cong 50\Omega$.
3. C_L = 50 pF ±10% (including jig and probe capacitance).
4. R_L = 499Ω ±1%.

FIGURE 5. Clear switching test circuit and waveforms (device type 03).



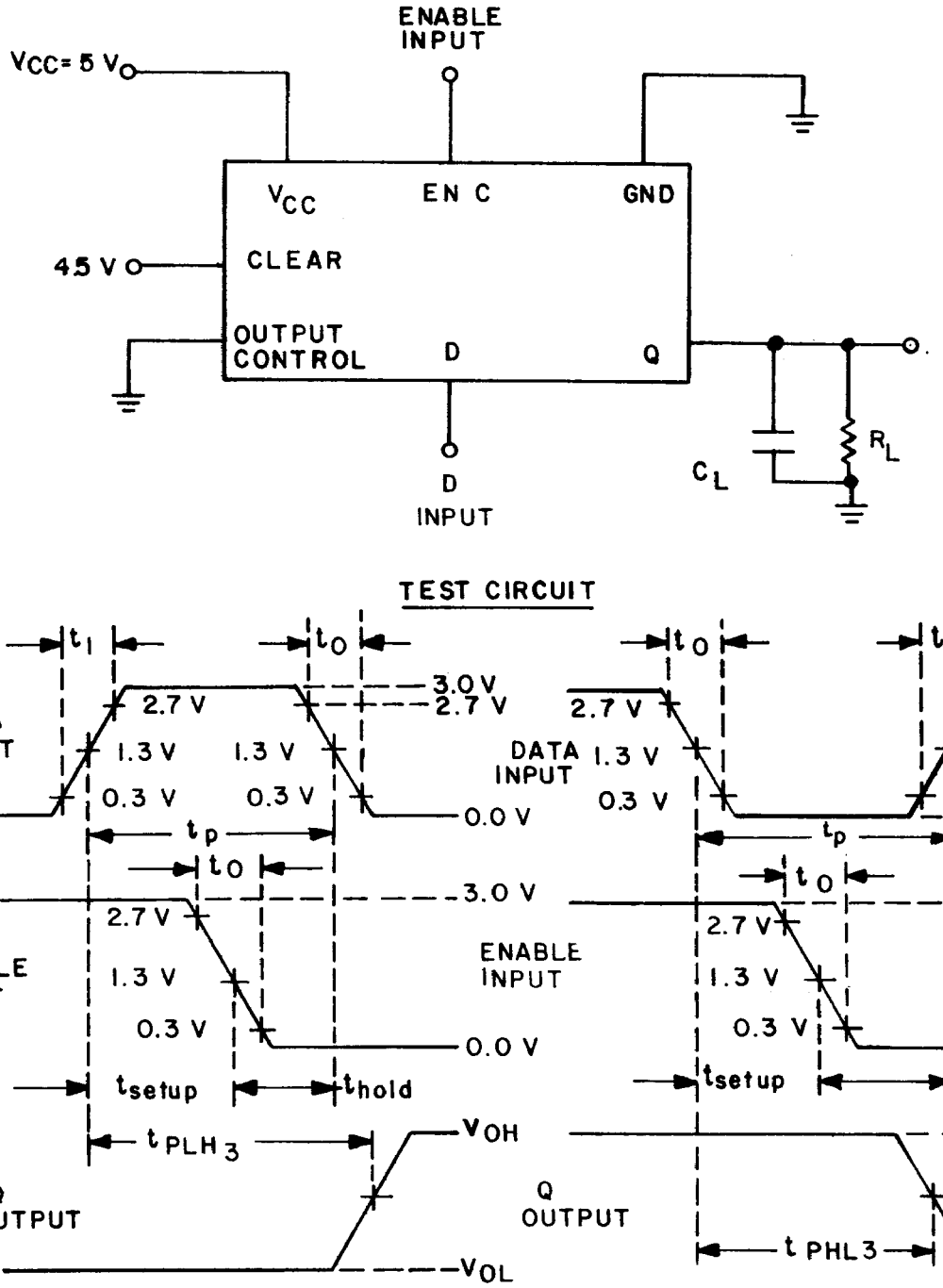
TEST CIRCUIT



VOLTAGE WAVEFORMS

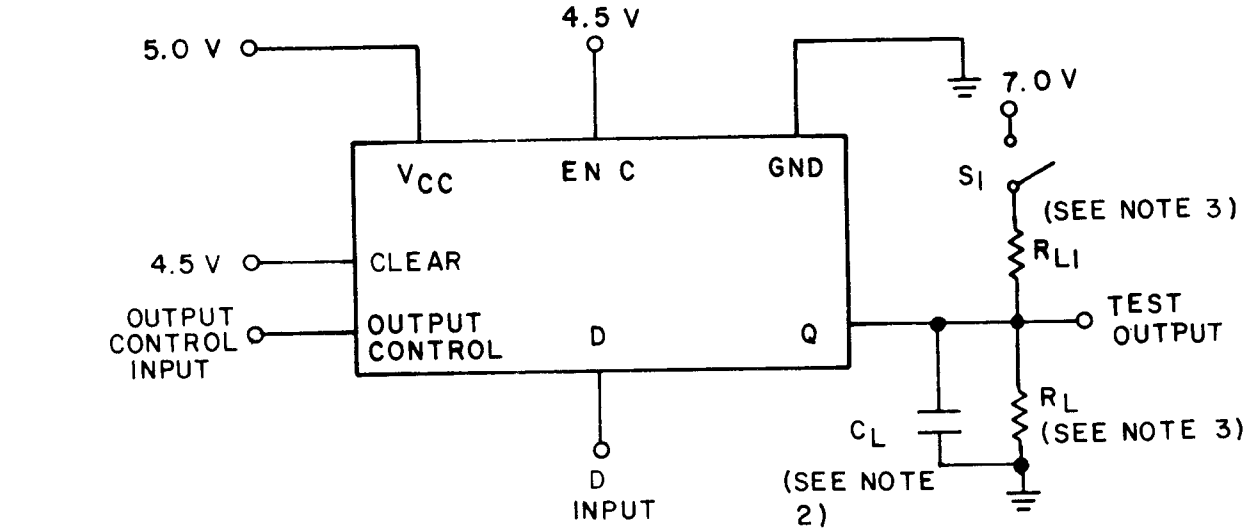
NOTES:
1. Enable input pulse characteristics: $t_1 = t_0 = 6 \pm 1.5$ ns; t_p (enable) = 10 ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. C_L = 50 pF ±10% (including jig and probe capacitance).
3. R_L = 499Ω ±1%.

FIGURE 5. Enable switching test circuit and waveforms (device type 03).

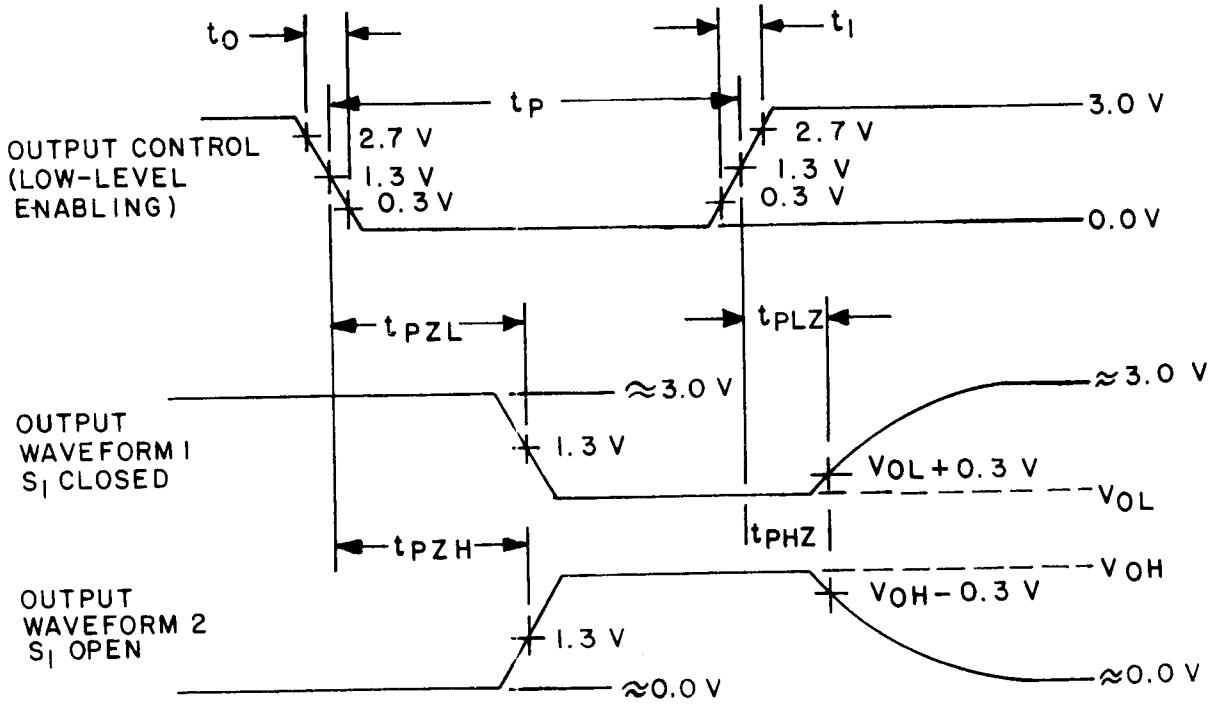


NOTES:
1. Enable input pulse characteristics: t_0 = 6 ±1.5 ns; t_p = 10 ns; PRR ≤ 1 MHz; $Z_{OUT} \cong$ 50Ω.
2. D input pulse characteristics: $t_1 = t_0$ = 6 ±1.5 ns; t_{setup} = 10 ns; t_{hold} = 7 ns; t_p = 17 ns; PRR is 50% of Enable PRR; $Z_{OUT} \cong$ 50Ω.
3. C_L = 50 pF ±10% (including jig and probe capacitance).
4. R_L = 499Ω ±1%.

FIGURE 5. Data switching test circuit and waveforms (device type 03).



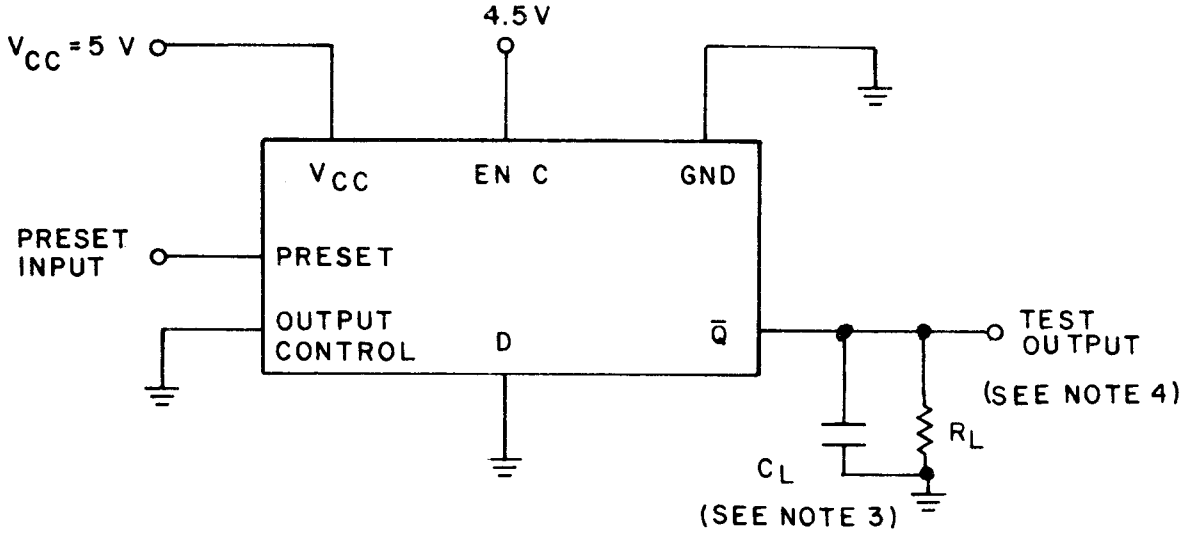
TEST CIRCUIT



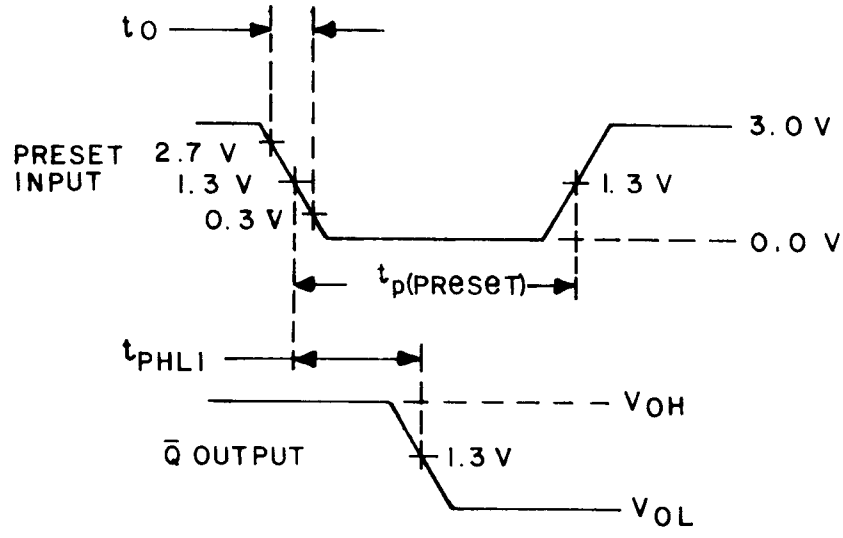
VOLTAGE WAVEFORMS

NOTES:
1. Output control input pulse characteristics: $t_0 = t_1 = 6 \pm 1.5$ ns; $t_p \geq 200$ ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. $C_L = 50$ pF ±10% (including jig and probe capacitance).
3. $R_L = R_{L_1} = 499\Omega \pm 1\%$.

FIGURE 5. Tri-state switching test circuit and waveforms for device type 03.



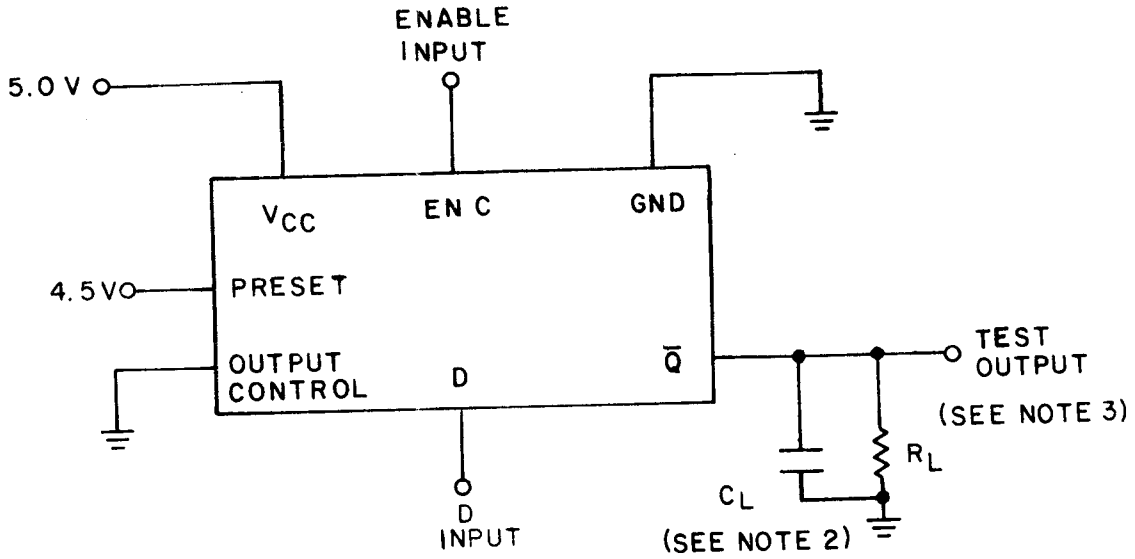
TEST CIRCUIT



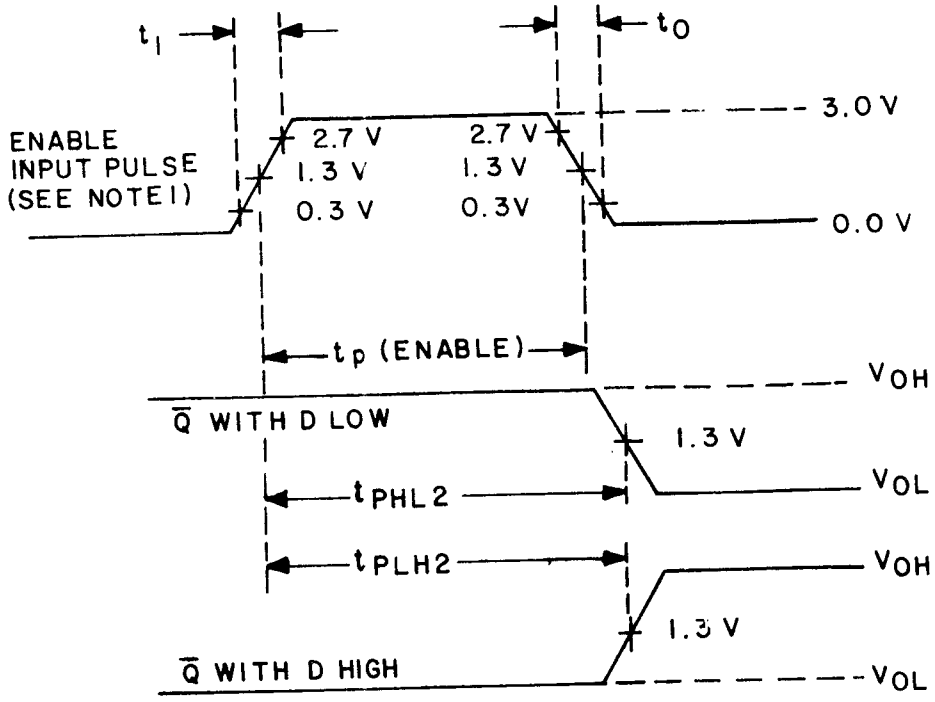
VOLTAGE WAVEFORM

NOTES:
1. Preset input dominates regardless of state of D input.
2. Preset input pulse characteristics: t_0 = 6 ±1.5 ns; t_p (preset) = 15 ns; PRR ≤ 1 MHz; $Z_{OUT} \approx 50\Omega$.
3. C_L = 50 pF ±10% (including jig and probe capacitance).
4. R_L = 499Ω ±1%.

FIGURE 5. Preset switching test circuit and waveforms for device type 04.



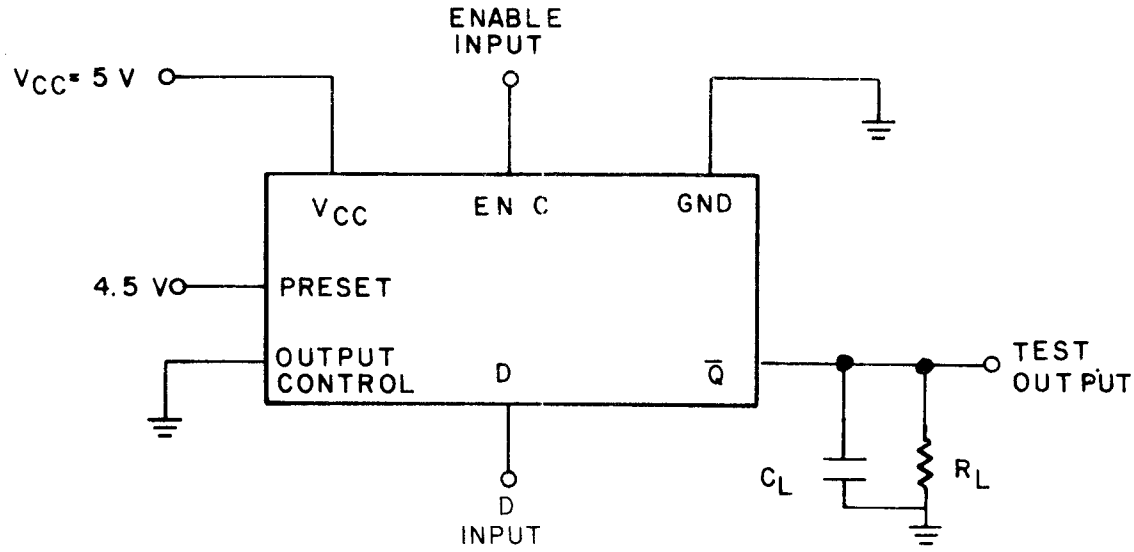
TEST CIRCUIT



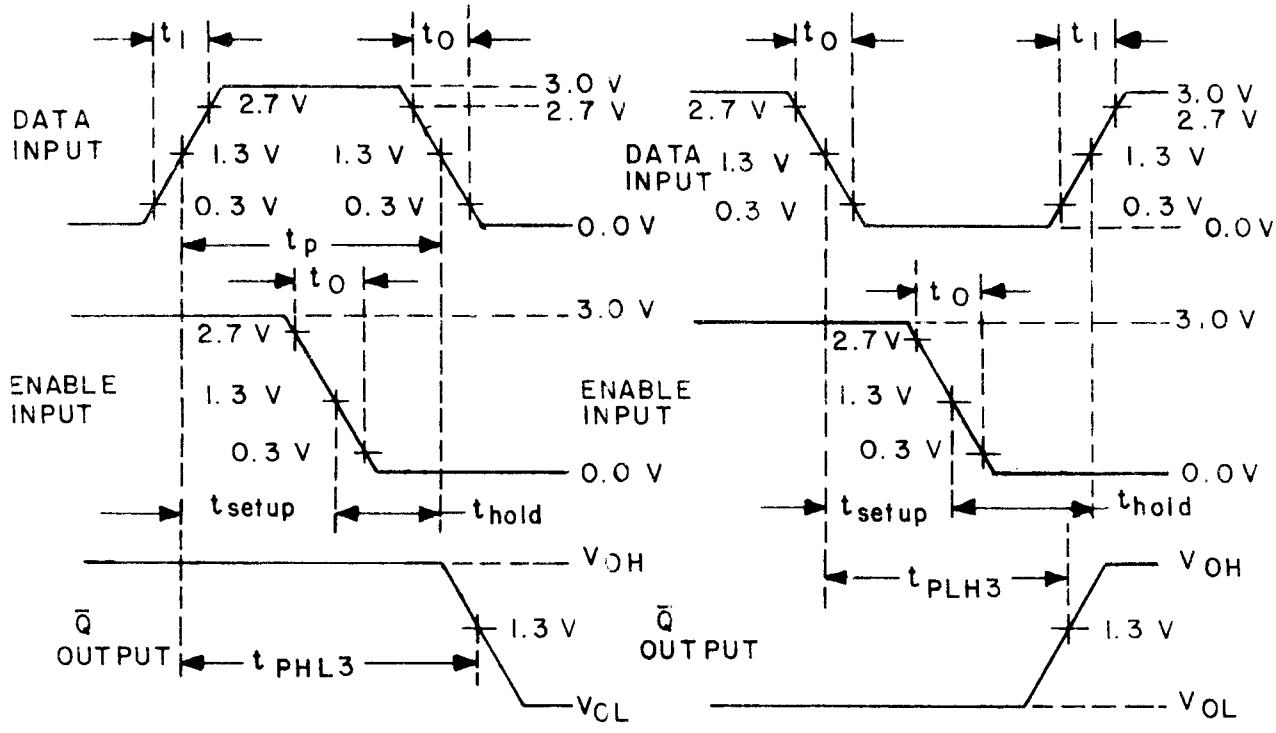
VOLTAGE WAVEFORMS

NOTES:
1. Enable input pulse characteristics: $t_1 = t_0 = 6 \pm 1.5$ ns; t_p (enable) = 15 ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. C_L = 50 pF ±10% (including jig and probe capacitance).
3. R_L = 499Ω ±1%.

FIGURE 5. Enable switching test circuit and waveforms (device type 04).



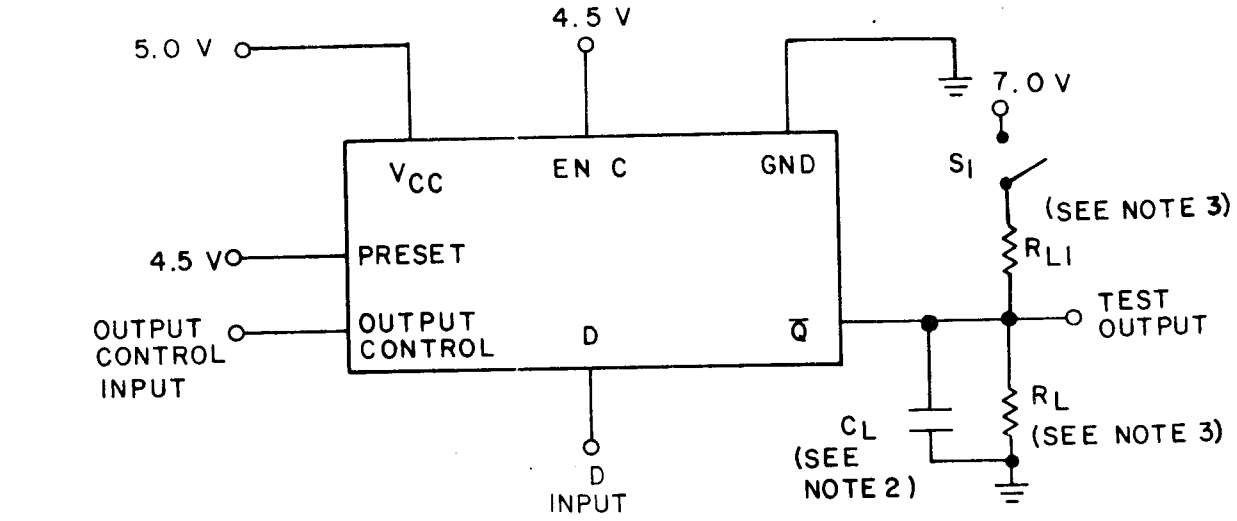
TEST CIRCUIT



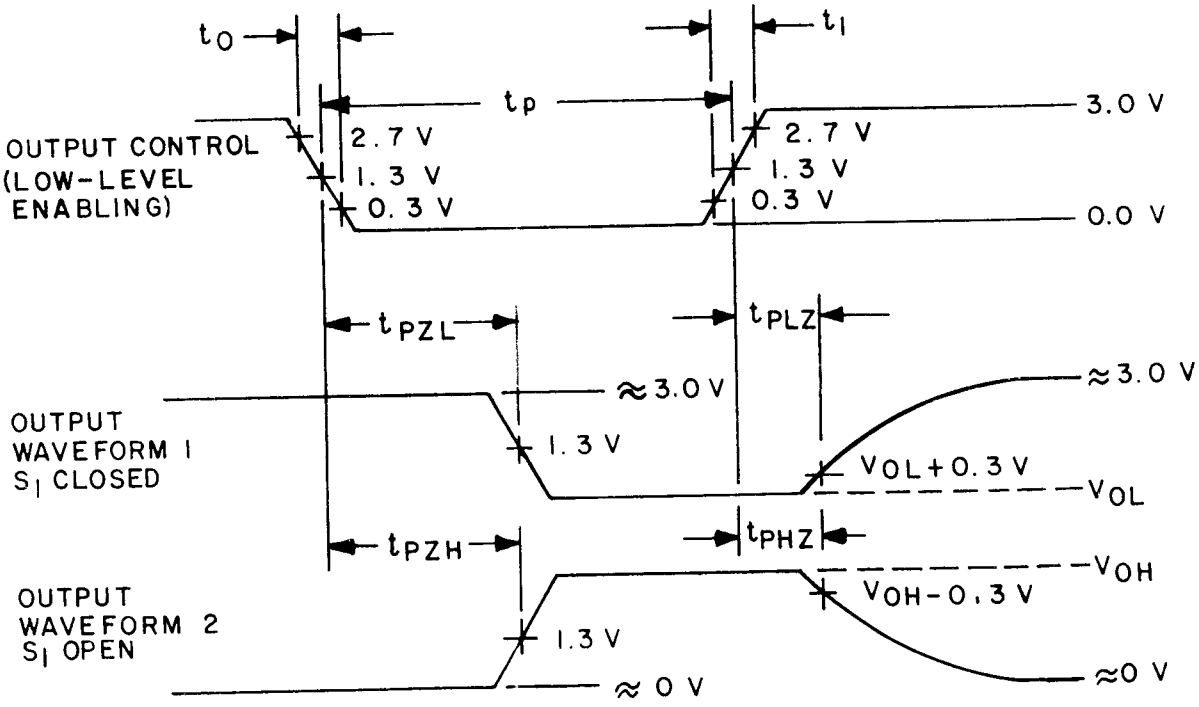
VOLTAGE WAVEFORMS

NOTES:
1. Enable input pulse characteristics: t_0 = 6 ±1.5 ns; t_p = 15 ns; PRR ≤ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. D input pulse characteristics: $t_1 = t_0$ = 6 ±1.5 ns; t_{setup} = 10 ns; t_{HOLD} = 10 ns; t_p = 20 ns; PRR is 50% of enable PRR, $Z_{OUT} \cong 50\Omega$.
3. C_L = 50 pF 10% (including jig and probe capacitance).
4. R_L = 499Ω ±1%.

FIGURE 5. Data switching test circuit and waveforms (device type 04).



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. Output control input pulse characteristics: $t_0 = t_1 = 6 \pm 1.5$ ns; $t_p \geq 200$ ns; PRR $\leq$ 1 MHz; $Z_{OUT} \cong 50\Omega$.
2. $C_L = 50$ pF ±10% (including jig and probe capacitance).
3. $R_L = R_{L_1} = 499\Omega \pm 1\%$.

FIGURE 5. Tri-state switching test circuit and waveforms for device type 04.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits Min	Test limits Max	Unit
				0C	1D	2D	3D	4D	5D	6D	7D	8D	GND	ENC	8Q	7Q	6Q	5Q	4Q	3Q	2Q	1Q	V_{CC}				
1 T_C=+25°C	V_{OH}	3006	1	0.8 V	2.0 V								GND	2.0 V								-1.0 mA	4.5 V	1Q	2.4		V
		"	2	"		2.0 V							"	"							-1.0 mA		"	2Q	"		"
		"	3	"			2.0 V						"	"						-1.0 mA			"	3Q	"		"
		"	4	"				2.0 V					"	"					-1.0 mA				"	4Q	"		"
		"	5	"					2.0 V				"	"				-1.0 mA					"	5Q	"		"
		"	6	"						2.0 V			"	"			-1.0 mA						"	6Q	"		"
		"	7	"							2.0 V		"	"		-1.0 mA							"	7Q	"		"
		"	8	"								2.0 V	"	"	-1.0 mA								"	8Q	"		"
	V_{OL}	3007	9	"	0.8 V								"	"								12 mA	"	1Q		0.4	"
		"	10	"		0.8 V							"	"							12 mA		"	2Q		"	"
		"	11	"			0.8 V						"	"						12 mA			"	3Q		"	"
		"	12	"				0.8 V					"	"				12 mA					"	4Q		"	"
		"	13	"					0.8 V				"	"			12 mA						"	5Q		"	"
		"	14	"						0.8 V			"	"									"	6Q		"	"
		"	15	"							0.8 V		"	"		12 mA							"	7Q		"	"
		"	16	"								0.8 V	"	"	12 mA								"	8Q		"	"
	V_{IC}		17	-18 mA									"										"	0C		-1.5	"
			18		-18 mA								"										"	1D		"	"
			19			-18 mA							"										"	2D		"	"
			20				-18 mA						"										"	3D		"	"
			21					-18 mA					"										"	4D		"	"
			22						-18 mA				"										"	5D		"	"
			23							-18 mA			"										"	6D		"	"
			24								-18 mA		"										"	7D		"	"
			25									-18 mA	"										"	8D		"	"
			26										"	-18 mA									"	ENC		"	"
	I_{IL}	3009	27	0.4 V									"										5.5 V	0C	1/	1/	µA
		"	28		0.4 V								"										"	1D	"	"	"
		"	29			0.4 V							"										"	2D	"	"	"
		"	30				0.4 V						"										"	3D	"	"	"
		"	31					0.4 V					"										"	4D	"	"	"
		"	32						0.4 V				"										"	5D	"	"	"
		"	33							0.4 V			"										"	6D	"	"	"
		"	34								0.4 V		"										"	7D	"	"	"
		"	35									0.4 V	"										"	8D	"	"	"
		"	36										"	0.4 V									"	ENC	"	"	"
	I_{IH1}	3010	37	2.7 V									"										"	0C		20	"
		"	38		2.7 V								"										"	1D		"	"
		"	39			2.7 V							"										"	2D		"	"
		"	40				2.7 V						"										"	3D		"	"
		"	41					2.7 V					"										"	4D		"	"
		"	42						2.7 V				"										"	5D		"	"
		"	43							2.7 V			"										"	6D		"	"
		"	44								2.7 V		"										"	7D		"	"
		"	45									2.7 V	"										"	8D		"	"
		"	46										"	2.7 V									"	ENC		"	"
	I_{IH2}	"	47	7.0 V									"										"	0C		100	"
		"	48		7.0 V								"										"	1D		"	"
		"	49			7.0 V							"										"	2D		"	"
		"	50				7.0 V						"										"	3D		"	"
		"	51					7.0 V					"										"	4D		"	"
		"	52						7.0 V				"										"	5D		"	"
		"	53							7.0 V			"										"	6D		"	"
		"	54								7.0 V		"										"	7D		"	"
		"	55									7.0 V	"										"	8D		"	"
		"	56										"	7.0 V									"	ENC		"	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits Min	Test limits Max	Unit
				OC	1D	2D	3D	4D	5D	6D	7D	8D	GND	ENC	8Q	7Q	6Q	5Q	4Q	3Q	2Q	1Q	V_{CC}				
1 T_C=+25°C	I_O	3011	57	GND	5.0 V								GND	5.0 V									5.5 V	1Q	3/ -15	-70	mA
		2/	58	"		5.0 V							"	"				2.25 V				2.25 V	"	2Q	"	"	"
		"	59	"			5.0 V						"	"					2.25 V		2.25 V		"	3Q	"	"	"
		"	60	"				5.0 V					"	"			2.25 V						"	4Q	"	"	"
		"	61	"					5.0 V				"	"		2.25 V							"	5Q	"	"	"
		"	62	"						5.0 V			"	"	2.25 V								"	6Q	"	"	"
		"	63	"							5.0 V		"	"									"	7Q	"	"	"
		"	64	"								5.0 V	"	"									"	8Q	"	"	"
	I_{OZH}		65	5.0 V	2.0 V								"	"									"	1Q		20	µA
			66	"		2.0 V							"	"									"	2Q		"	"
			67	"			2.0 V						"	"									"	3Q		"	"
			68	"				2.0 V					"	"									"	4Q		"	"
			69	"					2.0 V				"	"									"	5Q		"	"
			70	"						2.0 V			"	"									"	6Q		"	"
			71	"							2.0 V		"	"									"	7Q		"	"
			72	"								2.0 V	"	"									"	8Q		"	"
	I_{OZL}		73	5.0 V	0.8 V								"	"									"	1Q		-20	"
			74	"		0.8 V							"	"									"	2Q		"	"
			75	"			0.8 V						"	"									"	3Q		"	"
			76	"				0.8 V					"	"									"	4Q		"	"
			77	"					0.8 V				"	"									"	5Q		"	"
			78	"						0.8 V			"	"									"	6Q		"	"
			79	"							0.8 V		"	"									"	7Q		"	"
			80	"								0.8 V	"	"									"	8Q		"	"
	I_{CCH}	3005	81	GND	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	"	"									"	V_{CC}		19	mA
	I_{CCL}	"	82	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	"									"	V_{CC}		24	"
	I_{CCZ}	"	83	5.0 V	GND	GND	GND	GND	GND	GND	GND	GND	"	"									"	V_{CC}		27	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																										
7 4/ T_C=+25°C	Truth table tests	3014	84	B	B	B	B	B	B	B	B	B	GND	A	L	L	L	L	L	L	L	L	5.0 V	All outputs	5/	5/	
		"	85	"	A	B	A	A	A	A	A	A	"	"	H	L	L	L	L	L	L	L	"	"	"	"	
		"	86	"	B	A	B	A	B	B	B	B	"	B	L	H	L	L	L	L	L	L	"	"	"	"	
		"	87	"	B	B	A	B	A	B	B	B	"	B	H	H	L	L	L	L	L	L	"	"	"	"	
		"	88	"	A	A	A	A	B	A	B	B	"	A	L	L	H	L	L	L	L	L	"	"	"	"	
		"	89	"	"	"	"	"	"	B	A	B	"	B	H	H	H	L	L	L	L	L	"	"	"	"	
		"	90	"	"	"	"	"	"	"	"	A	"	A	L	L	L	H	L	L	L	L	"	"	"	"	
		"	91	"	B	B	B	B	B	B	B	B	"	B	H	H	H	H	H	L	L	L	"	"	"	"	
		"	92	"	B	B	B	B	B	B	B	B	"	A	L	L	L	L	L	L	L	L	"	"	"	"	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																										
9 T_C=+25°C	t_{PLH2}	3003 Fig. 5	93	GND	4.5 V								"	IN									5.0 V	ENC to 1Q	8	20	ns
		"	94	"		4.5 V							"	"									"	ENC to 2Q	"	"	"
		"	95	"			4.5 V						"	"									"	ENC to 3Q	"	"	"
		"	96	"				4.5 V					"	"									"	ENC to 4Q	"	"	"
		"	97	"					4.5 V				"	"									"	ENC to 5Q	"	"	"
		"	98	"						4.5 V			"	"									"	ENC to 6Q	"	"	"
		"	99	"							4.5 V		"	"									"	ENC to 7Q	"	"	"
		"	100	"								4.5 V	"	"									"	ENC to 8Q	"	"	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits Min	Test limits Max	Unit
				0C	1D	2D	3D	4D	5D	6D	7D	8D	GND	ENC	8Q	7Q	6Q	5Q	4Q	3Q	2Q	1Q	V_{CC}				
T_C=+25°C	t_{PHL2}	3003 Fig. 5	101	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN									5.0 V	ENC to 1Q	6	19	ns
			102	"									"	"									"	ENC to 2Q	"	"	"
			103	"									"	"						OUT			"	ENC to 3Q	"	"	"
			104	"									"	"					OUT				"	ENC to 4Q	"	"	"
			105	"									"	"				OUT					"	ENC to 5Q	"	"	"
			106	"									"	"			OUT						"	ENC to 6Q	"	"	"
			107	"									"	"		OUT							"	ENC to 7Q	"	"	"
			108	"									"	"	OUT								"	ENC to 8Q	"	"	"
	t_{PLH3}	"	109	"	IN	IN	IN	IN	IN	IN	IN	IN	"	"								OUT	"	1D to 1Q	2	14	"
			110	"									"	"							OUT		"	2D to 2Q	"	"	"
			111	"									"	"						OUT			"	3D to 3Q	"	"	"
			112	"									"	"					OUT				"	4D to 4Q	"	"	"
			113	"									"	"				OUT					"	5D to 5Q	"	"	"
			114	"									"	"			OUT						"	6D to 6Q	"	"	"
			115	"									"	"		OUT							"	7D to 7Q	"	"	"
			116	"									"	"	OUT								"	8D to 8Q	"	"	"
	t_{PHL3}	"	117	"	IN	IN	IN	IN	IN	IN	IN	IN	"	"								OUT	"	1D to 1Q	"	"	"
			118	"									"	"							OUT		"	2D to 2Q	"	"	"
			119	"									"	"						OUT			"	3D to 3Q	"	"	"
			120	"									"	"					OUT				"	4D to 4Q	"	"	"
			121	"									"	"				OUT					"	5D to 5Q	"	"	"
			122	"									"	"			OUT						"	6D to 6Q	"	"	"
			123	"									"	"		OUT							"	7D to 7Q	"	"	"
			124	"									"	"	OUT								"	8D to 8Q	"	"	"
	t_{PZH}	"	125	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	4.5 V								OUT	"	$\overline{0C}$ to 1Q	4	18	"
			126	"									"	"							OUT		"	$\overline{0C}$ to 2Q	"	"	"
			127	"									"	"						OUT			"	$\overline{0C}$ to 3Q	"	"	"
			128	"									"	"					OUT				"	$\overline{0C}$ to 4Q	"	"	"
			129	"									"	"				OUT					"	$\overline{0C}$ to 5Q	"	"	"
			130	"									"	"			OUT						"	$\overline{0C}$ to 6Q	"	"	"
			131	"									"	"		OUT							"	$\overline{0C}$ to 7Q	"	"	"
			132	"									"	"	OUT								"	$\overline{0C}$ to 8Q	"	"	"
	t_{PZL}	"	133	"	GND	GND	GND	GND	GND	GND	GND	GND	"	"								OUT	"	$\overline{0C}$ to 1Q	"	"	"
			134	"									"	"							OUT		"	$\overline{0C}$ to 2Q	"	"	"
			135	"									"	"						OUT			"	$\overline{0C}$ to 3Q	"	"	"
			136	"									"	"					OUT				"	$\overline{0C}$ to 4Q	"	"	"
			137	"									"	"				OUT					"	$\overline{0C}$ to 5Q	"	"	"
			138	"									"	"			OUT						"	$\overline{0C}$ to 6Q	"	"	"
			139	"									"	"		OUT							"	$\overline{0C}$ to 7Q	"	"	"
			140	"									"	"	OUT								"	$\overline{0C}$ to 8Q	"	"	"
	t_{PHZ}	"	141	"	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	"								OUT	"	$\overline{0C}$ to 1Q	2	10	"
			142	"									"	"							OUT		"	$\overline{0C}$ to 2Q	"	"	"
			143	"									"	"						OUT			"	$\overline{0C}$ to 3Q	"	"	"
			144	"									"	"					OUT				"	$\overline{0C}$ to 4Q	"	"	"
			145	"									"	"				OUT					"	$\overline{0C}$ to 5Q	"	"	"
			146	"									"	"			OUT						"	$\overline{0C}$ to 6Q	"	"	"
			147	"									"	"		OUT							"	$\overline{0C}$ to 7Q	"	"	"
			148	"									"	"	OUT								"	$\overline{0C}$ to 8Q	"	"	"
	t_{PLZ}	"	149	"	GND	GND	GND	GND	GND	GND	GND	GND	"	"								OUT	"	$\overline{0C}$ to 1Q	2	15	"
			150	"									"	"							OUT		"	$\overline{0C}$ to 2Q	"	"	"
			151	"									"	"						OUT			"	$\overline{0C}$ to 3Q	"	"	"
			152	"									"	"					OUT				"	$\overline{0C}$ to 4Q	"	"	"
			153	"									"	"				OUT					"	$\overline{0C}$ to 5Q	"	"	"
			154	"									"	"			OUT						"	$\overline{0C}$ to 6Q	"	"	"
			155	"									"	"		OUT							"	$\overline{0C}$ to 7Q	"	"	"
			156	"									"	"	OUT								"	$\overline{0C}$ to 8Q	"	"	"

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1 0C	2 1D	3 2D	4 3D	5 4D	6 5D	7 6D	8 7D	9 8D	10 GND	11 ENC	12 8Q	13 7Q	14 6Q	15 5Q	16 4Q	17 3Q	18 2Q	19 1Q	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
10 T_C=+125°C	t_{PLH2}	Same tests and terminal conditions as for subgroup 9, except T_C = +125°C.																							8	27	ns
	t_{PHL2}																								4	20	"
	t_{PLH3}																								2	15	"
	t_{PHL3}																								2	15	"
	t_{PZH}																								4	21	"
	t_{PZL}																								4	21	"
	t_{PHZ}																								2	12	"
	t_{PLZ}																								2	18	"
11 T_C=-55°C	Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C.																										

1/ I_{IL} limits shall be as follows:

Test	Limits in µA for circuit A	B	C
I_{IL}	0/-200	0/-100	0/-200

2/ Method 3011 shall be used, except the output voltage shall be as specified herein, and the output current shall be operating rather than short-circuit current. The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current I_{OS}.

3/ I_O limits shall be as follows:

Test	Limits in mA for circuit A	B	C
I_O	-30/-112	-15/-110	-70/-110

4/ Tests shall be performed in sequence, attributes data only.

5/ Outputs shall be high ≥1.5 V, low ≤1.5 V.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1 $\overline{OC}$	2 1D	3 2D	4 3D	5 4D	6 5D	7 6D	8 7D	9 8D	10 GND	11 ENC	12 $8\overline{Q}$	13 $7\overline{Q}$	14 $6\overline{Q}$	15 $5\overline{Q}$	16 $4\overline{Q}$	17 $3\overline{Q}$	18 $2\overline{Q}$	19 $1\overline{Q}$	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C=+25°C	V_{OH}	3006	1	0.8 V	0.8 V								GND	2.0 V								-1.0 mA	4.5 V	$1\overline{Q}$	2.4		V
	"	"	2	"		0.8 V							"	"							-1.0 mA		"	$2\overline{Q}$	"		"
	"	"	3	"			0.8 V						"	"						-1.0 mA			"	$3\overline{Q}$	"		"
	"	"	4	"				0.8 V					"	"					-1.0 mA				"	$4\overline{Q}$	"		"
	"	"	5	"					0.8 V				"	"				-1.0 mA					"	$5\overline{Q}$	"		"
	"	"	6	"						0.8 V			"	"			-1.0 mA						"	$6\overline{Q}$	"		"
	"	"	7	"							0.8 V		"	"		-1.0 mA							"	$7\overline{Q}$	"		"
	"	"	8	"								0.8 V	"	"	-1.0 mA								"	$8\overline{Q}$	"		"
	V_{OL}	3007	9	"	2.0 V								"	"								12 mA	"	$1\overline{Q}$		0.4	"
	"	"	10	"		2.0 V							"	"							12 mA		"	$2\overline{Q}$		"	"
	"	"	11	"			2.0 V						"	"						12 mA			"	$3\overline{Q}$		"	"
	"	"	12	"				2.0 V					"	"					12 mA				"	$4\overline{Q}$		"	"
	"	"	13	"					2.0 V				"	"				12 mA					"	$5\overline{Q}$		"	"
	"	"	14	"						2.0 V			"	"			12 mA						"	$6\overline{Q}$		"	"
	"	"	15	"							2.0 V		"	"		12 mA							"	$7\overline{Q}$		"	"
	"	"	16	"								2.0 V	"	"	12 mA								"	$8\overline{Q}$		"	"
	V_{IC}		17	-18 mA									"										"	$\overline{OC}$		-1.5	"
			18		-18 mA								"										"	1D		"	"
			19			-18 mA							"										"	2D		"	"
			20				-18 mA						"										"	3D		"	"
			21					-18 mA					"										"	4D		"	"
			22						-18 mA				"										"	5D		"	"
			23							-18 mA			"										"	6D		"	"
			24								-18 mA		"										"	7D		"	"
			25									-18 mA	"										"	8D		"	"
			26										"	-18 mA									"	ENC		"	"
	I_{IL}	3009	27	0.4 V									"										5.5 V	$\overline{OC}$	1/	1/	μA
	"	"	28		0.4 V								"										"	1D	"	"	"
	"	"	29			0.4 V							"										"	2D	"	"	"
	"	"	30				0.4 V						"										"	3D	"	"	"
	"	"	31					0.4 V					"										"	4D	"	"	"
	"	"	32						0.4 V				"										"	5D	"	"	"
	"	"	33							0.4 V			"										"	6D	"	"	"
	"	"	34								0.4 V		"										"	7D	"	"	"
	"	"	35									0.4 V	"										"	8D	"	"	"
	"	"	36										"	0.4 V									"	ENC	"	"	"
	I_{IH1}	3010	37	2.7 V									"										"	$\overline{OC}$		20	"
	"	"	38		2.7 V								"										"	1D		"	"
	"	"	39			2.7 V							"										"	2D		"	"
	"	"	40				2.7 V						"										"	3D		"	"
	"	"	41					2.7 V					"										"	4D		"	"
	"	"	42						2.7 V				"										"	5D		"	"
	"	"	43							2.7 V			"										"	6D		"	"
	"	"	44								2.7 V		"										"	7D		"	"
	"	"	45									2.7 V	"										"	8D		"	"
	"	"	46										"	2.7 V									"	ENC		"	"
	I_{IH2}	"	47	7.0 V									"										"	$\overline{OC}$		100	"
	"	"	48		7.0 V								"										"	1D		"	"
	"	"	49			7.0 V							"										"	2D		"	"
	"	"	50				7.0 V						"										"	3D		"	"
	"	"	51					7.0 V					"										"	4D		"	"
	"	"	52						7.0 V				"										"	5D		"	"
	"	"	53							7.0 V			"										"	6D		"	"
	"	"	54								7.0 V		"										"	7D		"	"
	"	"	55									7.0 V	"										"	8D		"	"
	"	"	56										"	7.0 V									"	ENC		"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1 $\overline{0C}$	2 1D	3 2D	4 3D	5 4D	6 5D	7 6D	8 7D	9 8D	10 GND	11 ENC	12 8$\overline{Q}$	13 7$\overline{Q}$	14 6$\overline{Q}$	15 5$\overline{Q}$	16 4$\overline{Q}$	17 3$\overline{Q}$	18 2$\overline{Q}$	19 1$\overline{Q}$	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C=+25°C	I_O 2/	3011	57	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.0 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	5.5 V	1$\overline{Q}$	3/ -15	3/ -70	mA
		"	58	"									"	"									"	2$\overline{Q}$	"	"	"
		"	59	"									"	"									"	3$\overline{Q}$	"	"	"
		"	60	"									"	"									"	4$\overline{Q}$	"	"	"
		"	61	"									"	"									"	5$\overline{Q}$	"	"	"
		"	62	"									"	"									"	6$\overline{Q}$	"	"	"
		"	63	"									"	"									"	7$\overline{Q}$	"	"	"
		"	64	"									"	"									"	8$\overline{Q}$	"	"	"
	I_{OZH}		65	5.0 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	"	"	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	"	1$\overline{Q}$		20	µA
			66	"									"	"									"	2$\overline{Q}$		"	"
			67	"									"	"									"	3$\overline{Q}$		"	"
			68	"									"	"									"	4$\overline{Q}$		"	"
			69	"									"	"									"	5$\overline{Q}$		"	"
			70	"									"	"									"	6$\overline{Q}$		"	"
			71	"									"	"									"	7$\overline{Q}$		"	"
			72	"									"	"									"	8$\overline{Q}$		"	"
	I_{OZL}		73	"	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	"	"	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	"	1$\overline{Q}$		-20	"
			74	"									"	"									"	2$\overline{Q}$		"	"
			75	"									"	"									"	3$\overline{Q}$		"	"
			76	"									"	"									"	4$\overline{Q}$		"	"
			77	"									"	"									"	5$\overline{Q}$		"	"
			78	"									"	"									"	6$\overline{Q}$		"	"
			79	"									"	"									"	7$\overline{Q}$		"	"
			80	"									"	"									"	8$\overline{Q}$		"	"
	I_{CCH}	3005	81	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	"									"	V_{CC}		17	mA
	I_{CCL}	"	82	GND	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	"	"									"	V_{CC}		24	mA
	I_{CCZ}	"	83	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	"	"									"	V_{CC}		27	mA
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																										
7 4/ T_C=+25°C	Truth table tests	3014	84	B	A	A	A	A	A	A	A	A	GND	A	L	L	L	L	L	L	L	L	5.0 V	All outputs	5/	5/	
		"	85	"	B	A	A	A	A	A	A	A	"	"	H	L	L	L	L	L	L	L	"	"	"	"	
		"	86	"	A	B	A	A	A	A	A	A	"	B	L	H	L	L	L	L	L	L	"	"	"	"	
		"	87	"	A	A	B	A	A	A	A	A	"	B	H	H	L	L	L	L	L	L	"	"	"	"	
		"	88	"	B	A	B	A	A	A	A	A	"	A	L	L	H	L	L	L	L	L	"	"	"	"	
		"	89	"	A	B	B	A	A	A	A	A	"	A	H	H	H	L	L	L	L	L	"	"	"	"	
		"	90	"	B	B	B	A	A	A	A	A	"	B	L	L	L	H	L	L	L	L	"	"	"	"	
		"	91	"	A	A	A	B	A	A	A	A	"	B	H	H	H	H	L	L	L	L	"	"	"	"	
		"	92	"	A	A	A	A	B	A	A	A	"	A	L	L	L	L	H	L	L	L	"	"	"	"	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																										
9 T_C=+25°C	t_{PLH2}	3003 Fig. 5	93	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	IN									5.0 V	ENC to 1$\overline{Q}$	8	22	µs
		"	94	"									"	"									"	ENC to 2$\overline{Q}$	"	"	"
		"	95	"									"	"									"	ENC to 3$\overline{Q}$	"	"	"
		"	96	"									"	"									"	ENC to 4$\overline{Q}$	"	"	"
		"	97	"									"	"									"	ENC to 5$\overline{Q}$	"	"	"
		"	98	"									"	"									"	ENC to 6$\overline{Q}$	"	"	"
		"	99	"									"	"									"	ENC to 7$\overline{Q}$	"	"	"
		"	100	"									"	"									"	ENC to 8$\overline{Q}$	"	"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits Min	Test limits Max	Unit
				$\overline{OC}$	1D	2D	3D	4D	5D	6D	7D	8D	GND	ENC	8$\overline{Q}$	7$\overline{Q}$	6$\overline{Q}$	5$\overline{Q}$	4$\overline{Q}$	3$\overline{Q}$	2$\overline{Q}$	1$\overline{Q}$	V_{CC}				
5 T_C=+25°C	t_{PHL2}	3003 Fig. 5	101	GND	4.5 V								GND	IN								OUT	5.0 V	ENC to 1$\overline{Q}$	8	21	ns
		"	102	"		4.5 V							"	"							OUT		"	ENC to 2$\overline{Q}$	"	"	"
		"	103	"			4.5 V						"	"						OUT			"	ENC to 3$\overline{Q}$	"	"	"
		"	104	"				4.5 V					"	"					OUT				"	ENC to 4$\overline{Q}$	"	"	"
		"	105	"					4.5 V				"	"				OUT					"	ENC to 5$\overline{Q}$	"	"	"
		"	106	"						4.5 V			"	"			OUT						"	ENC to 6$\overline{Q}$	"	"	"
		"	107	"							4.5 V		"	"		OUT							"	ENC to 7$\overline{Q}$	"	"	"
		"	108	"								4.5 V	"	"	OUT								"	ENC to 8$\overline{Q}$	"	"	"
	t_{PLH3}	"	109	"	IN								"	"								OUT	"	1D to 1$\overline{Q}$	3	18	"
		"	110	"		IN							"	"							OUT		"	2D to 2$\overline{Q}$	"	"	"
		"	111	"			IN						"	"						OUT			"	3D to 3$\overline{Q}$	"	"	"
		"	112	"				IN					"	"					OUT				"	4D to 4$\overline{Q}$	"	"	"
		"	113	"					IN				"	"				OUT					"	5D to 5$\overline{Q}$	"	"	"
		"	114	"						IN			"	"			OUT						"	6D to 6$\overline{Q}$	"	"	"
		"	115	"							IN		"	"		OUT							"	7D to 7$\overline{Q}$	"	"	"
		"	116	"								IN	"	"	OUT								"	8D to 8$\overline{Q}$	"	"	"
	t_{PHL3}	"	117	"	IN								"	"								OUT	"	1D to 1$\overline{Q}$	"	12	"
		"	118	"		IN							"	"							OUT		"	2D to 2$\overline{Q}$	"	"	"
		"	119	"			IN						"	"						OUT			"	3D to 3$\overline{Q}$	"	"	"
		"	120	"				IN					"	"					OUT				"	4D to 4$\overline{Q}$	"	"	"
		"	121	"					IN				"	"				OUT					"	5D to 5$\overline{Q}$	"	"	"
		"	122	"						IN			"	"			OUT						"	6D to 6$\overline{Q}$	"	"	"
		"	123	"							IN		"	"		OUT							"	7D to 7$\overline{Q}$	"	"	"
		"	124	"								IN	"	"	OUT								"	8D to 8$\overline{Q}$	"	"	"
	t_{PZH}	"	125	IN	GND								"	4.5 V								OUT	"	$\overline{OC}$ to 1$\overline{Q}$	4	18	"
		"	126	"		GND							"	"							OUT		"	$\overline{OC}$ to 2$\overline{Q}$	"	"	"
		"	127	"			GND						"	"						OUT			"	$\overline{OC}$ to 3$\overline{Q}$	"	"	"
		"	128	"				GND					"	"					OUT				"	$\overline{OC}$ to 4$\overline{Q}$	"	"	"
		"	129	"					GND				"	"				OUT					"	$\overline{OC}$ to 5$\overline{Q}$	"	"	"
		"	130	"						GND			"	"			OUT						"	$\overline{OC}$ to 6$\overline{Q}$	"	"	"
		"	131	"							GND		"	"		OUT							"	$\overline{OC}$ to 7$\overline{Q}$	"	"	"
		"	132	"								GND	"	"	OUT								"	$\overline{OC}$ to 8$\overline{Q}$	"	"	"
	t_{PZL}	"	133	"	4.5 V								"	"								OUT	"	$\overline{OC}$ to 1$\overline{Q}$	"	"	"
		"	134	"		4.5 V							"	"							OUT		"	$\overline{OC}$ to 2$\overline{Q}$	"	"	"
		"	135	"			4.5 V						"	"						OUT			"	$\overline{OC}$ to 3$\overline{Q}$	"	"	"
		"	136	"				4.5 V					"	"					OUT				"	$\overline{OC}$ to 4$\overline{Q}$	"	"	"
		"	137	"					4.5 V				"	"				OUT					"	$\overline{OC}$ to 5$\overline{Q}$	"	"	"
		"	138	"						4.5 V			"	"			OUT						"	$\overline{OC}$ to 6$\overline{Q}$	"	"	"
		"	139	"							4.5 V		"	"		OUT							"	$\overline{OC}$ to 7$\overline{Q}$	"	"	"
		"	140	"								4.5 V	"	"	OUT								"	$\overline{OC}$ to 8$\overline{Q}$	"	"	"
	t_{PHZ}	"	141	"	GND								"	"								OUT	"	$\overline{OC}$ to 1$\overline{Q}$	2	18	"
		"	142	"		GND							"	"							OUT		"	$\overline{OC}$ to 2$\overline{Q}$	"	"	"
		"	143	"			GND						"	"						OUT			"	$\overline{OC}$ to 3$\overline{Q}$	"	"	"
		"	144	"				GND					"	"					OUT				"	$\overline{OC}$ to 4$\overline{Q}$	"	"	"
		"	145	"					GND				"	"				OUT					"	$\overline{OC}$ to 5$\overline{Q}$	"	"	"
		"	146	"						GND			"	"			OUT						"	$\overline{OC}$ to 6$\overline{Q}$	"	"	"
		"	147	"							GND		"	"		OUT							"	$\overline{OC}$ to 7$\overline{Q}$	"	"	"
		"	148	"								GND	"	"	OUT								"	$\overline{OC}$ to 8$\overline{Q}$	"	"	"

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases R,S,2 Test no.	1 $\overline{0C}$	2 1D	3 2D	4 3D	5 4D	6 5D	7 6D	8 7D	9 8D	10 GND	11 ENC	12 $8\overline{Q}$	13 $7\overline{Q}$	14 $6\overline{Q}$	15 $5\overline{Q}$	16 $4\overline{Q}$	17 $3\overline{Q}$	18 $2\overline{Q}$	19 $1\overline{Q}$	20 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
9 T_C=+25°C	t_{PLZ}	3003 Fig. 5	149	IN	4.5 V	4.5 V							GND	4.5 V							OUT	OUT	5.0 V	0C to 1Q	3	13	ns
		"	150	"			4.5 V						"	"									"	0C to 2Q	"	"	"
		"	151	"				4.5 V					"	"									"	0C to 3Q	"	"	"
		"	152	"					4.5 V				"	"					OUT				"	0C to 4Q	"	"	"
		"	153	"						4.5 V			"	"				OUT					"	0C to 5Q	"	"	"
		"	154	"							4.5 V		"	"			OUT						"	0C to 6Q	"	"	"
		"	155	"								4.5 V	"	"		OUT							"	0C to 7Q	"	"	"
		"	156	"									"	"	OUT								"	0C to 8Q	"	"	"
10 T_C=+125°C	t_{PLH2}	Same tests and terminal conditions as for subgroup 9, except T_C = +125°C.																							8	29	"
	t_{PHL2}																								8	22	"
	t_{PLH3}																								3	21	"
	t_{PHL3}																								3	15	"
	t_{PZH}																								4	21	"
	t_{PZL}																								4	21	"
	t_{PHZ}																								2	10	"
	t_{PLZ}																								3	15	"
11 T_C=-55°C	Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C.																										

1/ I_{IL} limits shall be as follows:

Test	Limits in µA for circuit A	B	C
I_{IL}	0/-100	0/-100	0/-200

2/ Method 3011 shall be used, except the output voltage shall be as specified herein, and the output current shall be operating rather than short-circuit current. The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current I_{OS}.

3/ I_O limits for circuit C shall be -70 to -110 mA

4/ Tests shall be performed in sequence, attributes data only.

5/ Outputs shall be high ≥1.5 V, low ≤1.5 V.

TABLE III. Group A inspection for device type 03.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28	Measured terminal	Limits		Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	
			Test no.	$\overline{1CLR}$	$\overline{1OC}$	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	$\overline{2OC}$	GND	$\overline{2CLR}$	EN2C	2Q4	2Q3	2Q2	2Q1	1Q4	1Q3	1Q2	1Q1	EN1C	V_{CC}				
1 T_C = +25°C	V_{OH}	3006	1	2.0 V	0.8 V	2.0 V																					4.5 V	1Q1	2.4		V
			2	"	"		2.0 V																	-1.0 mA	-1.0 mA	2.0 V	"	1Q2	"		"
			3	"	"			2.0 V															-1.0 mA			"	"	1Q3	"		"
			4						2.0 V													-1.0 mA					"	1Q4	"		"
			5							2.0 V											-1.0 mA						"	2Q1	"		"
			6								2.0 V									-1.0 mA							"	2Q2	"		"
			7									2.0 V							-1.0 mA								"	2Q3	"		"
			8										2.0 V					-1.0 mA									"	2Q4	"		"
														0.8 V		2.0 V	2.0 V														
														"		"	"														
														"		"	"														
														"		"	"														
														"		"	"														
														"		"	"														
														"		"	"														
														"	GND	"	"														
	V_{OL}	3007	9	2.0 V	0.8 V	0.8 V																					4.5 V	1Q1		0.4	V
			10	"	"		0.8 V																	12 mA	12 mA	2.0 V	"	1Q2		"	"
			11	"	"			0.8 V															12 mA			"	"	1Q3		"	"
			12						0.8 V												12 mA						"	1Q4		"	"
			13							0.8 V				0.8 V		2.0 V	2.0 V										"	2Q1		"	"
			14								0.8 V			"		"	"			12 mA							"	2Q2		"	"
			15									0.8 V		"		"	"		12 mA								"	2Q3		"	"
			16										0.8 V	"		"	"											"	2Q4		"	"
			17	0.8 V	0.8 V													12 mA							12 mA	2.0 V	"	1Q1		"	"
			18	"	"																			12 mA		"	"	1Q2		"	"
			19	"	"																						"	1Q3		"	"
			20	"	"																						"	1Q4		"	"
			21											0.8 V		0.8 V	2.0 V										"	2Q1		"	"
			22											"		"	"										"	2Q2		"	"
			23											"		"	"										"	2Q3		"	"
			24											"		"	"										"	2Q4		"	"
	V_{IC}		25	-18 mA	-18 mA																						"	$\overline{1CLR}$		-1.5	"
			26			-18 mA																					"	$\overline{1OC}$		"	"
			27				-18 mA																				"	1D1		"	"
			28					-18 mA																			"	1D2		"	"
			29						-18 mA																		"	1D3		"	"
			30							-18 mA																	"	1D4		"	"
			31								-18 mA																"	2D1		"	"
			32									-18 mA															"	2D2		"	"
			33										-18 mA														"	2D3		"	"
			34											-18 mA													"	2D4		"	"
			35													-18 mA											"	$\overline{2OC}$		"	"
			36														-18 mA										"	$\overline{2CLR}$		"	"
			37																								"	EN2C		"	"
			38																							-18 mA	"	EN1C		"	"
	I_{IL}	3009	39	0.4 V																							5.5 V	$\overline{1CLR}$	2/	2/	μA
			40		0.4 V																						"	$\overline{1OC}$	"	"	"
			41			0.4 V																					"	1D1	"	"	"
			42				0.4 V																				"	1D2	"	"	"
			43					0.4 V																			"	1D3	"	"	"
			44						0.4 V																		"	1D4	"	"	"
			45							0.4 V																	"	2D1	"	"	"
			46								0.4 V																"	2D2	"	"	"
			47									0.4 V															"	2D3	"	"	"
			48										0.4 V														"	2D4	"	"	"
			49											0.4 V													"	$\overline{2OC}$	"	"	"
			50													0.4 V											"	$\overline{2CLR}$	"	"	"
			51														0.4 V										"	EN2C	"	"	"
			52																							0.4 V	"	EN1C	"	"	"

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28	Measured terminal	Limits		Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	15	14	15	16	17	18	19	20	21	22	23	24		Min	Max	
			Test no.	$\overline{1CLR}$	$\overline{1OC}$	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	$\overline{2OC}$	GND	2CLR	EN2C	2Q4	2Q3	2Q2	2Q1	1Q4	1Q3	1Q2	1Q1	EN1C	V_{CC}				
T_C = +25°C 1/	I_{IH1}	3010	53	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	GND	2.7 V	2.7 V									2.7 V	5.5 V	$\overline{1CLR}$		20	µA
			54												"												"	$\overline{1OC}$		"	
			55												"												"	1D1		"	
			56												"												"	1D2		"	
			57												"												"	1D3		"	
			58												"												"	1D4		"	
			59												"												"	2D1		"	
			60												"												"	2D2		"	
			61												"												"	2D3		"	
			62												"												"	2D4		"	
			63												"												"	$\overline{2OC}$		"	
			64												"												"	$\overline{2CLR}$		"	
			65												"												"	EN2C		"	
			66												"												"	EN1C		"	
	I_{IH2}	"	67	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	"	7.0 V	7.0 V									7.0 V	"	$\overline{1CLR}$		100	"
			68												"												"	$\overline{1OC}$		"	
			69												"												"	1D1		"	
			70												"												"	1D2		"	
			71												"												"	1D3		"	
			72												"												"	1D4		"	
			73												"												"	2D1		"	
			74												"												"	2D2		"	
			75												"												"	2D3		"	
			76												"												"	2D4		"	
			77												"												"	$\overline{2OC}$		"	
			78												"												"	$\overline{2CLR}$		"	
			79												"												"	EN2C		"	
			80												"												"	EN1C		"	
	I_D	3011 3/	81	5.0 V	GND	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	GND	"	5.0 V	5.0 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	5.0 V	"	1Q1	4/ -15	4/ -70	mA
			82	"	"										"	"	"										"	1Q2	"	"	
			83												"												"	1Q3		"	
			84												"												"	1Q4		"	
			85												"												"	2Q1		"	
			86												"												"	2Q2		"	
			87												"												"	2Q3		"	
			88												"												"	2Q4		"	
	I_{OZH}		89	5.0 V	5.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	5.0 V	"	5.0 V	5.0 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	5.0 V	"	1Q1		20	µA
			90	"	"										"	"	"										"	1Q2		"	
			91												"												"	1Q3		"	
			92												"												"	1Q4		"	
			93												"												"	2Q1		"	
			94												"												"	2Q2		"	
			95												"												"	2Q3		"	
			96												"												"	2Q4		"	
	I_{OZL}		97	5.0 V	5.0 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	5.0 V	"	5.0 V	5.0 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	2/	"	1Q1		-20	"
			98	"	"										"	"	"										"	1Q2		"	
			99												"												"	1Q3		"	
			100												"												"	1Q4		"	
			101												"												"	2Q1		"	
			102												"												"	2Q2		"	
			103												"												"	2Q3		"	
			104												"												"	2Q4		"	

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not destynated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/ Cases K,L Test no.	2 1 1CLR	3 2 1CC	4 3 1D1	5 4 1D2	6 5 1D3	7 6 1D4	9 7 2D1	10 8 2D2	11 9 2D3	12 10 2D4	13 11 2CC	14 12 GND	16 13 2CLR	17 14 EN2C	18 15 2Q4	19 16 2Q3	20 17 2Q2	21 18 2Q1	23 19 1Q4	24 20 1Q3	25 21 1Q2	26 22 1Q1	27 23 EN1C	28 24 V_{CC}	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	I_{CCH}	3005	105	5.0 V	GND	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	GND	GND	5.0 V	5.0 V									5.0 V	5.0 V	V_{CC}		21	mA
	I_{CCL}	"	106	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	"	GND	"									"	"	V_{CC}		25	"
	I_{CC2}	"	107	"	5.0 V	"	"	"	"	"	"	"	"	5.0 V	"	GND	"									"	"	V_{CC}		31	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																													
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																													
7 5/ T_C = +25°C	Truth table tests	3014	108	A	B	A	A	A	A	A	A	A	A	B	GND	A	H	H	H	H	H	H	H	H	H	A	5.0 V	All outputs	6/	6/	
	"	"	109	"	"	B	B	B	B	B	B	B	B	"	"	"	L	L	L	L	L	L	L	L	L	"	"	"	"	"	
	"	"	110	"	"	A	A	A	A	A	A	A	A	"	"	"	H	H	H	H	H	H	H	H	H	B	"	"	"	"	
	"	"	111	"	"	A	A	A	A	A	A	A	A	"	"	"	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	112	"	"	B	B	B	B	B	B	B	B	"	"	"	H	H	H	H	H	H	H	H	H	A	"	"	"	"	
	"	"	113	"	"	B	B	B	B	B	B	B	B	"	"	"	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	114	"	"	"	"	"	"	"	"	"	"	"	"	"	H	H	H	H	H	H	H	H	H	A	"	"	"	"	
	"	"	115	"	"	A	A	A	A	A	A	A	A	"	"	"	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	116	"	"	"	"	"	"	"	"	"	"	"	"	"	H	H	H	H	H	H	H	H	H	A	"	"	"	"	
	"	"	117	B	"	"	"	"	"	"	"	"	"	"	"	B	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	118	A	"	"	"	"	"	"	"	"	"	"	"	A	H	H	H	H	H	H	H	H	H	A	"	"	"	"	
	"	"	119	"	"	"	"	"	"	"	"	"	"	"	"	B	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	120	B	"	"	"	"	"	"	"	"	"	"	"	A	H	H	H	H	H	H	H	H	H	A	"	"	"	"	
	"	"	121	A	"	"	"	"	"	"	"	"	"	"	"	B	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	122	"	"	B	B	B	B	B	B	B	B	"	"	A	H	H	H	H	H	H	H	H	H	A	"	"	"	"	
	"	"	123	"	"	A	A	A	A	A	A	A	A	"	"	A	L	L	L	L	L	L	L	L	L	B	"	"	"	"	
	"	"	124	B	"	A	A	A	A	A	A	A	A	"	"	B	H	L	L	L	L	L	L	L	L	A	"	"	"	"	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																													
9 T_C = +25°C	t_{PHL1}	3003 Fig. 5	125	IN	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	GND	IN	4.5 V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	4.5 V	5.0 V	1CLR to 1Q1	6	24	ns
			126	"	"									"	"	"	"									"	"	1CLR to 1Q2	"	"	"
			127	"	"									"	"	"	"									"	"	1CLR to 1Q3	"	"	"
			128											"	"	"	"									"	"	1CLR to 1Q4	"	"	"
			129											"	"	"	"									"	"	2CLR to 2Q1	"	"	"
			130											"	"	"	"									"	"	2CLR to 2Q2	"	"	"
			131											"	"	"	"									"	"	2CLR to 2Q3	"	"	"
			132											"	"	"	"									"	"	2CLR to 2Q4	"	"	"
	t_{PLH2}	"	133	4.5 V	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	"	4.5 V	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	"	1EN1C to 1Q1	8	22	"
			134	"	"									"	"	"	"									"	"	1EN1C to 1Q2	"	"	"
			135	"	"									"	"	"	"									"	"	1EN1C to 1Q3	"	"	"
			136											"	"	"	"									"	"	1EN1C to 1Q4	"	"	"
			137											"	"	"	"									"	"	2EN2C to 2Q1	"	"	"
			138											"	"	"	"									"	"	2EN2C to 2Q2	"	"	"
			139											"	"	"	"									"	"	2EN2C to 2Q3	"	"	"
			140											"	"	"	"									"	"	2EN2C to 2Q4	"	"	"
	t_{PHL2}	"	141	4.5 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	4.5 V	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	"	1EN1C to 1Q1	"	21	"
			142	"	"									"	"	"	"									"	"	1EN1C to 1Q2	"	"	"
			143	"	"									"	"	"	"									"	"	1EN1C to 1Q3	"	"	"
			144											"	"	"	"									"	"	1EN1C to 1Q4	"	"	"
			145											"	"	"	"									"	"	2EN2C to 2Q1	"	"	"
			146											"	"	"	"									"	"	2EN2C to 2Q2	"	"	"
			147											"	"	"	"									"	"	2EN2C to 2Q3	"	"	"
			148											"	"	"	"									"	"	2EN2C to 2Q4	"	"	"

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28	Measured terminal	Limits		Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	
			Test no.	$\overline{1CLR}$	$\overline{1OC}$	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	$\overline{2OC}$	GND	$\overline{2CLR}$	EN2C	2Q4	2Q3	2Q2	2Q1	1Q4	1Q3	1Q2	1Q1	EN1C	V_{CC}				
9 T_C = +25°C	t_{PLH3}	3003 Fig. 5	149 150 151 152 153 154 155 156	4.5 V " "	GND " "	IN	IN	IN	IN	IN	IN	IN	IN	GND "	GND " " " " " "	4.5 V " "	IN " "	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN " "	5.0 V " " " " " "	1D1 to 1Q1 1D2 to 1Q2 1D3 to 1Q3 1D4 to 1Q4 2D1 to 2Q1 2D2 to 2Q2 2D3 to 2Q3 2D4 to 2Q4	2 " " " " " " "	12 " " " " " " "	ns " " " " " " "
	t_{PHL3}	" " " " " " "	157 158 159 160 161 162 163 164	4.5 V " "	GND " "	IN	IN	IN	IN	IN	IN	IN	IN	GND "	GND " " " " " "	4.5 V " "	IN " "	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN " "	" " " " " " "	1D1 to 1Q1 1D2 to 1Q2 1D3 to 1Q3 1D4 to 1Q4 2D1 to 2Q1 2D2 to 2Q2 2D3 to 2Q3 2D4 to 2Q4	" " " " " " " "	" " " " " " " "	" " " " " " " "
	t_{PZH}	" " " " " " "	165 166 167 168 169 170 171 172	4.5 V " "	IN " "	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	IN " "	" " " " " " "	4.5 V " "	4.5 V " "	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	4.5 V " "	" " " " " " "	1$\overline{0C}$ to 1Q1 1$\overline{0C}$ to 1Q2 1$\overline{0C}$ to 1Q3 1$\overline{0C}$ to 1Q4 2$\overline{0C}$ to 2Q1 2$\overline{0C}$ to 2Q2 2$\overline{0C}$ to 2Q3 2$\overline{0C}$ to 2Q4	4 " " " " " " "	18 " " " " " " "	" " " " " " " "
	t_{PZL}	" " " " " " "	173 174 175 176 177 178 179 180	4.5 V " "	IN " "	GND	GND	GND	GND	GND	GND	GND	GND	IN " "	" " " " " " "	4.5 V " "	4.5 V " "	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	2/ " "	" " " " " " "	1$\overline{0C}$ to 1Q1 1$\overline{0C}$ to 1Q2 1$\overline{0C}$ to 1Q3 1$\overline{0C}$ to 1Q4 2$\overline{0C}$ to 2Q1 2$\overline{0C}$ to 2Q2 2$\overline{0C}$ to 2Q3 2$\overline{0C}$ to 2Q4	3 " " " " " " "	13 " " " " " " "	" " " " " " " "
	t_{PHZ}	" " " " " " "	181 182 183 184 185 186 187 188	4.5 V " "	IN " "	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	IN " "	" " " " " " "	4.5 V " "	4.5 V " "	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	2/ " "	" " " " " " "	1$\overline{0C}$ to 1Q1 1$\overline{0C}$ to 1Q2 1$\overline{0C}$ to 1Q3 1$\overline{0C}$ to 1Q4 2$\overline{0C}$ to 2Q1 2$\overline{0C}$ to 2Q2 2$\overline{0C}$ to 2Q3 2$\overline{0C}$ to 2Q4	2 " " " " " " "	8 " " " " " " "	" " " " " " " "

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 05 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28	Measured terminal	Limits		Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
			Test no.	1CLR	1CC	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	2CC	GND	2CLR	EN2C	2Q4	2Q3	2Q2	2Q1	1Q4	1Q3	1Q2	1Q1	EN1C	V_{CC}			Min	Max	
1/		MIL-STD-883 Fig. 5	188	4.5 V	IA	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	4.5 V	5.5 V	1CC to 1Q1	2	12	ns
		"	190	"	"										"	"	"											1CC to 1Q2	"	"	"
		"	191	"	"										"	"	"											1CC to 1Q3	"	"	"
		"	192	"	"										"	"	"											1CC to 1Q4	"	"	"
		"	193												"													2CC to 2Q1	"	"	"
		"	194												"													2CC to 2Q2	"	"	"
		"	195												"													2CC to 2Q3	"	"	"
		"	196												"													2CC to 2Q4	"	"	"
10 T_C = +125°C	t_{PHL1}	Same tests and terminal conditions as for subgroup 9, except T_C = +125°C.																											6	24	"
	t_{PLH2}																												8	25	"
	t_{PHL2}																												6	22	"
	t_{PLH3}																												2	15	"
	t_{PHL3}																												2	15	"
	t_{PZH}																												4	21	"
	t_{PZL}																												4	21	"
	t_{PHZ}																												2	10	"
	t_{PLZ}																												2	15	"
11 T_C = -55°C		Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C.																													

1/ Pins not referenced are N/C.

2/ I_{IL} limits shall be as follows:

Test	Limits in µA for circuit		
	A	B	C
I_{IL}	07-100	07-100	07-200

3/ Method 3011 shall be used, except the output voltage shall be as specified herein, and the output current shall be operating rather than short-circuit current. The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current I_{OS}.

4/ I_O limits for circuit C shall be -70 to -110 mA.

5/ Tests shall be performed in sequence, attributes data only.

6/ Outputs shall be high ≥1.5 V, low ≤1.5 V.

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/ Cases K,L Test no.	2 1 1PRE	3 2 1OC	4 3 1D1	5 4 1D2	6 5 1D3	7 6 1D4	9 7 2D1	10 8 2D2	11 9 2D3	12 10 2D4	13 11 2OC	14 12 GND	16 13 2PRE	17 14 EN2C	18 15 2Q4	19 16 2Q3	20 17 2Q2	21 18 2Q1	23 19 1Q4	24 20 1Q3	25 21 1Q2	26 22 1Q1	27 23 EN1C	28 24 V_{CC}	Measured terminal	Limits Min	Limits Max	Unit
1 T_C = +25°C	V_{OH}	3006	1	2.0 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	GND	2.0 V	2.0 V	-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA	2.0 V	4.5 V	1Q1	2.4		V
			2	"	"										"	"											1Q2	"		"
			3	"	"										"	"											1Q3	"		"
			4	"	"										"	"											1Q4	"		"
			5	"	"										"	"											2Q1	"		"
			6	"	"										"	"											2Q2	"		"
			7	"	"										"	"											2Q3	"		"
			8	"	"										"	"											2Q4	"		"
	V_{OL}	3007	9	2.0 V	0.8 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	"	2.0 V	2.0 V	12 mA	12 mA	12 mA	12 mA	12 mA	12 mA	12 mA	12 mA	2.0 V	"	1Q1		0.4	"
			10	"	"										"	"											1Q2			"
			11	"	"										"	"											1Q3			"
			12	"	"										"	"											1Q4			"
			13	"	"										"	"											2Q1			"
			14	"	"										"	"											2Q2			"
			15	"	"										"	"											2Q3			"
			16	"	"										"	"											2Q4			"
			17	"	"										"	"											1Q1			"
			18	"	"										"	"											1Q2			"
			19	"	"										"	"											1Q3			"
			20	"	"										"	"											1Q4			"
			21	"	"										"	"											2Q1			"
			22	"	"										"	"											2Q2			"
			23	"	"										"	"											2Q3			"
			24	"	"										"	"											2Q4			"
	V_{IC}		25	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	"	-18 mA	-18 mA									-18 mA	"	1PRE		-1.5	"
			26																									1OC			
			27																									1D1			
			28																									1D2			
			29																									1D3			
			30																									1D4			
			31																									2D1			
			32																									2D2			
			33																									2D3			
			34																									2D4			
			35																									2OC			
			36																									2PRE			
			37																									EN2C			
			38																									EN1C			
	I_{IL}	3009	39	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	"	0.4 V	0.4 V									0.4 V	5.5 V	1PRE	2/	2/	µA
			40																									1OC	"	"	"
			41																									1D1	"	"	"
			42																									1D2	"	"	"
			43																									1D3	"	"	"
			44																									1D4	"	"	"
			45																									2D1	"	"	"
			46																									2D2	"	"	"
			47																									2D3	"	"	"
			48																									2D4	"	"	"
			49																									2OC	"	"	"
			50																									2PRE	"	"	"
			51																									EN2C	"	"	"
			52																									EN1C	"	"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 3 1/ Cases K,L Test no.	1 1PRE	2 1CC	3 1D1	4 1D2	5 1D3	6 1D4	7 2D1	8 2D2	9 2D3	10 2D4	11 2CC	12 GND	13 2PRE	14 EN2C	15 2Q4	16 2Q3	17 2Q2	18 2Q1	19 1Q4	20 1Q3	21 1Q2	22 1Q1	23 EN1C	24 V_{CC}	Measured terminal	Limits Min	Limits Max	Unit
1 [illegible]	I_{IH1}	3010	53	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	GND	2.7 V	2.7 V										5.5 V	1PRE		20	µA
		"	54												"											"	1CC		"	"
		"	55												"											"	1D1		"	"
		"	56												"											"	1D2		"	"
		"	57												"											"	1D3		"	"
		"	58												"											"	1D4		"	"
		"	59												"											"	2D1		"	"
		"	60												"											"	2D2		"	"
		"	61												"											"	2D3		"	"
		"	62												"											"	2D4		"	"
		"	63												"											"	2CC		"	"
		"	64												"											"	2PRE		"	"
		"	65												"											"	EN2C		"	"
		"	66												"											"	EN1C		"	"
	I_{IHL}	"	67	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	7.0 V	"	7.0 V	7.0 V									7.0 V	"	1PRE		100	"
		"	68												"											"	1CC		"	"
		"	69												"											"	1D1		"	"
		"	70												"											"	1D2		"	"
		"	71												"											"	1D3		"	"
		"	72												"											"	1D4		"	"
		"	73												"											"	2D1		"	"
		"	74												"											"	2D2		"	"
		"	75												"											"	2D3		"	"
		"	76												"											"	2D4		"	"
		"	77												"											"	2CC		"	"
		"	78												"											"	2PRE		"	"
		"	79												"											"	EN2C		"	"
		"	80												"											"	EN1C		"	"
	I_O	3011 3/	81	5.0 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	5.0 V	5.0 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	2.25 V	5.0 V	1Q1	-15 4/	-70 4/	mA
		"	82	"	"																					"	1Q2	"	"	"
		"	83	"	"																					"	1Q3	"	"	"
		"	84																							"	1Q4	"	"	"
		"	85																							"	2Q1	"	"	"
		"	86																							"	2Q2	"	"	"
		"	87																							"	2Q3	"	"	"
		"	88																							"	2Q4	"	"	"
	I_{OZH}		89	5.0 V	5.0 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	5.0 V	"	5.0 V	5.0 V			2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	2.7 V	5.0 V	"	1Q1		20	µA
		"	90	"	"									"												"	1Q2		"	"
		"	91	"	"									"												"	1Q3		"	"
		"	92																							"	1Q4		"	"
		"	93																							"	2Q1		"	"
		"	94																							"	2Q2		"	"
		"	95																							"	2Q3		"	"
		"	96																							"	2Q4		"	"
	I_{OZL}		97	5.0 V	5.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	5.0 V	"	5.0 V	5.0 V			0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	0.4 V	5.0 V	"	1Q1		-20	"
		"	98	"	"									"												"	1Q2		"	"
		"	99	"	"																					"	1Q3		"	"
		"	100																							"	1Q4		"	"
		"	101																							"	2Q1		"	"
		"	102																							"	2Q2		"	"
		"	103																							"	2Q3		"	"
		"	104																							"	2Q4		"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 2 1/	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28	Measured terminal	Limits Min	Limits Max	Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
			Test no.	$\overline{1PRE}$	$\overline{1OC}$	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	$\overline{2OC}$	GND	$\overline{2PRE}$	EN2C	$2\overline{Q}4$	$2\overline{Q}3$	$2\overline{Q}2$	$2\overline{Q}1$	$1\overline{Q}4$	$1\overline{Q}3$	$1\overline{Q}2$	$1\overline{Q}1$	EN1C	V_{CC}				
1 T_C = +25°C	I_{CCH}	3005	105	5.0 V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.0 V	5.0 V									5.0 V	5.5 V	V_{CC}		21	mA
	I_{CCL}	"	106	GND	"	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	5.0 V	"	"	GND	"									"	"	V_{CC}		25	"
	I_{CCZ}	"	107	"	5.0 V	"	"	"	"	"	"	"	"	5.0 V	"	"	"									5.0 V	"	V_{CC}		31	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and V_{IC} tests are omitted.																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																														
7 5/ T_C = +25°C	Truth table tests	3014	108	A	B	B	B	B	B	B	B	B	B	B	GND	A	A	H	H	H	H	H	H	H	H	A	5.0 V	All outputs	6/	6/	
		"	109	"	"	A	A	A	A	A	A	A	A	"	"	"	"	L	L	L	L	L	L	L	L	"	"	"	"	"	
		"	110	"	"	B	B	B	B	B	B	B	B	"	"	"	"	H	H	H	H	H	H	H	H	"	"	"	"	"	
		"	111	"	"	B	B	B	B	B	B	B	B	"	"	"	B	"	"	"	"	"	"	"	"	B	"	"	"	"	
		"	112	"	"	A	A	A	A	A	A	A	A	"	"	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	
		"	113	"	"	"	"	"	"	"	"	"	"	"	"	"	A	L	L	L	L	L	L	L	L	A	"	"	"	"	
		"	114	"	"	"	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"	"	B	"	"	"	"	
		"	115	"	"	B	B	B	B	B	B	B	B	"	"	"	B	"	"	"	"	"	"	"	"	B	"	"	"	"	
		"	116	"	"	"	"	"	"	"	"	"	"	"	"	"	A	H	H	H	H	H	H	H	H	A	"	"	"	"	
		"	117	B	"	"	"	"	"	"	"	"	"	"	"	B	"	L	L	L	L	L	L	L	L	"	"	"	"	"	
		"	118	A	"	"	"	"	"	"	"	"	"	"	"	A	"	H	H	H	H	H	H	H	H	"	"	"	"	"	
		"	119	A	"	"	"	"	"	"	"	"	"	"	"	A	B	H	H	H	H	H	H	H	H	B	"	"	"	"	
		"	120	B	"	"	"	"	"	"	"	"	"	"	"	B	B	L	L	L	L	L	L	L	L	B	"	"	"	"	
		"	121	A	"	"	"	"	"	"	"	"	"	"	"	A	A	H	H	H	H	H	H	H	H	A	"	"	"	"	
		"	122	A	"	"	"	"	"	"	"	"	"	"	"	A	"	H	H	H	H	H	H	H	H	"	"	"	"	"	
		"	123	B											"	B	"	L	L	L	L	L	L	L	L	"	"	"	"	"	
8 5/	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and -55°C.																														
9 T_C = +25°C	t_{PHL1}	3003 Fig. 5	124	IN	GND	GND									GND										OUT	4.5 V	5.0 V	$\overline{1PRE}$ to $1\overline{Q}1$	6	21	ns
		"	125	"	"		GND								"									OUT		"	"	$\overline{1PRE}$ to $1\overline{Q}2$	"	"	"
		"	126	"	"			GND							"								OUT			"	"	$\overline{1PRE}$ to $1\overline{Q}3$	"	"	"
		"	127	"	"				GND						"							OUT				"	"	$\overline{1PRE}$ to $1\overline{Q}4$	"	"	"
		"	128							GND				GND	"	IN	4.5 V				OUT						"	$\overline{2PRE}$ to $2\overline{Q}1$	"	"	"
		"	129								GND			"	"	"	"			OUT							"	$\overline{2PRE}$ to $2\overline{Q}2$	"	"	"
		"	130									GND		"	"	"	"		OUT								"	$\overline{2PRE}$ to $2\overline{Q}3$	"	"	"
		"	131										GND	"	"	"	"	OUT									"	$\overline{2PRE}$ to $2\overline{Q}4$	"	"	"
	t_{PLH2}		132	4.5 V	GND	GND									"										OUT	IN	"	EN1C to $1\overline{Q}1$	8	24	"
			133	"	"		GND								"									OUT		"	"	EN1C to $1\overline{Q}2$	"	"	"
		"	134	"	"			GND							"								OUT			"	"	EN1C to $1\overline{Q}3$	"	"	"
		"	135	"	"				GND						"							OUT				"	"	EN1C to $1\overline{Q}4$	"	"	"
		"	136							GND				GND	"	4.5 V	IN				OUT						"	EN2C to $2\overline{Q}1$	"	"	"
		"	137								GND			"	"	"	"			OUT							"	EN2C to $2\overline{Q}2$	"	"	"
		"	138									GND		"	"	"	"		OUT								"	EN2C to $2\overline{Q}3$	"	"	"
		"	139										GND	"	"	"	"	OUT									"	EN2C to $2\overline{Q}4$	"	"	"
	t_{PHL2}	"	140	4.5 V	GND	4.5 V									"										OUT	IN	"	EN1C to $1\overline{Q}1$	"	21	"
		"	141	"	"		4.5 V								"									OUT		"	"	EN1C to $1\overline{Q}2$	"	"	"
		"	142	"	"			4.5 V							"								OUT			"	"	EN1C to $1\overline{Q}3$	"	"	"
		"	143	"	"				4.5 V						"							OUT				"	"	EN1C to $1\overline{Q}4$	"	"	"
		"	144							4.5 V				GND	"	4.5 V	IN				OUT						"	EN2C to $2\overline{Q}1$	"	"	"
		"	145								4.5 V			"	"	"	"			OUT							"	EN2C to $2\overline{Q}2$	"	"	"
		"	146									4.5 V		"	"	"	"		OUT								"	EN2C to $2\overline{Q}3$	"	"	"
		"	147										4.5 V	"	"	"	"	OUT									"	EN2C to $2\overline{Q}4$	"	"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case 5 1/	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28	Measured terminal	Limits		Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Min	Max	
			Test no.	1$\overline{PRE}$	1$\overline{OC}$	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	2$\overline{OC}$	GND	2$\overline{PRE}$	EN2C	2$\overline{Q}$4	2$\overline{Q}$3	2$\overline{Q}$2	2$\overline{Q}$1	1$\overline{Q}$4	1$\overline{Q}$3	1$\overline{Q}$2	1$\overline{Q}$1	EN1C	V_{CC}				
T_C = +25°C	t_{PLH}	3003 Fig. 5	148	4.5 V	GND	IN	IN	IN	IN	IN	IN	IN	IN	GND	GND	4.5 V	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	5.0 V	1D1 to 1$\overline{Q}$1	5	20	ns
			149	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D2 to 1$\overline{Q}$2	"	"	"
			150	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D3 to 1$\overline{Q}$3	"	"	"
			151	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D4 to 1$\overline{Q}$4	"	"	"
			152	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D1 to 2$\overline{Q}$1	"	"	"
			153	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D2 to 2$\overline{Q}$2	"	"	"
			154	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D3 to 2$\overline{Q}$3	"	"	"
			155	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D4 to 2$\overline{Q}$4	"	"	"
	t_{PHL}	"	156	4.5 V	GND	IN	IN	IN	IN	IN	IN	IN	IN	GND	GND	4.5 V	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	"	1D1 to 1$\overline{Q}$1	5	12	"
			157	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D2 to 1$\overline{Q}$2	"	"	"
			158	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D3 to 1$\overline{Q}$3	"	"	"
			159	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D4 to 1$\overline{Q}$4	"	"	"
			160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D1 to 2$\overline{Q}$1	"	"	"
			161	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D2 to 2$\overline{Q}$2	"	"	"
			162	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D3 to 2$\overline{Q}$3	"	"	"
			163	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D4 to 2$\overline{Q}$4	"	"	"
	t_{PLH}	"	164	4.5 V	IN	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	4.5 V	"	1D1 to 1$\overline{Q}$1	5	18	"
			165	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D2 to 1$\overline{Q}$2	"	"	"
			166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D3 to 1$\overline{Q}$3	"	"	"
			167	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1D4 to 1$\overline{Q}$4	"	"	"
			168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D1 to 2$\overline{Q}$1	"	"	"
			169	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D2 to 2$\overline{Q}$2	"	"	"
			170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D3 to 2$\overline{Q}$3	"	"	"
			171	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2D4 to 2$\overline{Q}$4	"	"	"
	t_{PZL}	"	172	4.5 V	IN	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	IN	4.5 V	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	4.5 V	"	1$\overline{OC}$ to 1$\overline{Q}$1	5	18	"
			173	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1$\overline{OC}$ to 1$\overline{Q}$2	"	"	"
			174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1$\overline{OC}$ to 1$\overline{Q}$3	"	"	"
			175	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1$\overline{OC}$ to 1$\overline{Q}$4	"	"	"
			176	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$1	"	"	"
			177	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$2	"	"	"
			178	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$3	"	"	"
			179	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$4	"	"	"
	t_{PHZ}	"	180	4.5 V	IN	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	4.5 V	4.5 V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	4.5 V	"	1$\overline{OC}$ to 1$\overline{Q}$1	2	20	"
			181	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1$\overline{OC}$ to 1$\overline{Q}$2	"	"	"
			182	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1$\overline{OC}$ to 1$\overline{Q}$3	"	"	"
			183	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1$\overline{OC}$ to 1$\overline{Q}$4	"	"	"
			184	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$1	"	"	"
			185	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$2	"	"	"
			186	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$3	"	"	"
			187	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2$\overline{OC}$ to 2$\overline{Q}$4	"	"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be high ≥2.0 V, or low ≤0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case Ω 1/	2	3	4	5	6	7	8	9	10	11	12	13	14	16	17	18	19	20	21	22	24	25	26	27	28	Measured terminal	Limits		Unit
			Cases K,L	1	2	3	4	5	6	7	8	9	10	11	12	13	15	14	15	16	17	18	19	20	21	22	23	24				
			Test no.	$\overline{1PRE}$	$\overline{1OC}$	1D1	1D2	1D3	1D4	2D1	2D2	2D3	2D4	$\overline{2OC}$	GND	$\overline{2PRE}$	EN2C	$\overline{2Q4}$	$\overline{2Q3}$	$\overline{2Q2}$	$\overline{2Q1}$	$\overline{1Q4}$	$\overline{1Q3}$	$\overline{1Q2}$	$\overline{1Q1}$	EN1C	V_{CC}				
9 T_C = +25°C	t_{PLZ}	3003 Fig. 5	186	4.5 V	IN	4.5 V	4.5 V	4.5 V	GND	4.5 V	$\overline{1OC}$ to $1\overline{Q1}$	5	15	ns
			189	"	"				"		$\overline{1OC}$ to $1\overline{Q2}$			
			190	"	"				"		$\overline{1OC}$ to $1\overline{Q3}$			
			191	"	"				"		$\overline{1OC}$ to $1\overline{Q4}$			
			192	"	"				"		$\overline{2OC}$ to $2\overline{Q1}$			
			193	"	"				"		$\overline{2OC}$ to $2\overline{Q2}$			
			194	"	"				"		$\overline{2OC}$ to $2\overline{Q3}$			
			195	"	"				"		$\overline{2OC}$ to $2\overline{Q4}$			
10 T_C = +125°C	t_{PHL1}	Same tests and terminal conditions as for subgroup 9, except T_C = +125°C.																												6	24	"
	t_{PLH2}																													8	31	"
	t_{PHL2}																													8	22	"
	t_{PLH3}																													3	23	"
	t_{PHL3}																													3	15	"
	t_{PZH}																													4	21	"
	t_{PZL}																													4	21	"
	t_{PH2}																													2	10	"
	t_{PLZ}																															
11 T_C = -55°C		Same tests, terminal conditions, and limits as for subgroup 10, except T_C = -55°C.																														

1/ Pins not referenced are N/C.

2/ I_{IL} limits shall be as follows:

Test	Limits in μA for circuit		
	A	B	C
I_{IL}	0/-100	0/-100	0/-200

3/ Method 3011 shall be used, except the output voltage shall be as specified herein, and the output current shall be operating rather than short-circuit current. The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current I_{OS}.

4/ I_O limits for circuit C shall be -70 to -110 mA.

5/ Tests shall be performed in sequence, attributes data only.

6/ Outputs shall be high ≥1.5 V, low ≤1.5 V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable, these requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	Ground zero voltage potential.
V_{IN}	Voltage level at an input terminal.
I_{IN}	Current flowing into an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer lead lengths and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	54ALS573
02	54ALS580
03	54ALS873
04	54ALS880

6.6 Manufacturers' designations. Manufacturers' circuits which form a part of this specification are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturers' designations.

Device type	Circuits		
	A	B	C
	Texas Instruments	Motorola Inc.	National Semi-conductor Corp.
01	X		
02	X		
03	X		
04	X		

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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