TEXAS INSTRUMENTS

TVP5031

NTSC/PAL Digital Video Decoder

Data Manual

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MSDS Multimedia

SLAS267

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Contents

List of Illustrations

List of Tables

1 Introduction

The TVP5031 is a high quality single-chip digital video decoder that converts base-band analog National Television System Committee (NTSC) and phase alternating line (PAL) video into digital component video. The TVP5031 includes a 9-bit A/D converter with 2x sampling. Sampling is square-pixel or ITU-R BT.601 (27 MHz) and is line-locked for correct pixel alignment. The output formats can be 8-bit, 10-bit or 16-bit 4:2:2, and 8-bit or 10-bit ITU-R BT.656 with embedded synchronization. The TVP5031 utilizes Texas Instruments patented technology for locking to weak, noisy, or unstable signals, and a chroma frequency control output is generated for synchronizing downstream video encoders.

Complementary three-line adaptive (2-H delay) comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available. Video characteristics including hue, contrast, and saturation may be programmed using one of four supported host port interfaces; I^2C and three parallel host interface (PHI) modes. The TVP5031 generates synchronization, blanking, field, lock and clock signals in addition to digital video outputs.

The TVP5031 includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor slices, parses, and performs error checking on teletext data in several formats. A built-in FIFO stores up to 14 lines of teletext data, and with proper host synchronization full-screen teletext retrieval is enabled. The VBI data processor also retrieves closed-caption data. The TVP5031 can also pass through over sampled raw composite data for host-based software VBI processing.

The main blocks of the TVP5031 include:

- Analog processors and A/D converters
- Y/C separation
- Chrominance processor
- Luminance processor
- Clock/timing processor and power-down control
- Output formatter
- Host port interface
- VBI data processor

1.1 Features

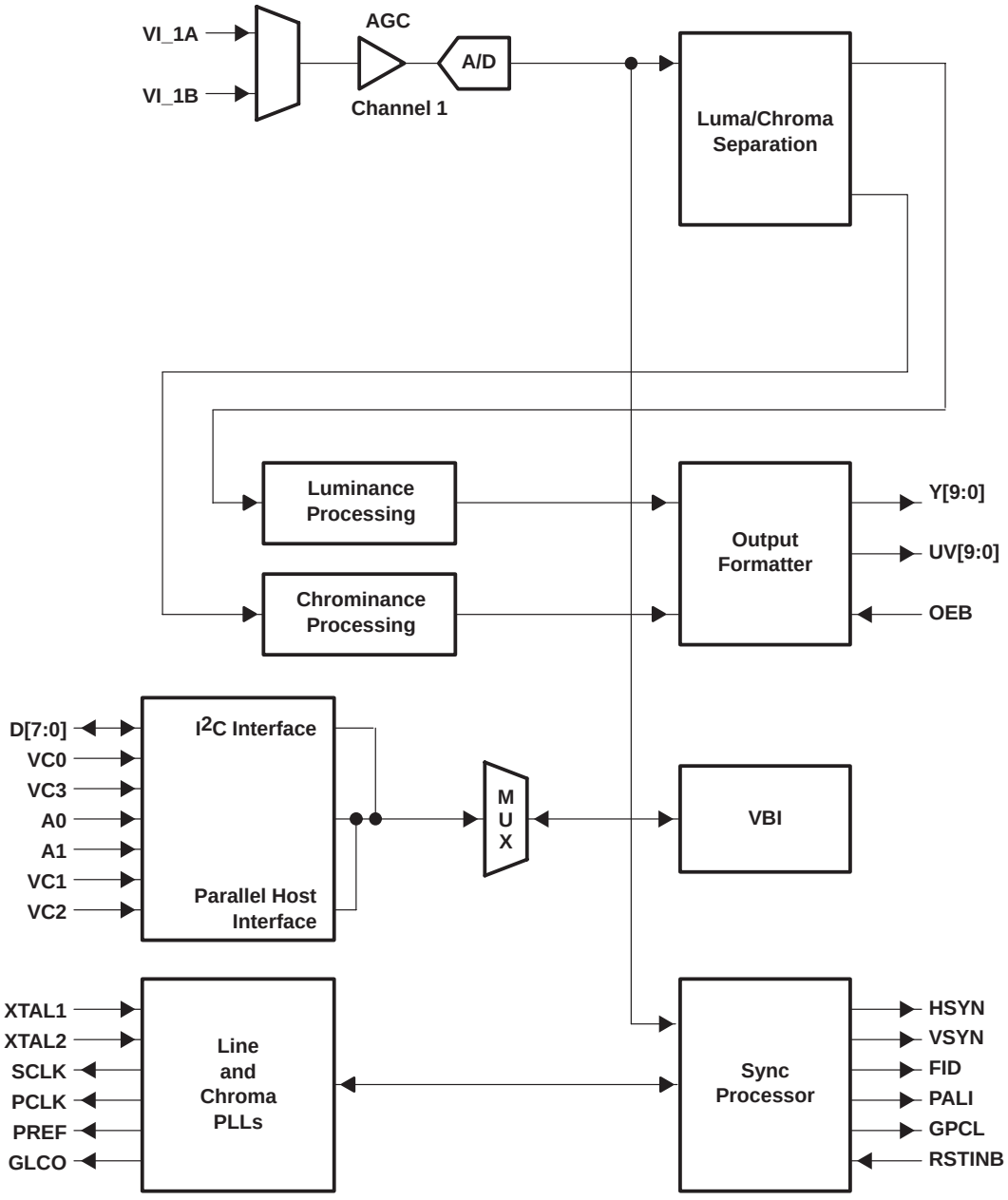
- Accepts NTSC (M) and PAL (B, D, G, H, I, M, N) composite video
- Two analog video inputs for composite video
- A fully differential CMOS analog preprocessing channel with clamping and AGC for best S/N performance
- High speed 2x over-sampling 9-bit A/D converter
- Patented architecture for locking to weak, noisy, or unstable signals
- Single 14.31818 MHz reference crystal for all standards
- Line-locked clock and sampling at square-pixel or 27 MHz rates
- Programmable output data rates:
  - 12.2727 MHz Square-Pixel (NTSC)
  - 14.7500 MHz Square-Pixel (PAL)
  - 13.5 MHz ITU-R BT.601 (NTSC and PAL)
- Optional automatic switching between PAL and NTSC standards

- Complementary 3-line (2-H delay) adaptive comb filters for both cross-luminance and cross-chrominance noise reduction
- Subcarrier genlock output for synchronizing color subcarrier of external encoder
- Standard programmable video output formats:
  - 16-bit 4:2:2 YCbCr
  - 20-bit 4:2:2 YCbCr
  - 8-bit 4:2:2 YCbCr
  - 10-bit 4:2:2 YCbCr
  - ITU-R BT.656 8-bit 4:2:2 with embedded syncs
  - ITU-R BT.656 10-bit 4:2:2 with embedded syncs
- Advanced programmable video output formats:
  - 2x oversampled raw VBI data during active video
  - Sliced VBI data as ancillary data in video stream
- Teletext (NABTS, WST) and closed-caption decode with FIFO
- Programmable host port options including I^2C and three parallel host interface (PHI) modes
- Brightness, contrast, saturation , and hue control through host port
- 5-V tolerant digital I/O ports
- 80-pin TQFP package

1.2 Applications

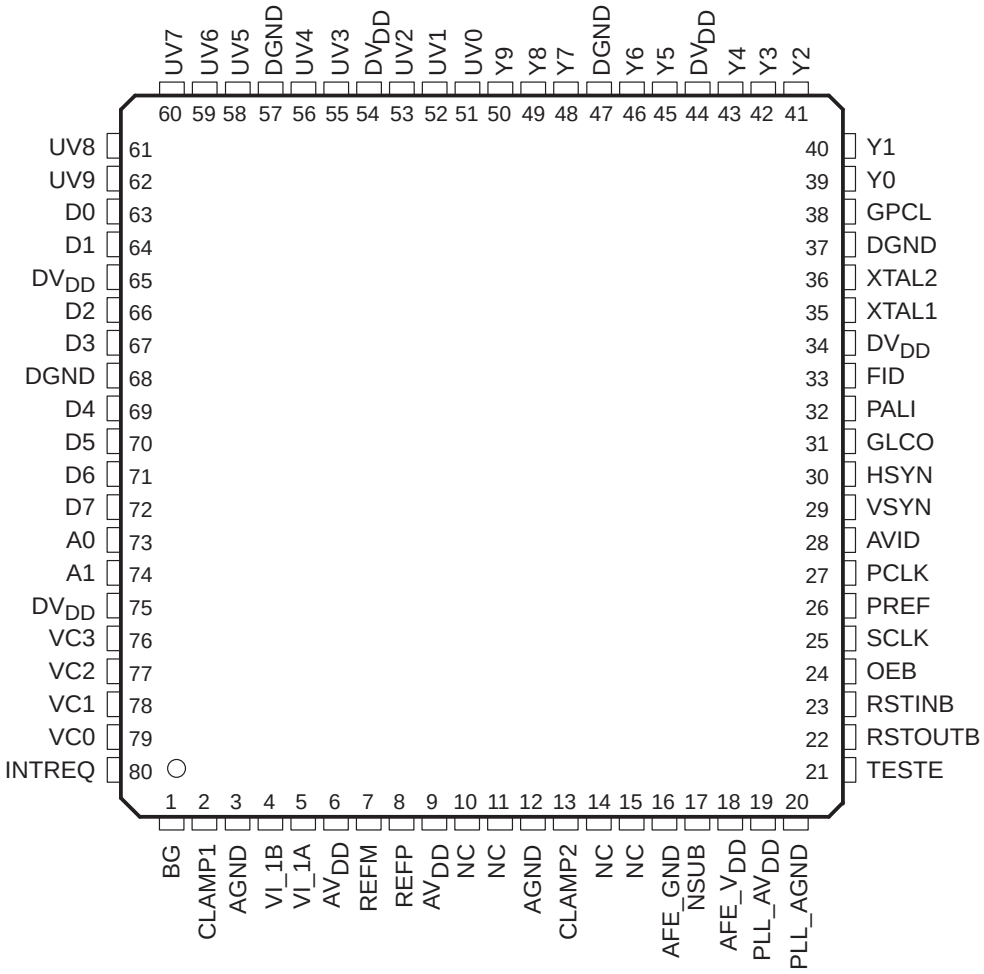
- Digital image processing
- Video conferencing
- Multimedia
- Digital video
- Desktop video
- Video capture
- Video editing
- Security applications

1.3 Functional Block Diagram



1.4 Terminal Assignments

TQFP PACKAGE
(TOP VIEW)



1.5 Ordering Information

DEVICE:	TVP5031CPFP
PFP:	Plastic flat-pack with PowerPAD™

PowerPAD is a trademark of Texas Instruments.

1.6 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Analog Video			
VI_1A VI_1B	5 4	I	Analog video inputs. Up to two composite inputs. The inputs must be AC coupled. The recommended coupling is 0.1 μF
Clock Signals			
PCLK	27	O	Pixel clock output. The frequency is 12.2727 MHz for square-pixel NTSC, 14.75 MHz for square-pixel PAL, and 13.5 MHz for ITU-R.BT.601 sampling modes.
PREF	26	I/O	Clock phase reference signal. This signal qualifies clock edges when SCLK is used to clock data that is changing at the pixel clock rate.
SCLK	25	O	System clock output with twice the frequency of the pixel clock (PCLK).
XTAL1 XTAL2	35 36	I	External clock reference. The user may connect XTAL1 to a TTL-compatible oscillator or to one terminal of a crystal oscillator. The user may connect XTAL2 to the other terminal of the crystal oscillator or not connect XTAL2 at all. One single 14.31818 MHz crystal or oscillator is needed for square pixel sampling and ITU-R BT.601 sampling.
Digital Video			
UV[9:0]	62, 61, 60, 59, 58, 56, 55, 53, 52, 51	I/O	10-bit digital chrominance outputs. These terminals may also be configured to output the data from the channel 2 A/D converter.
Y[9:0]	50, 49, 48, 46, 45, 43, 42, 41, 40, 39	I/O	10-bit digital luminance outputs, or 10-bit multiplexed luminance and chrominance outputs. These terminals may also be configured to output the data from the channel 1 A/D converter.
Host Port-Bus			
A[1:0]	74, 73	I	PHI mode: PHI address port.
D[7:0]	72, 71, 70, 69, 67, 66, 64, 63	I/O	PHI mode: PHI data port-bit [7:0].
INTREQ	80	I/O	PHI mode: Interrupt Request (INTREQ). Pullup is required if configured as open drain. I^2C mode: Interrupt Request (INTREQ). Pullup is required if configured as open drain.
VC0	79	I/O	PHI mode: PHI port data acknowledgement or ready signal **(**DTACK**)** I^2C mode: Serial clock (SCL) pullup is required.
VC1	78	I/O	PHI mode: PHI port read-write or write (RW/WR) I^2C mode: Serial data (SDA) pullup is required.
VC2	77	I/O	PHI mode: PHI port data strobe or read signal (DS/RD)
VC3	76	I	PHI mode: PHI port chip select (VC) I^2C mode: Slave address select (I^2CA)

1.6 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Miscellaneous Signals			
RSTOUTB	22	O	Reset output, active low
RSTINB	23	I	Reset input, active low
OEB	24	I/O	Output enable for Y and UV terminals. Output enable is also controllable via the host port. When this terminal is a logic 1 forces Y and UV output terminals to high impedance states (active low).
GLCO	31	I/O	This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control by the TVP5031. Data is transmitted at the SCLK rate. Additionally, this terminal, in conjunction with PALI and FID, is used to determine the host port mode configuration during initial powerup.
GPCL	38	I/O	General-purpose control logic. This terminal has three functions: 1) General-purpose output. In this mode the state of GPCL is directly programmed via the host port. 2) Vertical blank output. In this mode the GPCL terminal is used to indicate the vertical blanking interval of the output video. The beginning and end times of this signal are programmable via the host port. 3) Sync lock control input. In this mode when GPCL is high, the output clock frequencies and the sync timing are forced to nominal values.
CLAMP1, CLAMP2	2, 13	O	Clamp voltage outputs. Connect a 0.1 μF decoupling capacitor from each terminal to AGND.
NC	10, 11, 14, 15		No connection
BG	1	O	Connect a 1.0-μF capacitor from this terminal to AGND.
Power Supplies			
AFE_V_{DD}	18		Analog supply. Connect to 3.3-V analog supply
AFE_GND	16		Analog ground
AGND	3, 12		Analog grounds
AV_{DD}	6, 9		Analog supply. Connect to 3.3-V analog supply
DGND	37, 47, 57, 68		Digital grounds
PLL_AGND	20		PLL ground. Connect to analog ground
PLL_AV_{DD}	19		PLL supply. Connect to 3.3-V analog supply
DV_{DD}	34, 44, 54, 65, 75		Digital supply. Connect to 3.3-V
NSUB	17		Substrate ground. Connect to analog ground
REFP	8	O	A/D reference supply. Connect a 4.7-μF capacitor from each terminal to AGND. Connect a 1.0-μF capacitor across the REFM and REFP terminals.
REFM	7	O	
Sync Signals			
AVID	28	I/O	Active video indicator. This signal is high during the horizontal active time of the video output on the Y and UV terminals. AVID continues to toggle during vertical blanking intervals. This terminal may be placed in a high-impedance state. During reset, AVID is an input, used to program the behavior of Y[9:0], UV[9:0], HSYN, VSYN, AVID and FID immediately after the completion of reset. If AVID is pulled up during reset, Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI and FID will be actively driving after reset. If AVID is pulled down during reset, Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI and FID will remain in high-impedance state after reset.
FID	33	I/O	Odd/even field indicator or vertical lock indicator. For odd/even indicator, a logic 1 indicates the odd field. For vertical lock indicator, a logic 1 indicates the internal vertical PLL is in a locked state. Additionally, this terminal in conjunction with GLCO and PALI is used to determine the host port configuration during initial power up and reset.

1.6 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Sync Signals (Continued)			
PALI	32	I/O	PAL line indicator or horizontal lock indicator. For PAL line indicator, a logic 1 indicates a noninverted line, and a logic 0 indicates an inverted line. For horizontal lock indicator, a logic 1 indicates the internal horizontal PLL is in a locked state. This terminal is an input terminal during reset and is used in conjunction with GLCO and FID to select the mode of the host interface. During reset, this terminal can be pulled up to set a 1, or pulled down to set a 0.
VSYN	29	O	Vertical sync signal

1.7 Strapping Terminals Description

All of the following terminals have reset strapping options. The states of these terminals are sampled during reset to configure TVP5031 for various modes of operation. These terminals are temporarily turned into inputs with weak internal pulldowns (~40 kΩ resistor) during reset and return to their normal operation after reset. Each of the following terminals can be pulled up with a 10-KΩ resistor to set a 1 to the corresponding bit or be left undriven during reset, relying on the internal pulldown resistor to pull the terminal low to set a 0 to the corresponding bit.

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AVID	28	Y, U/V output enable (bit 4) and HSYN, VSYN, AVID, FID, and PALI output enable (bit 3) of miscellaneous control (Register 03)
PREF	26	Clock enable bit (bit 0) of miscellaneous control (Register 03)
FID	33	Host interface mode (see Table 2-2).
PALI	32	Host interface mode (see Table 2-2).
GLCO	31	Host interface mode (see Table 2-2).

2 Functional Description

2.1 Analog Video Processing and A/D Converters

Figure 2–1 shows a functional diagram of the analog video preprocessor and A/D converter. This block provides the analog interface to all the video inputs. It accepts up to two inputs and performs source selection, video clamping, video amplification, analog-to-digital conversion, and fine gain and offset adjustments to center the digitized video signal.

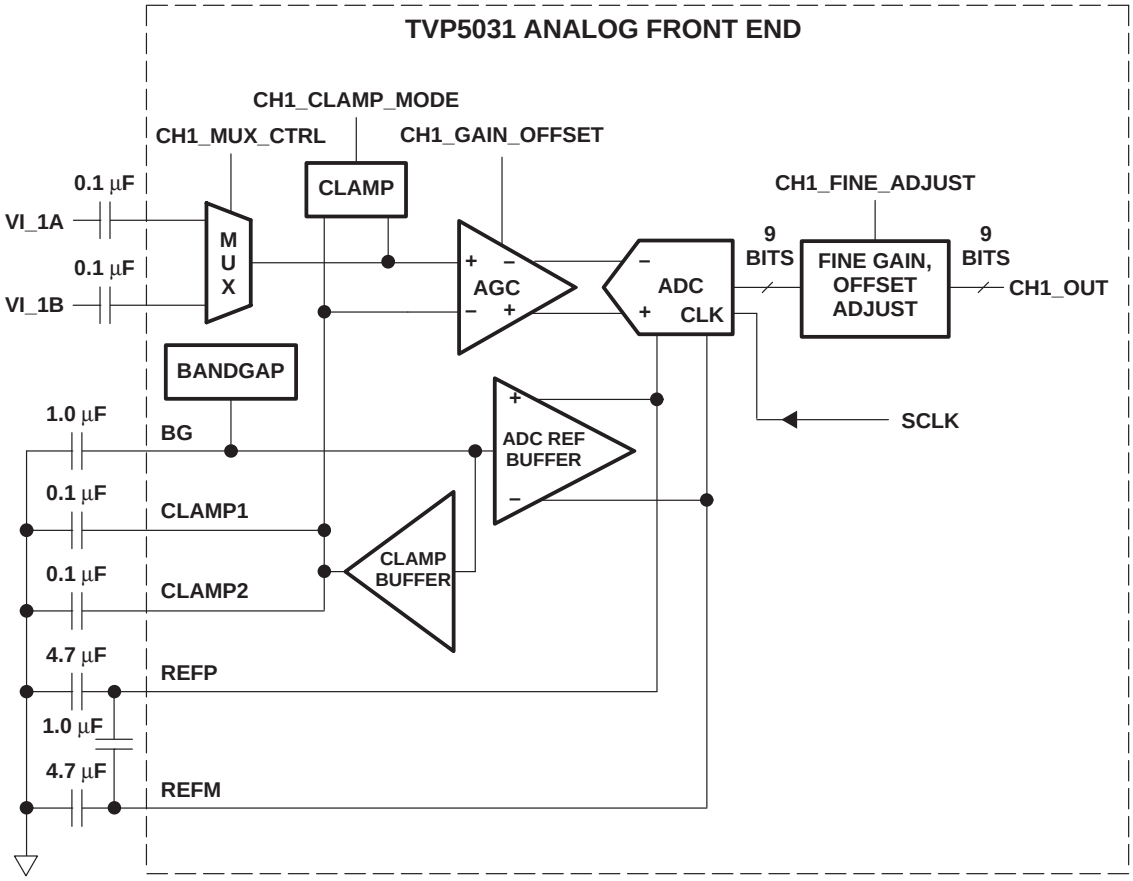


Figure 2–1. Analog Video Processors and A/D Converters

2.1.1 Video Input Selection

The TVP5031 has one analog channel that accepts two video inputs ac coupled through 0.1 µF capacitors. The internal video multiplexers can be configured via the host port. The two analog video inputs may be connected as two selectable individual composite video inputs.

2.1.2 Analog Input Clamping and Automatic Gain Control Circuits

An internal clamping circuit restores the ac coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage. Two modes of clamping are provided, coarse and fine. In coarse mode, the most negative portion of the input signal (typically the sync tip) is clamped to a fixed dc level. Fine clamp mode may be enabled to prevent spurious level shifting caused by noise more negative than the sync tip on the input signal. If fine clamp mode is selected, clamping is only enabled during the sync period. S-video requires fine clamp mode on the chroma channel for proper operation. External capacitors of 0.1 μF on terminal CLAMP1 and CLAMP2 are required to store and filter the clamp voltage.

Input video signal amplitude may vary significantly from the nominal level of $1V_{pp}$. An automatic gain control circuit (AGC) adjusts the signal amplitude to utilize the maximum range of the A/D converter without clipping. The AGC adjusts gain to achieve desired sync amplitude. Some nonstandard video signals contain peak white levels that saturate the A/D converter. In these cases, AGC automatically cuts back gain to avoid clipping.

In the digital data path, scaling is applied to the A/D output data to reach CCIR601 Y, Cr, Cb levels. This scaling introduces distortion if digitized sync tip and back porch levels are not precise. The fine gain and offset adjustment block precisely controls the sync tip and back porch levels to achieve best linearity performance.

2.1.3 A/D Converter

The TVP5031 contains one 9-bit oversampling A/D converter that digitizes the analog video inputs. As the input is digitized at greater than two times the Nyquist sampling rate, only a simple external antialiasing low pass filter is needed to prevent out-of-band frequencies. A/D converter reference voltages on terminals REFP and REFM require an external capacitor network for filtering, as shown in Figure 2–1.

2.2 Digital Processing

Figure 2–2 is a block diagram of the TVP5031 digital video decoder processing. This block receives digitized composite video signal from the A/D converter and performs Y/C separation, and Y, U/V signal enhancements. It also generates horizontal and vertical syncs. The Y U/V digital output may be programmed into various formats: 20-bit, 16-bit, 10-bit or 8-bit 4:2:2, and 10-bit or 8-bit ITU-R BT.656 parallel interface standard. This block also retrieves VBI data and stores it in a FIFO. The data from the FIFO can be read either through the host port or output as ancillary data on the video port.

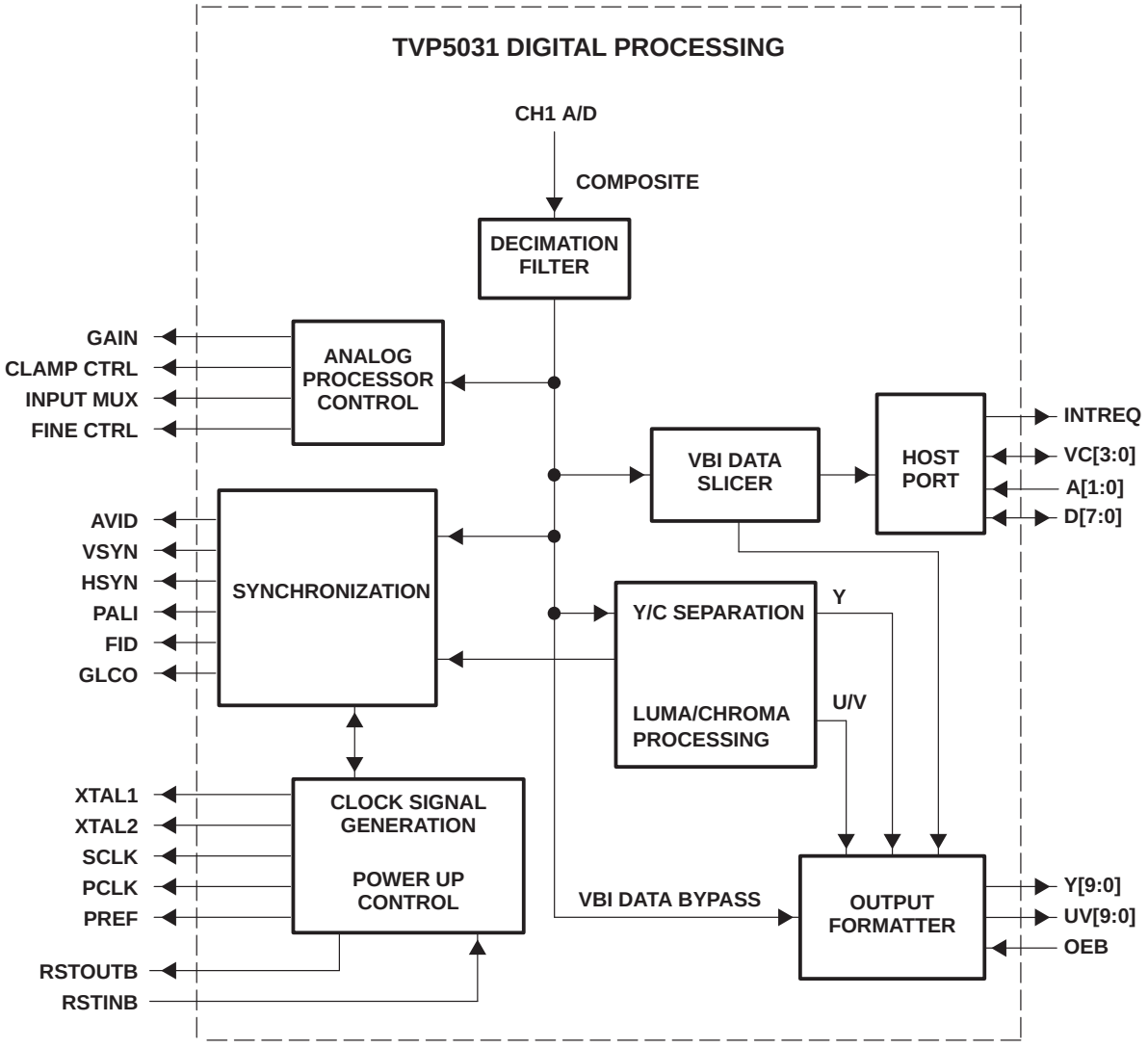


Figure 2–2. Digital Video Signal Processing Block Diagram

2.2.1 Decimation Filter

Digitized composite video at 2x PCLK rate first passes through the decimation filter that reduces the data rate from 2x to 1x PCLK. The decimation filter is a half-band filter whose frequency response is shown in Figure 2–3. For applications that cannot tolerate high frequency rolloff, the decimation filter can be bypassed the host port. 2x oversampling and decimation filtering can effectively increase the overall signal-to-noise ratio by 3 dB. This advantage is lost if decimation filtering is bypassed.

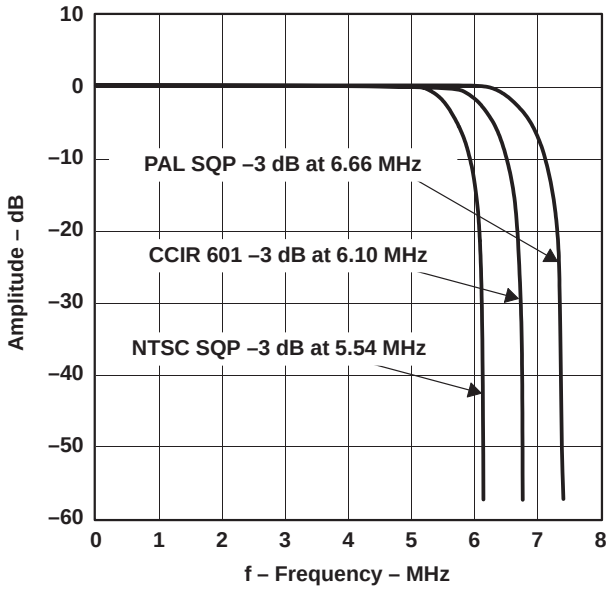


Figure 2–3. Decimation Filter Frequency Response

2.2.2 Y/C Separation

Figure 2–4 illustrates the luminance/chrominance (Y/C) separation process in the TVP5031. The 9-bit composite video is multiplied by subcarrier signals in the quadrature demodulator to generate color difference signals U and V. U and V are then low-pass filtered to achieve the desired bandwidth. An adaptive 3-line comb filter separates UV from Y based on the unique property of color phase shift from line to line. Chroma is remodulated through a quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C separation is completely complementary, thus there is no loss of information. However in some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. Contrast, brightness, hue, and saturation are programmable.

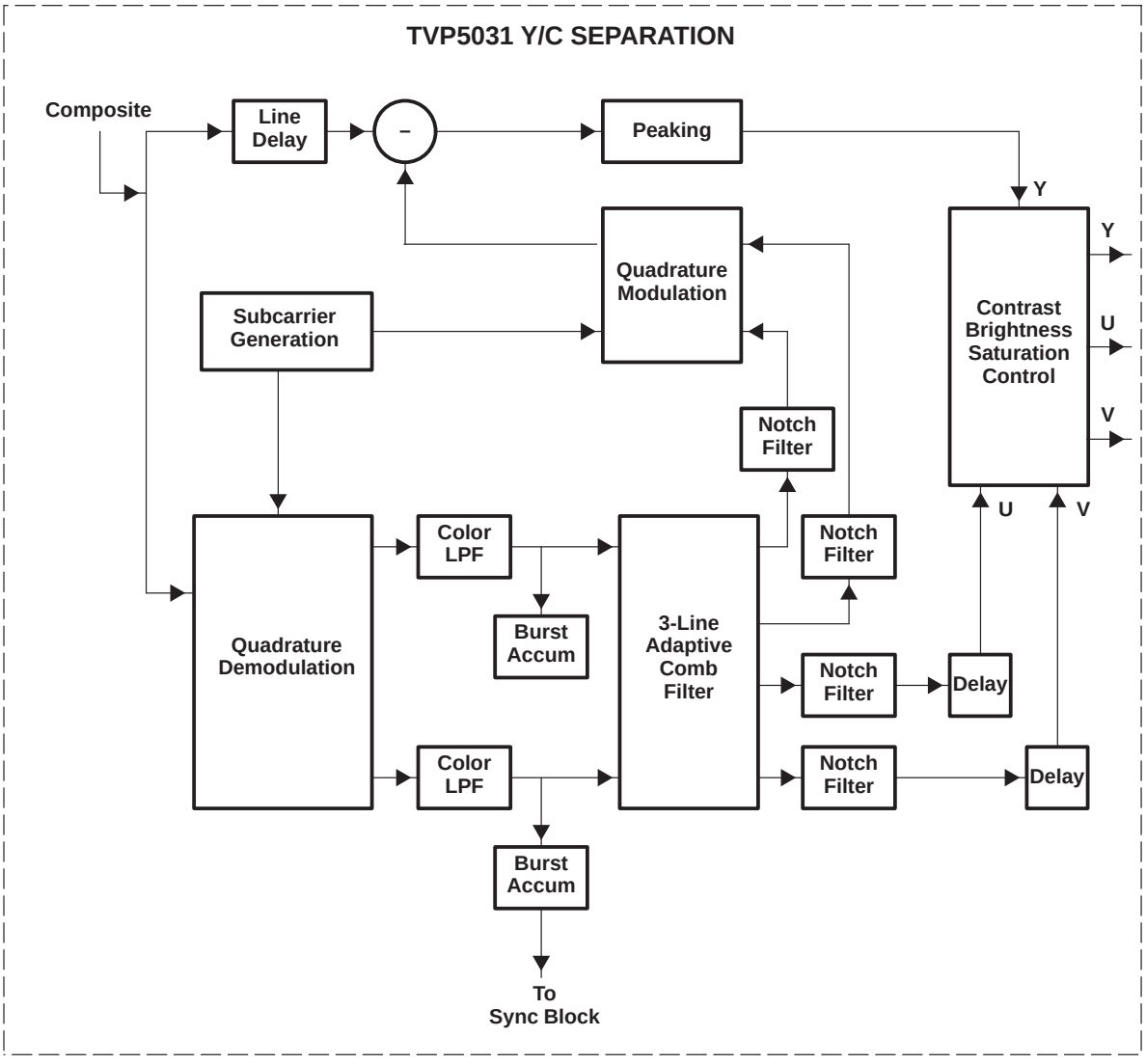


Figure 2–4. Y/C Separation Block Diagram

2.2.2.1 Color Low-Pass Filter

Color low-pass filter frequency responses are shown in Figures 2–5 to 2–8. High filter bandwidth preserves sharp color transitions and produces crisp color boundaries. However for nonstandard video sources that have asymmetrical U and V side bands, it is desirable to limit the filter bandwidth to avoid UV crosstalk. Color low-pass filter bandwidth is programmable by enabling one of the three notch filters.

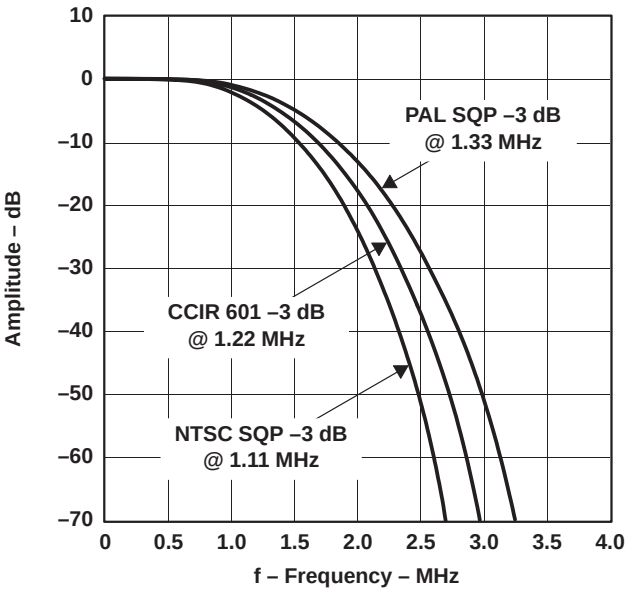


Figure 2–5. Color Low-Pass Filter Frequency Response

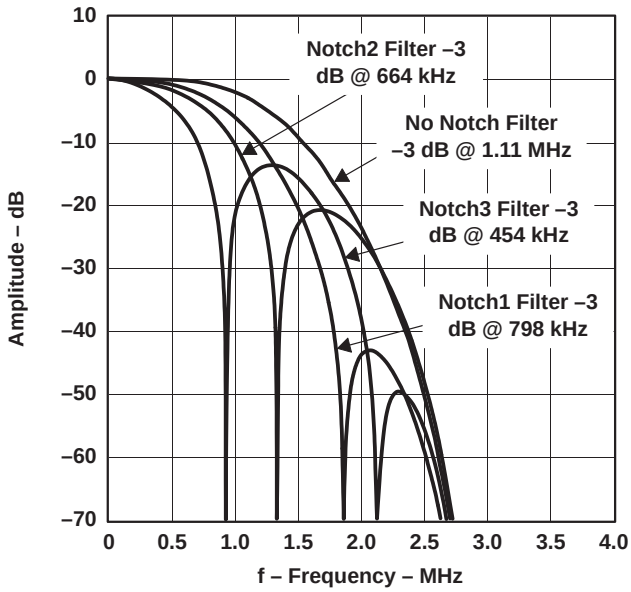


Figure 2–6. Color Low-Pass Filter With Notch Filter Frequency Response (NTSC and PAL-M Square Pixel Sampling)

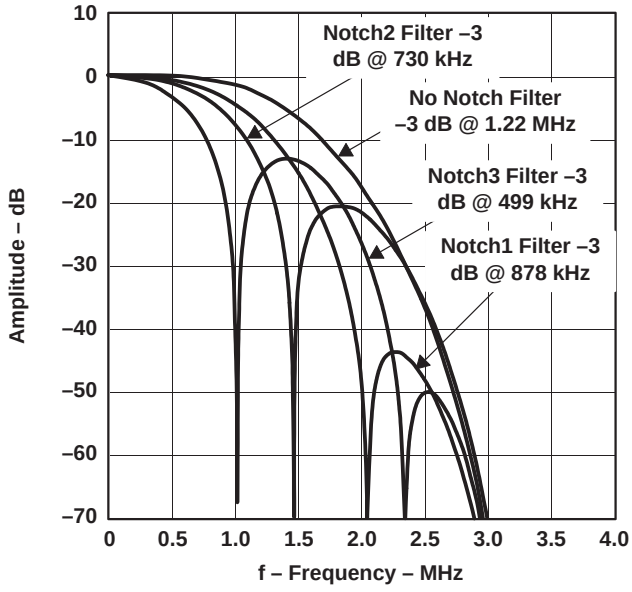


Figure 2–7. Color Low-Pass Filter With Notch Filter Characteristics (13.5 MHz Sampling)

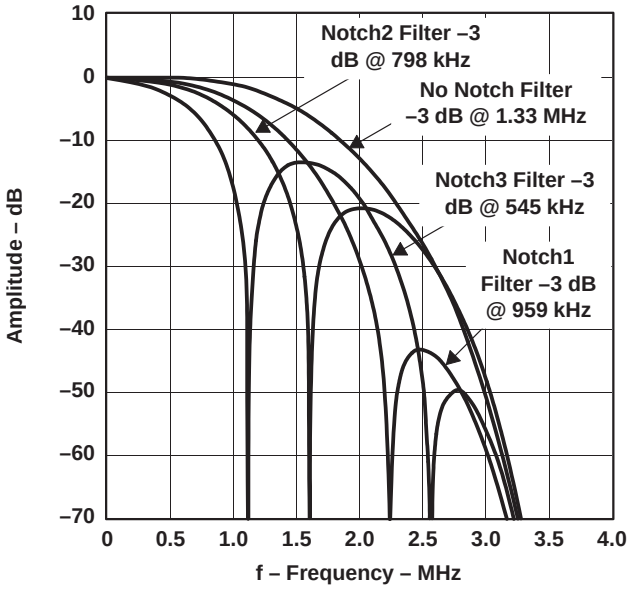


Figure 2–8. Color Low-Pass Filter With Notch Filter Frequency Response (PAL Square Pixel Sampling)

2.2.2.2 Adaptive Comb Filter

Y/C separation may be done using adaptive 3-line (2-H delay), fixed 3-line, fixed 2-line comb filters, or a chroma trap filter as shown in Figure 2–9. Adaptive comb filtering is available for both luminance and chrominance. The adaptive comb filter algorithm computes the vertical and horizontal contours of color based on a block of 3×3 pixels. If there is a sharp color transition, comb filtering is applied to the two lines that have less color changes. If there is no color transition, 3-line comb filtering is used with a choice of filter coefficients [1/4, 1/2, 1/4] or [1/2, 0, 1/2] programmable via the host port. Characteristics of 2-line and 3-line comb filters are shown in Figure 2–10. The filter frequency plots show that both 2-line and 3-line (with filter coefficients [1/4,1/2,1/4]) comb filters have zeros at 1/2 of the horizontal line frequency to separate the interleaved Y/C spectrum in NTSC. The 3-line comb filter has less cross-luma and cross-chroma noise due to slightly sharper filter cut off. The 3-line comb filter with filter coefficients[1/2, 0, 1/2] has two zeros at 1/4 and 3/4 of the horizontal line frequency. This should be used for PAL only because of its 90 degrees U/V phase shifting from line to line. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figures 2–11 to 2–13. TI's patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundary and detects and properly handles false colors in high frequency luminance images such as a multiburst pattern or circle pattern. Adaptive comb filtering is the recommended mode of operation.

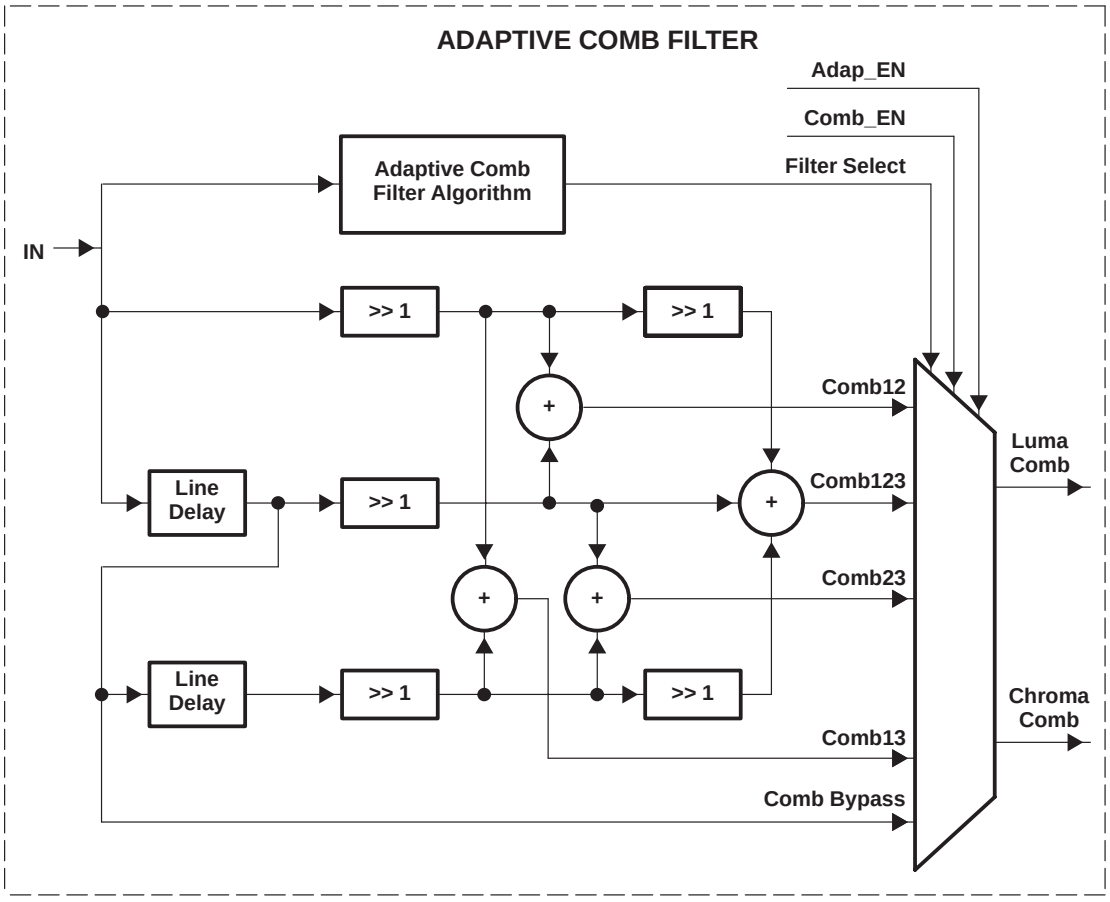


Figure 2–9. 3-Line Adaptive Comb Filtering

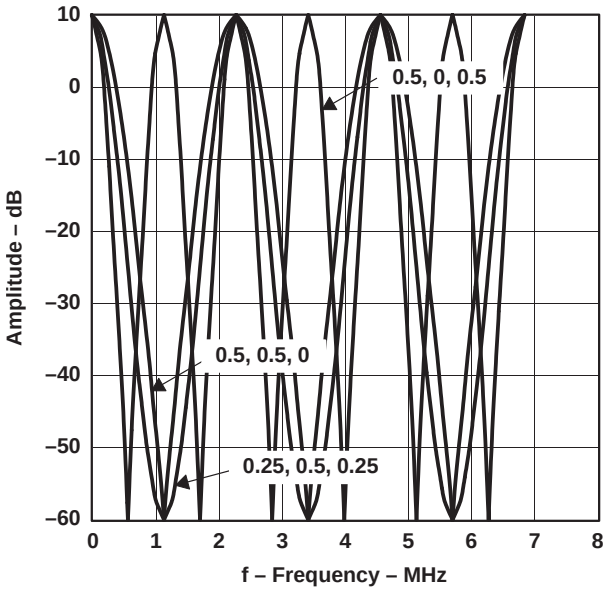


Figure 2–10. Comb Filters Frequency Response

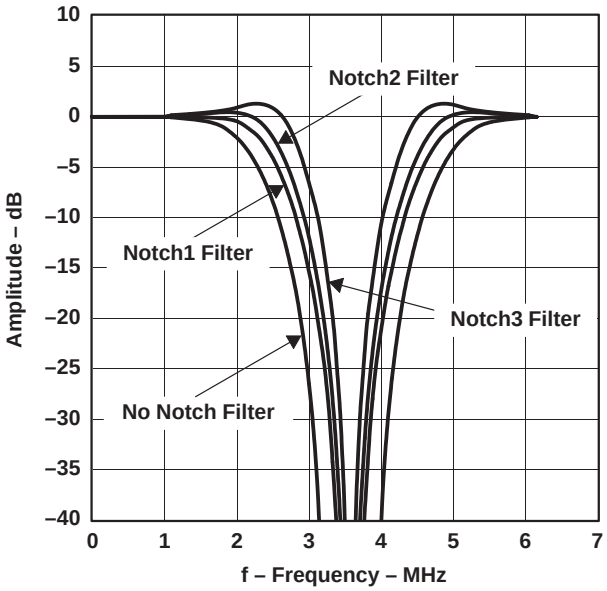


Figure 2–11. Chroma Trap Filter Frequency Response

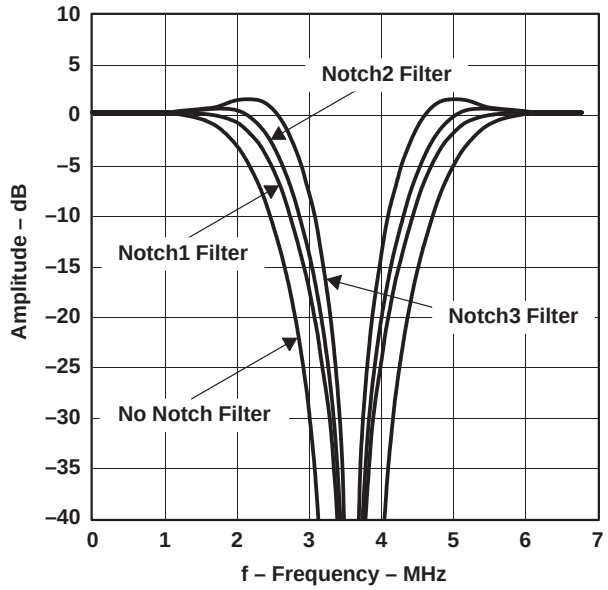


Figure 2–12. Chroma Trap Filter Frequency Response (13.5 MHz Sampling)

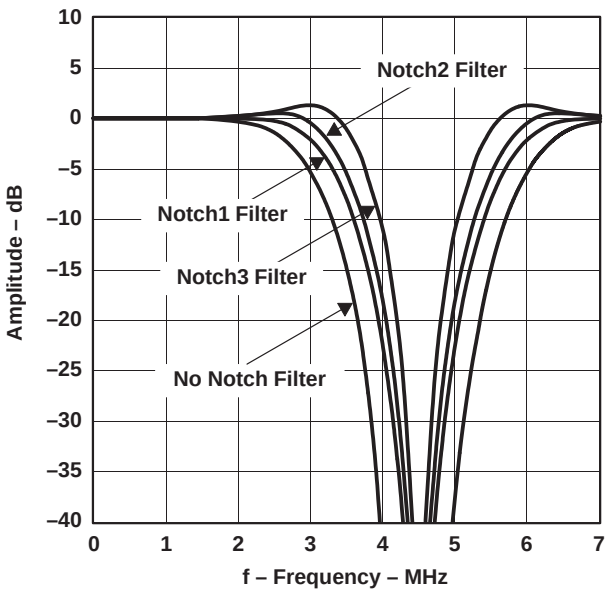


Figure 2–13. Chroma Trap Filter Frequency Response (PAL Square Pixel Sampling)

2.2.3 Luminance Processing

The digitized composite video signal passes through either a luminance comb filter or a chroma trap filter, either of which removes chrominance information from the composite signal to generate a luminance signal. The luminance signal is then fed to the input of a peaking circuit. Figure 2–14 illustrates the basic functions of the luminance data path. High frequency components of the luminance signal are enhanced by a peaking filter (edge-enhancer). Figure 2–15, Figure 2–16, and Figure 2–17 show the characteristics of the peaking filter at four different gain settings programmable via the host port.

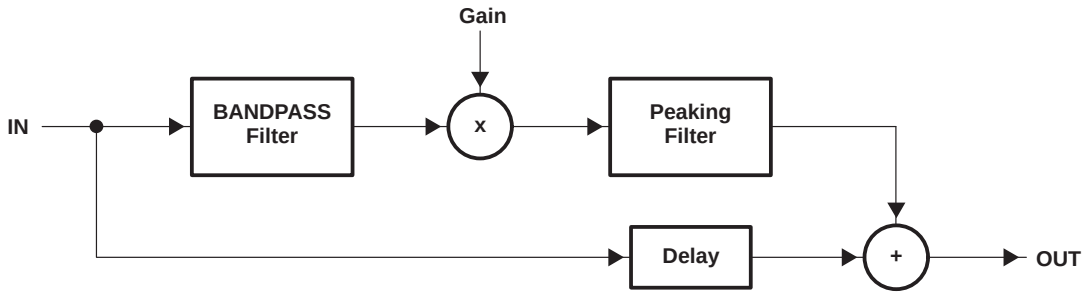


Figure 2–14. Luminance Edge-Enhancer Peaking Block Diagram

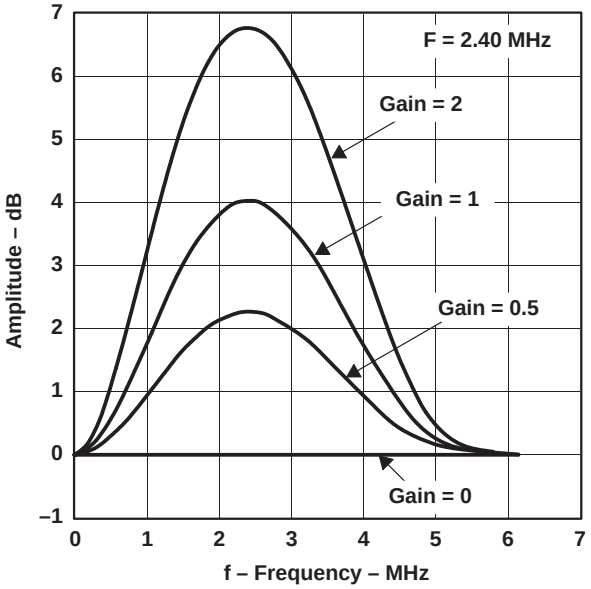


Figure 2–15. Peaking Filter Response, NTSC and PAL-M Square Pixel Sampling

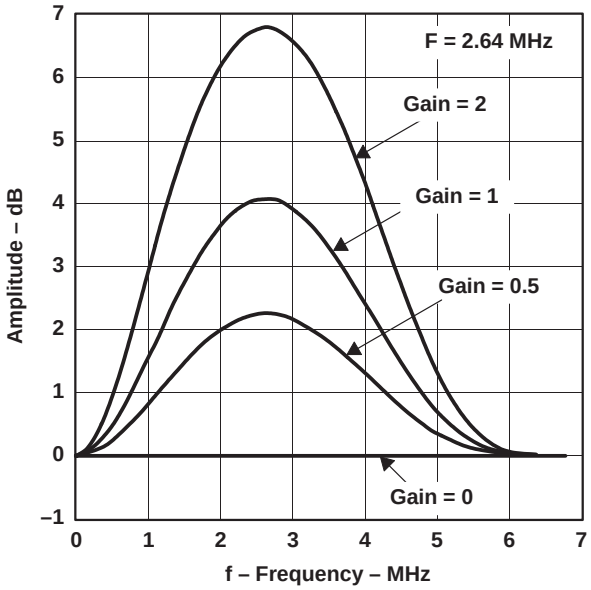


Figure 2–16. Peaking Filter Response, 13.5 MHz Sampling Rate

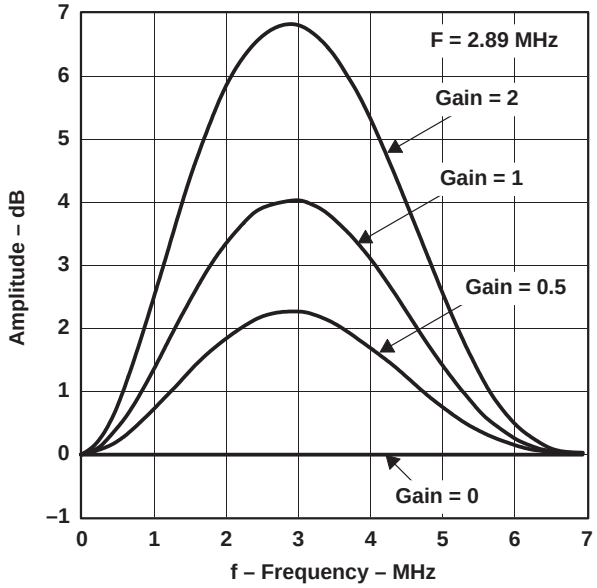


Figure 2–17. Peaking Filter Response, PAL Square Pixel

2.2.4 Chrominance Processing

A quadrature demodulator extracts U and V components from the composite signal. The U/V signals then pass through the gain control stage for chroma saturation adjustment. A comb filter is applied to both U and V to eliminate cross-chrominance noise. Hue control is achieved with phase shift of the digitally controlled oscillator. An automatic color killer (ACK) circuit is also included in this block. The ACK will suppress the chroma processing when the color burst of the video signal is weak or not present.

2.2.5 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. Figure 2–18 shows a simplified clock circuit diagram. The digital control oscillator (DCO) generates the reference signal for the horizontal PLL. A 14.318 MHz clock is required to drive the DCO. This may be input to the TVP5031 at TTL level on the XTAL1 terminal, or a crystal of 14.318 MHz fundamental resonant frequency may be connected across terminals XTAL1 and XTAL2. Figure 2–19 shows the reference clock configurations. For the example crystal circuit shown in Figure 2–19 (a parallel-resonant crystal with 14.31818 MHz fundamental frequency), the external capacitors should have the following relationship:

$$C_{L1} = C_{L2} = 2C_L - C_{stray}$$

Where C_{stray} is the terminal capacitance with respect to ground.

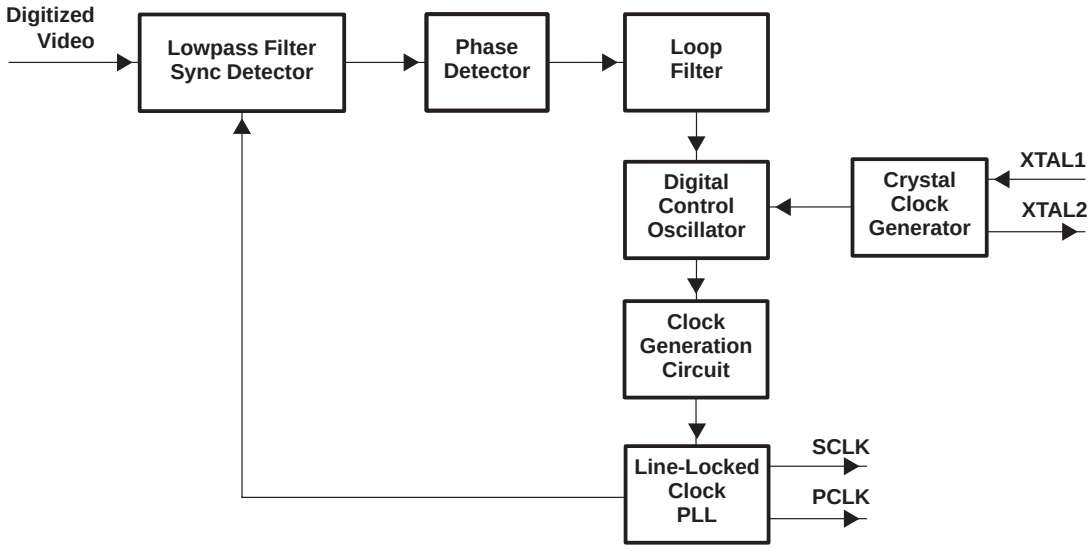


Figure 2–18. Clock Circuit Diagram

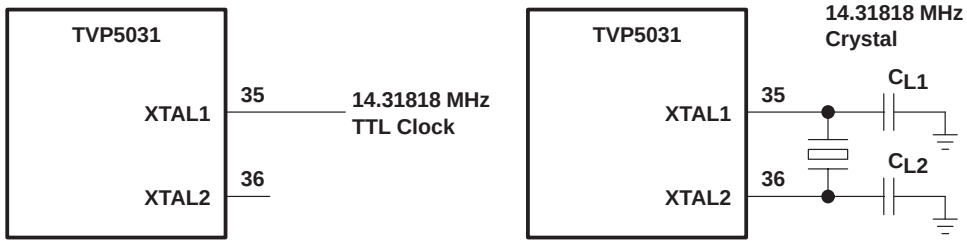


Figure 2–19. Example Reference Clock Configurations

The TVP5031 generates three signals PCLK, SCLK, and PREF used for clocking data. PCLK, the pixel clock, can be used for clocking data in the 20-bit and 16-bit 4:2:2 output formats. SCLK is twice the PCLK frequency and may be used for clocking data in the 10-bit and 8-bit 4:2:2 as well as in ITU-R BT.656 formats. PREF is used as a clock qualifier with SCLK to clock data in the 20-bit and 16-bit 4:2:2 formats.

2.3 Genlock Control

The frequency control word of the internal color subcarrier digital control oscillator (DCO) and the sub-carrier phase reset bit are transmitted via the GLCO terminal. The frequency control word is a 23-bit binary number. The frequency of the DCO can be calculated from the following equation:

$$F_{dco} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

where F_{dco} is the frequency of the DCO, F_{ctrl} is the 23-bit DCO frequency control and F_{sclk} is the frequency of the SCLK.

The last bit (bit 0) of the DCO frequency control is always 0 .

A write of 1 to bit 4 of the chrominance control register at the host port sub-address 1Ah causes the sub-carrier DTO phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 8 SCLKs after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5031 internal sub-carrier DCO is reset to zero.

A genlocking slave device can be connected to the GLCO terminal and use the information on GLCO to synchronize its internal color phase DCO to achieve clean line and color lock.

Figure 2–20 shows the timing of GLCO.

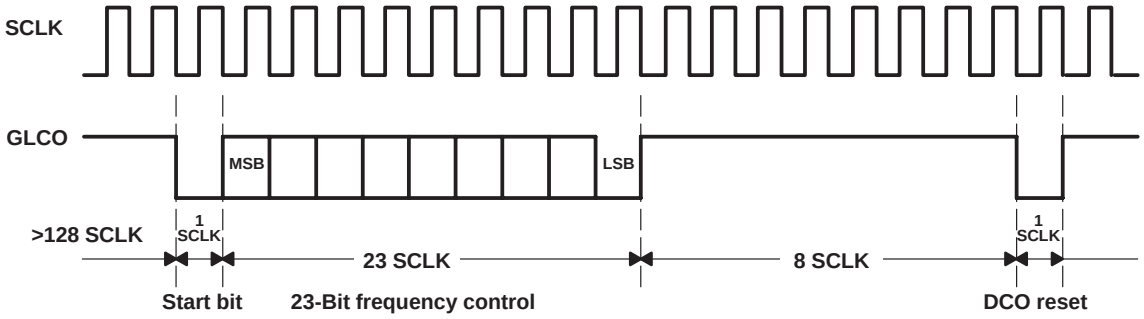


Figure 2–20. GLCO Timing

2.4 Video Output Format

The TVP5031 supports both square-pixel and ITU-R BT.601 sampling formats and multiple Y-UV output formats:

- 20-bit 4:2:2
- 16-bit 4:2:2
- 10-bit 4:2:2
- 8-bit 4:2:2
- 10-bit ITU-R BT.656
- 8-bit ITU-R BT.656

2.4.1 Sampling Frequencies and Patterns

The sampling frequencies that control the number of pixels per line differ depending on the video format and standards. Table 2–1 shows a summary of the sampling frequencies. The TVP5031 outputs data in the 4:2:2 sampling pattern. Every second sample is both a luminance and chrominance sample. The remainder are luminance-only samples.

Table 2–1. Summary of Line Frequencies, Data Rates, and Pixel Counts

STANDARDS	HORIZONTAL LINE RATE (kHz)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	PCLK FREQUENCY (MHz)	SCLK FREQUENCY (MHz)
NTSC, square-pixel	15.73426	780	640	12.2727	24.54
NTSC, ITU-R BT.601	15.73426	858	720	13.50	27.00
PAL(B,D,G,H,I), square-pixel	15.625	944	768	14.75	29.50
PAL(B,D,G,H,I),ITU-R BT.601	15.625	864	720	13.50	27.00
PAL(M),square-pixel	15.73426	780	640	12.2727	24.54
PAL(M),ITU-R BT.601	15.73426	858	720	13.50	27.00
PAL(N),square-pixel	15.625	944	768	14.75	29.50
PAL(N),ITU-R BT.601	15.625	864	720	13.50	27.00

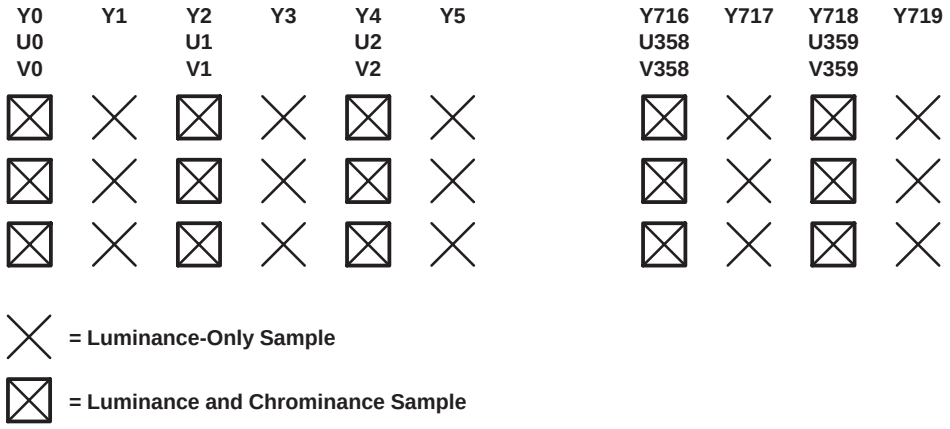


Figure 2–21. 4:2:2 Sampling

2.4.2 Video Port 20-Bit and 16-Bit 4:2:2 Output Format Timing

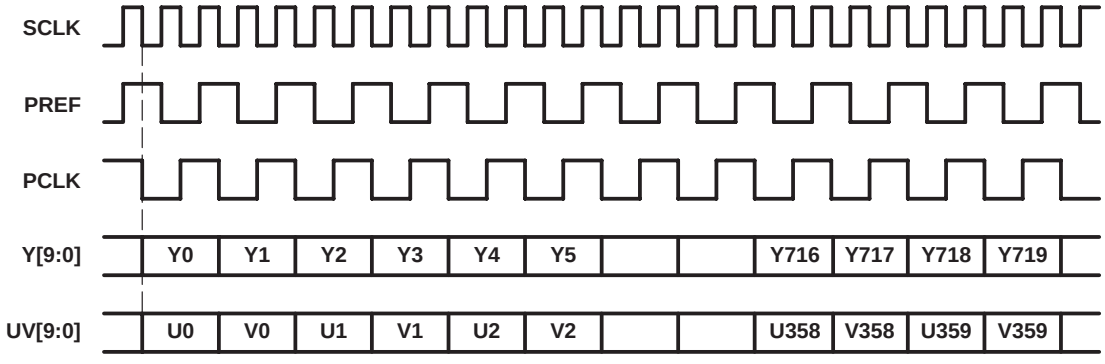
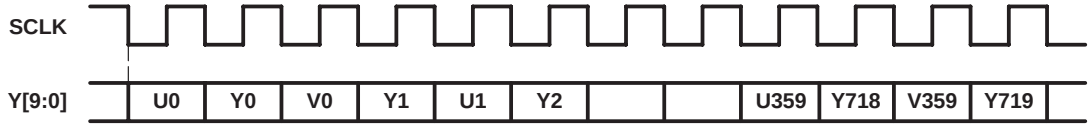


Figure 2–22. 20-Bit 4:2:2 Output Format

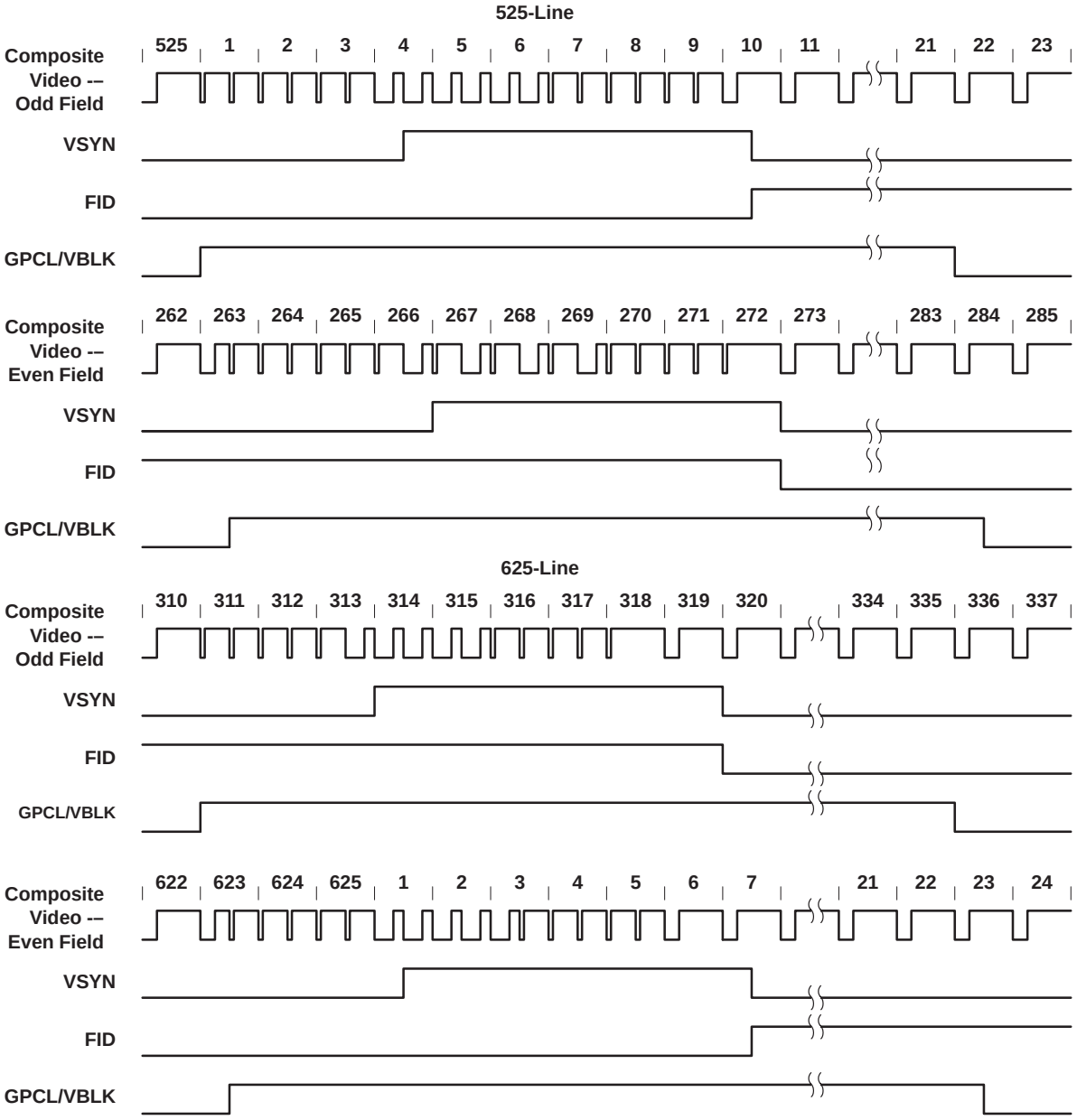
2.4.3 Video Port 10-Bit and 8-Bit 4:2:2 and ITU-R BT.656 Output Format Timing



UV[9:0] HIGH
Numbering shown is for 13.5 MHz sampling

Figure 2–23. 20-Bit 4:2:2 Output Format

2.5 Synchronization Signals



Note: Line numbering conforms to ITU-R BT-470

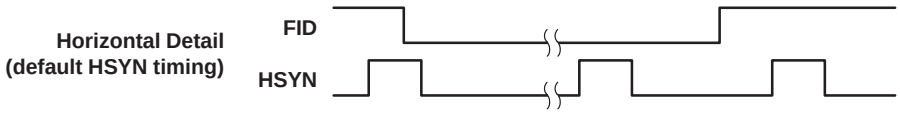


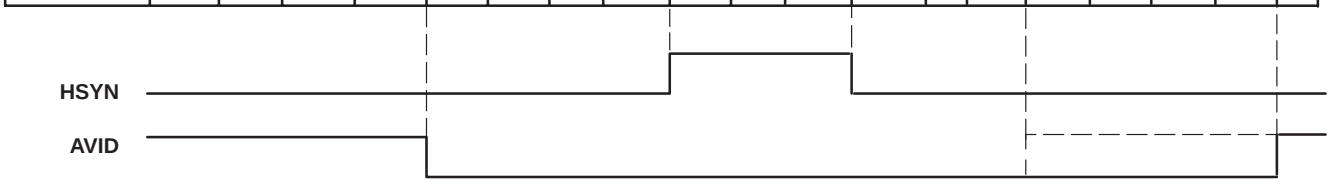
Figure 2–24. Vertical Synchronization Signals

10-bit 4:2:2 timing with 2x pixel clock (SCLK) reference. ITU-R BT.656 timing also shown

NTSC 601	1436	1437	1438	1439	1440	1441	…	1471	1472	…	1599	1600	⋯	1711	1712	1713	1714	1715	0
PAL 601	1436	1437	1438	1439	1440	1441	…	1463	1464	…	1591	1592	⋯	1723	1724	1725	1726	1727	0
ITU 656 Datastream	Cb 359	Y 718	Cr 359	Y 719	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0

NTSC sqp	1276	1277	1278	1279	1280	1281	…	1323	1324	…	1451	1452	⋯	1555	1556	1557	1558	1559	0
ITU 656 Datastream	Cb 319	Y 638	Cr 319	Y 639	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0

PAL sqp	1532	1533	1534	1535	1536	1537	…	1587	1588	…	1715	1716	⋯	1883	1884	1885	1886	1887	0
ITU 656 Datastream	Cb 383	Y 766	Cr 383	Y 767	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0



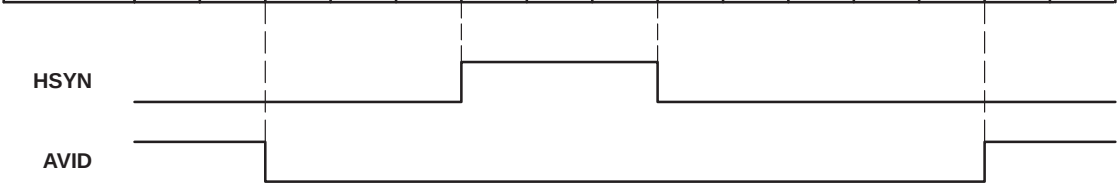
NOTE: AVID rising edge occurs 4 SCLK cycles early when in ITU656 output mode

(A)

The HSYN timing shown is valid when HSYN start (register 16/17) is set to its default value of 80h.

20-bit 4:2:2 timing with 1x pixel clock (PCLK) reference.

NTSC 601	718	719	720	…	735	736	…	799	800	…	855	856	857	0	1
PAL 601	718	719	720	…	731	732	…	795	796	…	861	862	863	0	1
NTSC sqp	638	639	640	…	661	662	…	725	726	…	777	778	779	0	1
PAL sqp	766	767	768	…	793	794	…	857	858	…	941	942	943	0	1



(B)

The HSYN timing shown is valid when HSYN start (register 16/17) is set to its default value of 80h.

Figure 2–25. Horizontal Synchronization Signals

2.6 Host Interface

The host interface is used to initialize the internal microprocessor, to read and write status registers and control registers, and to access sliced VBI data.

The interface modes supported by the TVP5031 are I^2C, and three parallel interface modes. The host interface is configured at powerup and reset using the GLCO, PALI, and the FID terminals as shown in Table 2–2.

Table 2–2. Host Port Mode Select

INTERFACE CONFIGURATION	TERMINALS		
	GLCO	PALI	FID
I^2C	0	0	1
Parallel A	1	0	1
Parallel B	1	1	0
Parallel C	1	1	1

NOTE: 1 = pullup 0 = pulldown

2.6.1 I^2C Host Interface

The TVP5031 host interface is configured for I^2C operation by attaching external pullup and pulldown resistors to the GLCO, PALI, and FID terminals. The following is the combination of resistors required to select I^2C host mode (1 is pullup and 0 is pulldown).

	GLCO	PALI	FID
I^2C host port enabled	0	0	1

2.6.1.1 I^2C Host Port Select

The I^2C standard consists of two signals, serial input/output data line (VC1) and input/output clock line (VC0), which carry information between the devices connected to the bus. A third signal (VC3) is used for slave address selection. Although the I^2C system can be multi-mastered, the TVP5031 will function as a slave device only.

Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull up resistor. When the bus is free, both lines are high.

The slave address select terminal (VC3) enables the use of two TVP5031 devices tied to the same I^2C bus.

Table 2–3 summarizes the terminal functions of the I2C-mode host interface.

Table 2–3. I2C Host Port Terminal Description

SIGNAL	TYPE	DESCRIPTION
VC3 (I2CA)	I	Slave address selection
VC0 (SCL)	I/O (open drain)	Input/output clock line
VC1 (SDA)	I/O (open drain)	Input/output data line

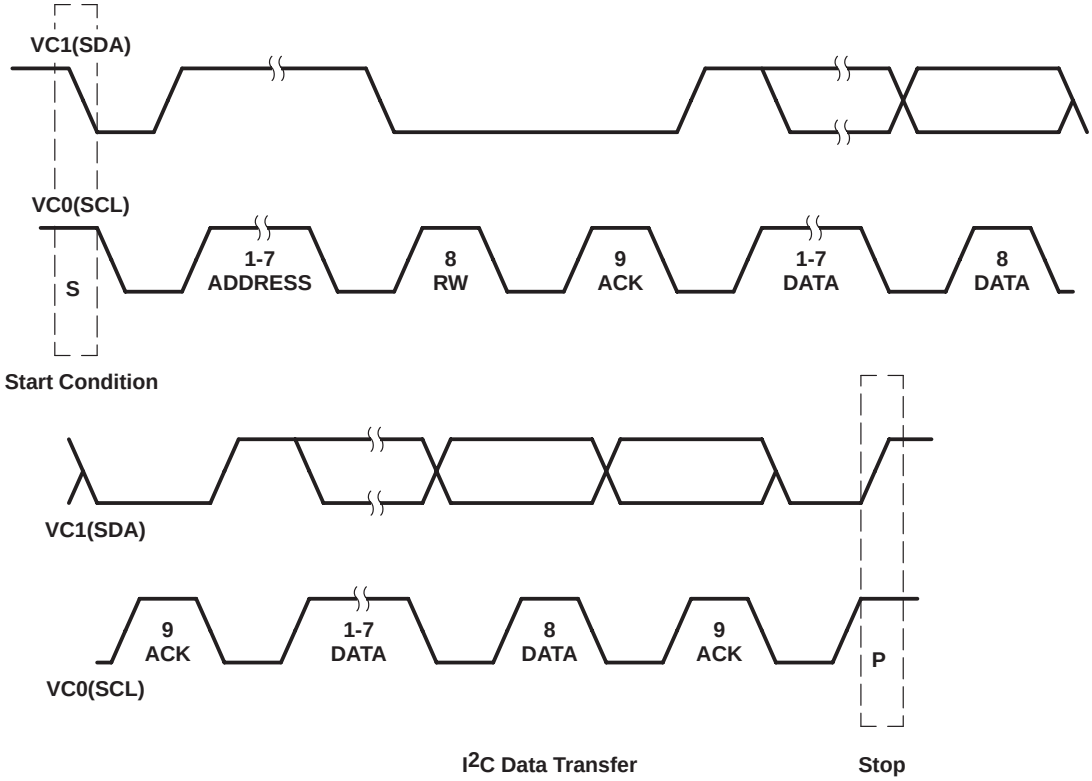


Figure 2–26. I2C Data Transfer Example

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change with the clock signal on the SCL line being low.

- If multiple bytes are transferred during one read or write operation, the internal subaddress is automatically incremented.
- A high to low transition on the SDA line while the SCL is high indicates a start condition.
- A low to high transition on the SDA line while the SCL is high indicates a stop condition.
- Acknowledge (SDA Low)
- Not-Acknowledge (SDA High)

Every byte placed on the SDA line must be 8-bits long. The number of bytes which can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. If the slave cannot receive another complete byte of data until it has performed another function, it can hold the clock line (SCL) low to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and release the clock line (SCL).

Data transfer with acknowledge is obligatory. The acknowledge related clock pulse is generated by the master. The master releases the SDA line high during the acknowledge clock pulse. The slave must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

When a slave does not acknowledge the slave address, the data line must be left high by the slave. The master can then generate a stop condition to abort the transfer.

If a slave does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line high and the master generates the stop condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a stop or repeated start condition.

2.6.1.2 I2C Write Operation

Data transfers occur utilizing the following illustrated formats.

An I2C master initiates a write operation to TVP5031 by generating a start condition followed by TVP5031s I2C address 101110X , the X in the TVP5031 address is 0 when VC3 terminal is tied low and is 1 when VC3 terminal is tied high, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from TVP5031, the master presents the subaddress of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. TVP5031 acknowledges each byte after completion of each transfer. The I2C master terminates the write operation by generating a stop condition.

STEP 1	**0**
I2C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I2C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Write register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

STEP 5	**9**
I2C Acknowledge (slave)	A

STEP 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 7†	**9**
I2C Acknowledge (slave)	A

† Repeat steps 6 and 7 until all data has been written

STEP 8	**0**
I2C Stop (master)	P

2.6.1.3 I2C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I2C master initiates a write operation to TVP5031 by generating a start condition followed by TVP5031s I2C address 101110X, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledge from TVP5031, the master presents the subaddress of the register, or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition. The second phase is the data phase. In this phase, a I2C master initiates a read operation to TVP5031 by generating a start condition followed

by TVP5031s I2C address 101110X, in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from TVP5031, the I2C master receives one or more bytes of data from TVP5031. The I2C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5031 to the master, the master generates a not acknowledge followed by a stop.

2.6.1.4 Read Phase 1:

STEP 1	**0**
I2C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I2C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Read register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

STEP 5	**9**
I2C Acknowledge (slave)	A

STEP 6	**0**
I2C Stop (master)	P

2.6.1.5 Read Phase 2:

STEP 7	**0**
I2C Start (master)	S

STEP 8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	1

STEP 9	**9**
I2C Acknowledge (slave)	A

STEP 10	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 11‡	**8**
I2C Acknowledge (master)	A

‡ Repeat steps 10 and 11 for all but the last byte read

STEP 12	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 13	**9**
I2C Not acknowledge (master)	$\overline{A}$

STEP 14	**0**
I2C Stop (master)	P

2.6.1.6 I2C Microcode Write Operation

Data written during the micro-code write operation will be written to the TVP5031 program RAM. During the write cycle the microprocessor will reset and point to location zero in the program and will remain reset. Upon completion of the write operation, a microprocessor clear-reset operation is required. This is performed by writing into the 7F register to clear reset and resume microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume the microprocessor function.)

STEP 1	**0**
I2C Start (master)	S

STEP 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	**9**
I2C Acknowledge (slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Write register address (master)	0	1	1	1	1	1	1	0

Write to program RAM address=7E

STEP 5	**9**
I2C Acknowledge (slave)	A

STEP 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 7§	**9**
I2C Acknowledge (slave)	A

§ Repeat steps 6 and 7 until all data has been written.

STEP 8	**0**
I2C Stop (master)	P

2.6.1.7 Microprocessor Clear Reset

	0
I2C Start (master)	S

	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	0

	9
I2C Acknowledge (slave)	A

	7	6	5	4	3	2	1	0
I2C Write register address (master)	0	1	1	1	1	1	1	1

Write to microprocessor clear reset address=7F

	9
I2C Acknowledge (slave)	A

	7	6	5	4	3	2	1	0
I2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Any data written to 7F will start the microprocessor.

	9
I2C Acknowledge (slave)	A

	0
I2C Stop (master)	P

2.6.1.8 I2C Microcode Read Operation

Data read during the microcode write operation will be read from the TVP5031 program RAM. During the read cycle the microprocessor will reset and point to location zero in the program and will remain reset. Upon completion of the read operation, a microprocessor clear-reset operation is required. This is performed by writing into the 7F register to clear reset and resume the microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume microprocessor function.)

STEP 1	0
I2C Start (master)	S

STEP 2	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	0

STEP 3	9
I2C Acknowledge (slave)	A

STEP 4	7	6	5	4	3	2	1	0
I2C Read register address (master)	1	0	0	0	1	1	1	0

Read address=8E

STEP 5	9
I2C Acknowledge (slave)	A

STEP 6	0
I2C Stop (master)	P

2.6.1.9 Read Phase 2:

STEP 7	0
I2C Start (master)	S

STEP 8	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	1

STEP 9	7
I2C Acknowledge (slave)	A

STEP 10	7	6	5	4	3	2	1	0
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 11	7
I2C Acknowledge (master)	A

Repeat STEP 10 and STEP 11 for all but the last byte read from program RAM.

STEP 12	7	6	5	4	3	2	1	0
I2C Read Data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

STEP 13	9
I2C Not acknowledge (master)	$\overline{A}$

STEP 14	0
I2C Stop (master)	P

2.6.2 Parallel Host Interface A

Parallel host interface A is compatible with Video Electronics Standards Association (VESA) Video Module Interface (VMI) proposal version 1.4 mode A. The terminal descriptions are defined in Table 2–4.

Table 2–4. Parallel Host Interface A Terminal Description

TERMINAL	SIGNAL	TYPE	DESCRIPTION
A[1:0]	HA[1:0]	I	Address bus from host
D[7:0]	HD[7:0]	I/O	Bidirectional data bus
VC3	$\overline{CS}$	I	Chip select, active low
VC2	$\overline{DS}$	I	Data strobe, active low
VC1	RD/$\overline{WR}$	I	Read, active high Write, active low
VC0	$\overline{DTACK}$	O	Data acknowledge
INTREQ	INTREQ	O	Interrupt request, Open drain by default, active low, pullup resistor required Can be configured, subaddress C2, as a conventional CMOS buffer, active high, no pullup required.

Parallel host interface A timing is shown in Figure 2–27. The cycle is initiated by the host when VC2-DS transitions low. The TVP5031 responds by pulling VC0-DTACK low to indicate data has been received or that the requested data is present on the bus. The host then completes the cycle by pulling VC2-DS high. Once the host has completed the cycle, the TVP5031 sets VC0-DTACK to high impedance. A pullup is required to pull VC0-DTACK high to indicate the operation is complete.

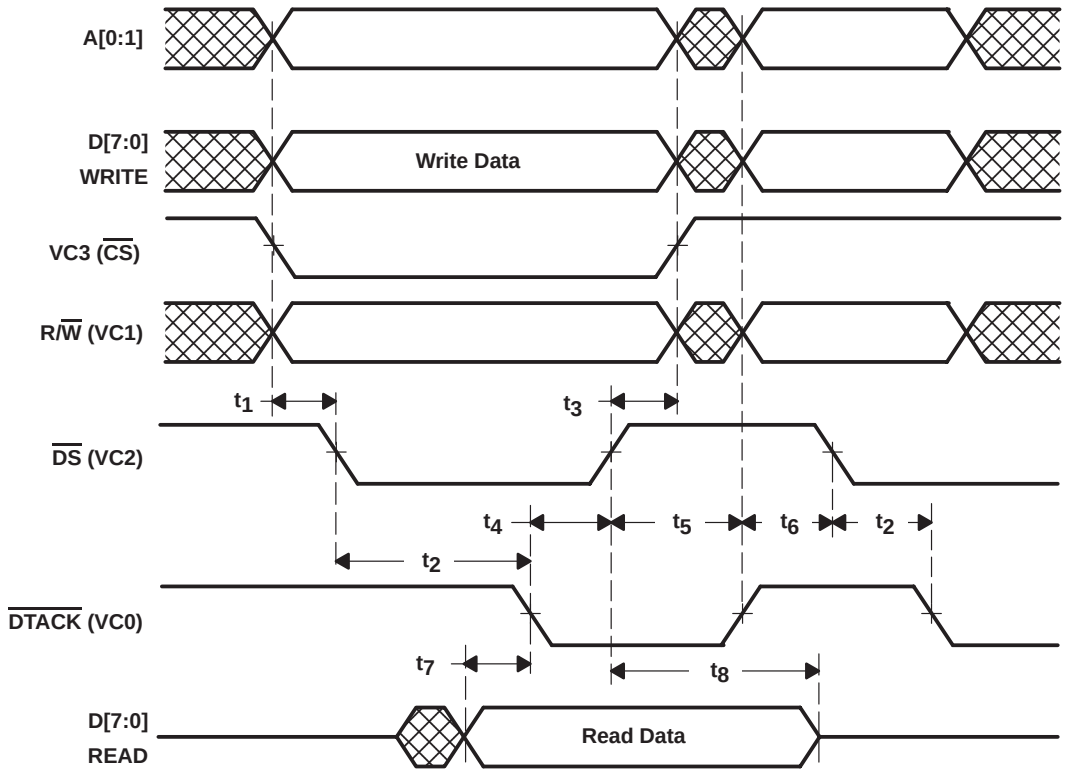


Figure 2–27. Parallel Host Interface A Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	A[1:0],D[0:7],VC1 setup until VC2 low		5			ns
t_2	Delay VC0 low after VC2 low		0			ns
t_3	A[1:0], D[0:7],VC1 hold after VC0 low		5			ns
t_5	Delay VC0 high after VC2 high		0			ns
t_6	Delay VC2 low(next cycle) after VC0 high		5			ns
t_8	(Read cycle) D[7:0] setup until VC0 low		10			ns

2.6.3 Parallel Host Interface B

Parallel host interface B is compatible with Video Electronics Standards Association (VESA) Video Module Interface (VMI) proposal version 1.4 mode B. The terminal descriptions are defined in Table 2–5.

Table 2–5. Parallel Host Interface B Terminal Description

TERMINAL	SIGNAL	TYPE	DESCRIPTION
A[1:0]	HA[1:0]	I	Address bus from host
D[7:0]	HD[7:0]	I/O	Bidirectional data bus
VC3	$\overline{CS}$	I	Chip select, active low
VC2	$\overline{RD}$	I	Read, active low
VC1	WR	I	Write, active high
VC0	RDY	O	Data acknowledge
INTREQ		O	Interrupt request, Open drain by default, active low, pullup resistor required Can be configured, subaddress C2, as a conventional CMOS buffer, active high, no pullup required.

Parallel host interface B timing is shown in Figure 2–28. The cycle is initiated by the host when VC2-$\overline{RD}$ OR VC1-$\overline{WR}$ transitions low. The TVP5031 responds by pulling VC0-RDY low. The TVP5031 will then set VC0-RDY to high impedance, a pullup resistor is required, to indicate the data was received or that the requested data is present on the bus. The host then completes the cycle by pulling the asserted signal, VC2-$\overline{RD}$ or VC1-$\overline{WR}$ high.

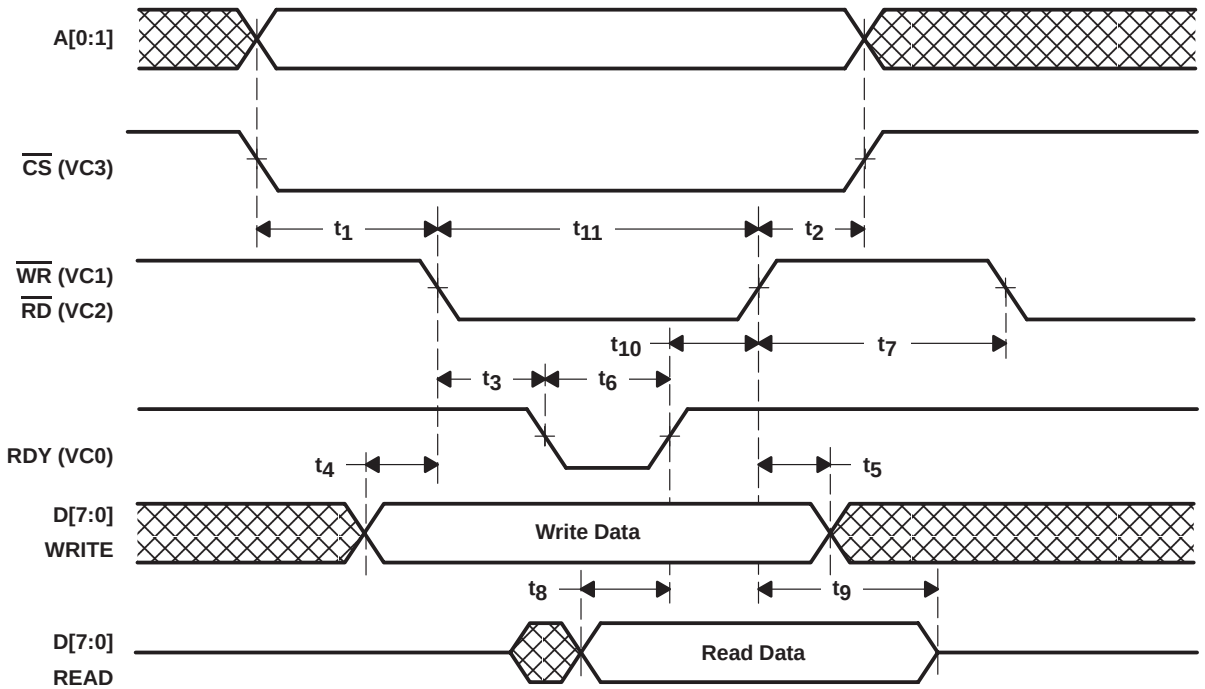


Figure 2–28. Parallel Host Interface B Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Delay VC1 or VC2 active after valid A[1:0]		10			ns
t_2	A[1:0] hold after VC1 or VC2 inactive		10			ns
t_3	Delay VC0 low after VC1 or VC2 active				28	ns
t_4	D[7:0] setup until VC1 active		5			ns
t_5	D[7:0] hold after VC1 inactive		10			ns
t_6	VC0 inactive pulse width		10			ns
t_7	VC1 inactive until any command active		80			ns
t_8	(Read cycle) VC1 low until D[7:0] non 3-state		5			ns
t_9	(Read cycle) D[7:0] setup until VC0 inactive		0			ns
t_{10}	(Read cycle) D[7:0] hold after VC1 inactive		0		15	ns
t_{11}	Hold VC1 active after VC0 active		0			ns

2.6.4 Parallel Host Interface C

The terminal descriptions are defined in Table 2–6.

Table 2–6. Parallel Host Interface C Terminal Description

TERMINAL	SIGNAL	TYPE	DESCRIPTION
A[1:0]	HA[1:0]	I	Address bus from host
D[7:0]	HD[7:0]	I/O	Bidirectional data bus
VC3	$\overline{CS}$	I	Chip select, active low
VC2	$\overline{DS}$	I	Data strobe, active low
VC1	RD/$\overline{WR}$	I	Read, active high Write, active low
VC0	$\overline{RDY}$	O	Ready, active high
INTREQ		O	Interrupt request, Open drain by default, active low, pullup resistor required Can be configured, subaddress C2, as a conventional CMOS buffer, active high, no pullup required.

Parallel host interface C timing is shown in Figure 2–29. The cycle is initiated by the host when VC2-$\overline{DS}$ transitions low. The TVP5031 responds by pulling VC0-RDY low. The TVP5031 will then set VC0-RDY to high impedance, a pullup resistor is required, to indicate the data was received or that the requested data is present on the bus. The host then completes the cycle by pulling VC2-$\overline{DS}$ high.

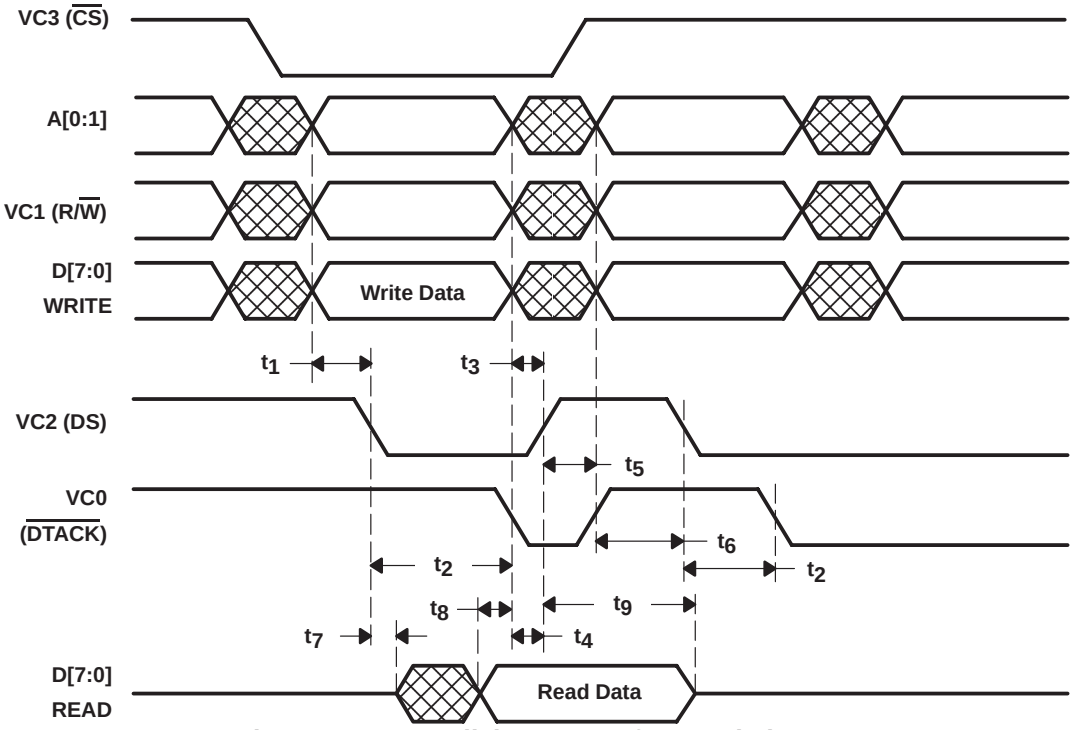


Figure 2–29. Parallel Host Interface C Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	A[1:0],D[0:7],VC1 setup until VC2 low		5			ns
t_2	Delay VC0 LOW after VC2 low		0			ns
t_3	A[1:0], D[0:7],VC1 hold after VC0 low		5			ns
t_5	Delay VC0 high after VC2 high		0			ns
t_6	Delay VC2 low(next cycle) after VC0 high		5			ns
t_8	(Read cycle) D[7:0] setup until VC0 low		10			ns
t_9	(Read cycle) D[7:0] hold after VC2 high		0			ns

2.6.5 Parallel Host Interface Register Map

The parallel host interface (PHI) module contains only four registers that are directly accessible to the host (see Figure 2–30). The address register holds an indirect address for internal register access. When the host accesses the data register the PHI module reads or writes the internal register selected by the indirect address register. Two other registers are provided for direct access. The FIFO register provides direct access to the VBI FIFO. The other direct access register is the status/Interrupt register. This register contains the state of the interrupt sources.

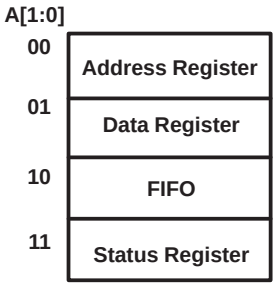


Figure 2–30. PHI Address Register Map

Normally read or write operations require two accesses. To read the FIFO register, set A[1:0] to 2'b10 and perform a read cycle. The FIFO read data will be placed on the D[7:0] bus. To read/write the status/interrupt register, set A[1:0] to 2'b11 and perform the read/write cycle. The read/write data will be appropriately muxed to/from the external data bus.

Indirect register read/write

All PHI accesses except for the VBI FIFO and the status/interrupt register require a two-step operation. To access an indirect register the desired internal address must first be written to the address register of the PHI. This is done by setting A[1:0] to 00 and performing a write cycle with D[7:0] = indirect register address. To write to an indirect register, the second step consists of writing the desired data to PHI address 01. To read an indirect register, the second step consists of reading the requested data from address 01.

Read Indirect Register

Step 1	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write register address	0	0	Register address							

Step 2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Read register data	0	1	Data from register							

Write Indirect Register

Step 1	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write register address	0	0	Register address							

Step 2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Read register data	0	1	Data to register							

Latency

PHI accesses to indirect addresses 00-8F require special consideration due to response latencies of up to 64 μs for these addresses. Latency occurs between steps 1 and 2 for a read operation, and following step 2 for a write operation. To avoid violating PHI cycle time requirements the host can poll the cycle complete bit in the PHI status register following step 1 for a read or step 2 for a write. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1) can be set to generate an interrupt for the host when an access has been completed.

PHI accesses to indirect addresses 90-CF occur with minimal latency and interrupts will not be generated for the completion of access cycles to these addresses.

VBI FIFO

The VBI FIFO containing sliced VBI data can be read directly by the PHI host.

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Read VBI FIFO	1	0	Data from FIFO							

Status/Interrupt Register

The status/interrupt register provides the host with information regarding the source of an interrupt. After an interrupt condition is set it can be reset by writing a 1 to the appropriate bit in the status/interrupt register. Section 2.14 contains a description of the PHI status/interrupt register.

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Access status/interrupt register	1	1	Data from status/interrupt register							

2.6.6 Parallel Host Interface Microcode Write Operation

Data written to indirect register 7E will be written to the TVP5031 program RAM. During the write cycle the microprocessor will reset and point to location zero in the program and will remain reset. Upon completion of the write operation, a microprocessor clear-reset operation is required. This is performed by writing into the 7F register to clear reset and resume microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume microprocessor function.)

To avoid violating PHI cycle time requirements during a microcode write operation the host can poll the cycle complete bit in the PHI status register after writing each byte data to the PHI data register. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1) can be set to generate an interrupt for the host when a write has been completed.

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write microcode register address	0	0	0	1	1	1	1	1	1	0

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write microcode register data	0	1	First byte of microcode data (Wait for cycle complete status or interrupt.)							
Write microcode register data	0	1	Second byte of microcode data (Wait for cycle complete status or interrupt.)							
Write microcode register data	0	1	Last byte of microcode data (Wait for cycle complete status or interrupt.)							

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write clear reset dummy data	0	1	Dummy data							

2.6.7 Parallel Host Interface Microcode Read Operation

Data read from indirect register 8E will be read from the TVP5031 program RAM. During the read cycle the microprocessor will reset and point to location zero in the program and will remain reset. Upon completion of the read operation, a microprocessor clear-reset operation is required. This is performed by writing into the 7F register to clear reset and resume microprocessor function. (There is no specific data requirement to be written into the 7F register, any data will resume microprocessor function.)

To avoid violating PHI cycle time requirements during a microcode read operation the host can poll the cycle complete bit in the PHI status register after writing to the PHI address register. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1) can be set to generate an interrupt for the host when the read data is available in the PHI data register.

Step 1	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write program RAM read address	0	0	1	0	0	0	1	1	1	0
	(Wait for cycle complete status or interrupt)									

Step 2	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Read program RAM read data	0	1	data							

NOTE: Repeat Steps 1 and 2 until all program RAM data has been read.

Step 3	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write reset clear register address	0	0	0	1	1	1	1	1	1	1

Step 4	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Write reset clear register data	0	1	X	X	X	X	X	X	X	X
	(Wait for cycle complete status or interrupt)									

2.7 VBI Data Processor

The TVP5031 VBI data processor slices, parses, and performs error checking on teletext data contained in the vertical blanking interval or during active lines. Teletext formats supported are North American Basic Teletext Specification (NABTS) equivalent to ITU-R BT.653 system C, and World System Teletext (WST) equivalent to ITU-R BT.653 system B. Data is stored in an internal FIFO and may be read via the host port or transmitted as ancillary data in the digital video stream in BT.656 mode. The VBI data FIFO holds up to 14 lines of NABTS or 11 lines of WST data. Interrupts generated by the VBI data processor are configurable to enable host synchronization for retrieval of full-field teletext data.

Closed caption data may also be sliced by the VBI data processor and is stored in a register accessible via the host port.

2.7.1 Teletext Data Byte Order

Table 2–7 shows the order in which teletext data is read from the FIFO.

Table 2–7. Teletext Data Byte Order

BYTE NUMBER	NABTS - 525 LINE SYSTEM	WST - 625 LINE SYSTEM
1	Video Line [7:0]	Video Line [7:0]
2	00, Hamming Error, Parity Error, LPC Error, Match number 2, Match number 1, Video Line [8]	00, Hamming Error, Parity Error, 0, Match number 2, Match number 1, Video Line [8]
3	Packet address 1	Magazine
4	Packet address 2	Row address
5	Packet address 3	Data byte 1
6	Continuity index	Data byte 2
7	Packet structure	Data byte 3
8	Data block 1	Data byte 4
9	Data block 2	Data byte 5
10	Data block 3	Data byte 6
11	Data block 4	Data byte 7
12	Data block 5	Data byte 8
13	Data block 6	Data byte 9
14	Data block 7	Data byte 10
15	Data block 8	Data byte 11
16	Data block 9	Data byte 12
17	Data block 10	Data byte 13
18	Data block 11	Data byte 14
19	Data block 12	Data byte 15
20	Data block 13	Data byte 16
21	Data block 14	Data byte 17
22	Data block 15	Data byte 18
23	Data block 16	Data byte 19
24	Data block 17	Data byte 20
25	Data block 18	Data byte 21
26	Data block 19	Data byte 22
27	Data block 20	Data byte 23
28	Data block 21	Data byte 24
29	Data block 22	Data byte 25
30	Data block 23	Data byte 26
31	Data block 24	Data byte 27
32	Data block 25	Data byte 28
33	Data block 26	Data byte 29
34	Data block 27 / suffix	Data byte 30
35	Data block 28 / suffix	Data byte 31
36	Padding byte†	Data byte 32
37		Data byte 33
38		Data byte 34
39		Data byte 35
40		Data byte 36
41		Data byte 37
42		Data byte 38
43		Data byte 39
44		Data byte 40

† The padding byte is used to ensure an even number of writes. This byte does not contain any useful information. The read pointer automatically advances past this byte so the user does not have to read the padding byte.

2.7.2 Teletext as Ancillary Data in Video Stream

Sliced teletext data can be output as ancillary data in the video stream in ITU-R BT.656 mode. Teletext data is output on the Y[7:0] terminals during the horizontal blanking period following the line from which the data was retrieved. Dummy ancillary data blocks with special timing header information are inserted during certain horizontal blanking periods to provide data synchronization information. Table 2–8 and Table 2–9 show the format and sequence of the ancillary data inserted into the video stream.

Table 2–8. NABTS 525-Line Ancillary Data Sequence

BYTE NO.	MSB 7	6	5	4	3	2	1	LSB 0	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data preamble
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID
5	1	0	0	0	0	0	0	0	Secondary data ID
6	1	0	0	0	1	0	0	1	Number of 32-bit data words
7	Video line number 7:0								Internal data ID
8	0	0	Hamming error	Parity error	LPC error	Match 2	Match 1	Video line 8	
9	Packet address 1								Data byte
10	Packet address 2								Data byte
11	Packet address 3								Data byte
12	Continuity index								Data byte
13	Packet structure								Data byte
14	Teletext data 1								Data byte
15	Teletext data 2								Data byte
39	Teletext data 26								Data byte
40	Teletext data 27/suffix								Data byte
41	Teletext data 28/suffix								Data byte
42	NEP	EP	Checksum						Checksum
43	1	0	0	0	0	0	0	0	Fill byte
44	1	0	0	0	0	0	0	0	Fill byte

Table 2–9. Dummy Timing Ancillary Data Sequence

BYTE NO.	MSB 7	6	5	4	3	2	1	LSB 0	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data preamble
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID
5	1	0	0	0	0	0	0	0	Secondary data ID
6	1	0	0	0	0	0	0	0	Number of 32-bit data words

In the tables above, EP is even parity on the lower 6 bits and NEP is negated even parity. The checksum for teletext data blocks is the 6 LSBs of the sum of the data bytes. The data ID byte provides timing information. Table 2–10 shows the possible values of the data ID byte and their meanings.

Table 2–10. Data ID

DATA ID	EVENT IN SOURCE STREAM	DATA TYPE
50	Start of first, odd field	Dummy timing block
91	Sliced data of lines 1-23 of first field	VBI data
92	End of nominal VBI of first field, line 23	Dummy timing block
53	Sliced data of line 24 to end of first field	Full field teletext data
94	Start of second, even field	Dummy timing block
55	Sliced data of lines 1-23 of second field	VBI data
56	End of nominal VBI of second field, line 23	Dummy timing block
97	Sliced data of line 24 to end of second field	Full field teletext data

A dummy timing block will be inserted into the video stream during the horizontal blanking period following line 23 of each field. If teletext data is available from line 23 it will be inserted into the video stream prior to the dummy timing block.

2.8 Raw Video Data Output

The TVP5031 can output raw A/D samples in the ITU-656 VBI video stream if desired in order to process VBI data externally. The data occurs at the 2x pixel rate. The data is preceded by a preamble sequence of 00, FF, FF, 60. The preamble sequence occurs immediately following the start of active video (SAV) sequence.

2.9 Reset and Initialization

Reset is initiated at power up or any time the RSTINB terminal is brought low. Table 2–11 describes the status of the TVP5031s terminals during and immediately after reset. Following a power up reset, the host must download microcode to the TVP5031s program memory for use by the internal microprocessor.

Table 2–11. Reset Sequence

SIGNAL NAMES	DURING RESET	RESET COMPLETED
Y[9:0], UV[9:0], HSYN, VSYN, FID, PALI	Input	High-impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.
AVID	Input	High-impedance if AVID is pulled down during reset. Active output if AVID is pulled up during reset.
SCLK, PCLK	High-impedance if PREF is pulled down during reset. Active if PREF is pulled up during reset.	Active output
PREF	Input	Active output
GLCO	Input	Active output
VC0	High impedance	High impedance
D[7:0]	Input	High impedance
A[1:0] in PHI mode	Input	Input
RSTINB, SDA, SCL, I2CA, OEB, GPCL	Input	Input

2.10 Internal Control Registers

The TVP5031 is initialized and controlled by a set of internal registers which set all the device operating parameters. Communication between and the external controller and TVP5031 is through a standard the host port interface port. Table 2–12 shows the summary of these registers. The reserved bits must be written with 0. The detailed programming information of each register is described in the following sections.

Table 2–12. Registers Summary

REGISTER FUNCTION	PHI	I2C	R/W
Video input source selection 1	00 ← 00	**00h**	R†/W
Analog channel controls	00 ← 01	**01h**	R†/W
Operation mode controls	00 ← 02	**02h**	R†/W
Miscellaneous controls	00 ← 03	**03h**	R†/W
Reserved	00 ← 04-05	**04-05h**	R†/W
Color killer threshold control	00 ← 06	**06h**	R†/W
Luminance processing control 1	00 ← 07	**07h**	R†/W
Luminance processing control 2	00 ← 08	**08h**	R†/W
Brightness control	00 ← 09	**09h**	R†/W
Color saturation control	00 ← 0A	**0Ah**	R†/W
Color hue control	00 ← 0B	**0Bh**	R†/W
Contrast control	00 ← 0C	**0Ch**	R†/W
Outputs and data rate select	00 ← 0D	**0Dh**	R†/W
Luminance processing control 3	00 ← 0E	**0Eh**	R†/W
Reserved	00 ← 0F-15	**0F-15h**	R†/W
Horizontal sync start NTSC	00 ← 16	**16h**	R†/W
Horizontal sync start PAL	00 ← 17	**17h**	R†/W
Vertical blanking start	00 ← 18	**18h**	R†/W
Vertical blanking stop	00 ← 19	**19h**	R†/W
Chroma processing control 1	00 ← 1A	**1Ah**	R†/W
Chroma processing control 2	00 ← 1B	**1Bh**	R†/W
Interrupt reset B	00←1C	**1Ch**	R†/W
Interrupt enable B	00←1D	**1Dh**	R†/W
Interrupt configuration B	00←1E	**1Eh**	R†/W
Reserved	00 ← F1–7D	**1F-7Dh**	R†/W
Program RAM write	00 ← 7E	**7E**	W
Microprocessor reset clear	00 ← 7F	**7Fh**	W
Major software revision	00 ← 80	**80h**	R
Status 1	00 ← 81	**81h**	R
Status 2	00 ← 82	**82h**	R
Status 3	00 ← 83	**83h**	R
Status 4	00 ← 84	**84h**	R
Interrupt status B	00 ← 85	**85h**	R
Interrupt B active	00 ← 86	**86h**	R

NOTE: R = Read only for all interfaces
W = Write only for all interfaces
R/W = Read and write for all host interfaces
R†/W = Read and write for I^2C host interface. Write only for PHI host interfaces.

Table 2–12. Registers Summary (Continued)

REGISTER FUNCTION	PHI	I2C	R/W
Minor software revision	00 ← 87	**87h**	R
Status 5	00 ← 88	**88h**	R
Reserved	00 ← 86-8F	**86-8Fh**	
Program RAM read	00 ← 8E	**8Eh**	R
Reserved	00 ← 8F	**8Fh**	
TXF filter 1 params	00 ← 90	**90h**	R/W
TXF filter 2 params	00 ← 95	**95h**	R/W
TXF error filtering enable	00 ← 9A	**9Ah**	R/W
TXF transaction processing enables	00 ← 9B	**9Bh**	R/W
Reserved	00 ← 9C-9F	**9C-9Fh**	
TTX control register	00 ← A0	**A0**	R/W
Line enable register A	00 ← A1	**A1**	R/W
Line enable register B	00 ← A2	**A2**	R/W
Custom sync pattern	00 ← A3	**A3**	R/W
Reserved	00 ← A4 - AF	**A4 - AF**	
Teletext FIFO	00 ← B0	**B0**	R
Field 1 CC data	00 ← B1	**B1**	R
Field 2 CC data	00 ← B2	**B2**	R
Buffer status A	00 ← B3	**B3**	R
Interrupt threshold	00 ← B4	**B4**	R/W
Interrupt line number	00 ← B5	**B5**	R/W
FIFO control	00 ← B6	**B6**	R/W
FIFO RAM test	00 ← B7	**B7**	W
Reserved	00 ← B8 - BF	**B8 - BF**	
Interrupt status register A	00 ← C0	**C0**	R/W
Interrupt enable A	00 ← C1	**C1**	R/W
Interrupt configuration A	00 ← C2	**C2**	R/W
Reserved	00 ← C3 - FF	**C3 - FF**	
PHI teletext FIFO	10	**N/A**	R/W
PHI status/interrupt A	11	**N/A**	R/W

NOTE: R = Read only for all interfaces
W = Write only for all interfaces
R/W = Read and write for all host interfaces
$R^{\dagger}$/W = Read and write for I^2C host interface. Write only for PHI host interfaces.

2.11 Register Definitions

2.11.1 Video Input Source Selection 1

Address	00h

7	6	5	4	3	2	1	0
Reserved						Channel 1 source selection	Reserved

Channel 1 source selection:

0 = VI1A selected (default)
1 = VI1B selected

Table 2–13. Analog Channel and Video Mode Selection

	INPUT(S) SELECTED	ADDRESS 00 BIT 1
Composite	1A	0
	1B	1

2.11.2 Analog Channel Controls

Address	01h

7	6	5	4	3	2	1	0
Reserved		Reserved		Automatic offset control		Automatic gain control	

Automatic offset control:

00 = Reserved
01 = Automatic clamping enabled (default)
10 = Reserved
11 = Clamping level frozen

Automatic gain control:

00 = Disabled (fixed gain value)
01 = AGC enabled using luma input as the reference (default).
10 = Reserved
11 = AGC frozen

2.11.3 Operation Mode Controls

Address	02h

7	6	5	4	3	2	1	0
Reserved	Reserved	TV/VCR mode		Reserved	Color subcarrier DTO frozen	Reserved	Powerdown mode

TV/VCR mode:

00 = Automatic, mode determined by the internal detection circuit (default)
01 = Reserved
10 = VCR (nonstandard video) mode
11 = TV (standard video) mode

With automatic detection enabled, unstable or nonstandard syncs on input video will force the device into VCR mode. This turns off the luminance and chrominance comb filters and turns on the chroma trap filter.

TV/VCR MODE	ACE	CE	CM[2:0]	LE	CF	LF	STANDARD	NOTE
00	0/1 0/1	0/1 1/1	XXX/000 1XX/000	1/0 1/0	10/00 01/00	11/00 11/00	NTSC PAL	Auto detection and switching between VCR/TV
01	X	X	XXX	X	XX	XX		Manual programming
10	0 0	0 1	XXX 1XX	1 1	10 01	11 11	NTSC PAL	VCR mode
11	1 1	1 1	000 000	0 0	00 00	00 00	NTSC PAL	TV mode

ACE = Adaptive comb filter enable. Chrominance control register register 1A, bit 3
CE = Comb filter enable. Chrominance control register register 1A, bit 2
CM[2:0] = Comb filter mode. Chrominance control register register 1A, bits 7-5.
LE = Luminance filter select. Luminance processing control 2 register 08, bit 6
CF = Chrominance filter select. Chrominance control 2 register 1B, bits 1 and 0.
LF = Luminance filter select. Luminance control 3 register 0E, bits 1 and 0.
X = No change

Color subcarrier DTO frozen:

0 = Color subcarrier DTO increments by the internally generated phase increment. (default)
GLCO terminal outputs the phase increment
1 = Color subcarrier DTO stops incrementing and is frozen to nominal. GLCO terminal outputs zero.

Power-down mode:

0 = Normal operation (default)
1 = Power-down mode. A/Ds are turned off and internal clocks are reduced to minimum.

2.11.4 Miscellaneous Control

Address	03h

7	6	5	4	3	2	1	0
GPCL function select		PALI and FID function select	Y U/V output enable	HSYN, VSYN, AVID, FID, PALI output enable	Reserved	Vertical blanking on/off	Clock output enable

GPCL terminal function select:

00 = GPCL is logic 0 output (default)
01 = GPCL is logic 1 output
10 = GPCL is vertical blank output
11 = GPCL is external sync lock control input

When GPCL is configured as a vertical blank output, the vertical blanking on/off bit is used to activate the output. When GPCL is configured as a sync lock control, it can be used to force the internal PLLs to their normal settings. This causes all clocks and synchronization signals to assume nominal values. The sync lock control input is active high.

PALI terminal and FID terminal function select:

0 = PALI outputs PAL indicator signal and terminal FID outputs field ID signal (default)
1 = PALI outputs horizontal lock indicator (HLK) and terminal FID outputs vertical lock indicator (VLK)

Y U/V output enable:

0 = Y U/V high impedance (default)
1 = Y U/V active

Horizontal sync (HSYN), vertical sync (VSYN), active video indicator (AVID), PALI, and FID output enables:

0 = HSYN, VSYN, AVID, PALI, and FID are high impedance
1 = HSYN, VSYN, AVID, PALI, and FID are active

This bit is default to 0 after reset if the AVID terminal is pulled down during reset or default to 1 if the AVID terminal is pulled up during reset.

Vertical blanking on/off control:

0 = Vertical blanking off (default)
1 = Vertical blanking on

Clock enable:

0 = SCLK and PCLK outputs are high impedance
1 = SCLK and PCLK outputs are enabled

This bit is default to 0 after reset if the PREF terminal is pulled down during reset or default to 1 if the AVID is pulled up during reset.

Table 2–14. Digital Output Control

OEB PIN	AVID PIN	REG 03, BIT 4 (TVPOE)	REG C2, BIT 2 (VDPOE)	YUV OUTPUT	NOTES
1	X	X	X	High impedance	At all times
0	1 during reset	X	X	Active after reset	After reset and before YUV output enable bits are programmed. TVPOE bit is default to 1 and VDPOE bit is to 1
0	0 during reset	X	X	High impedance after reset	After reset and before YUV output enable bits are programmed. TVPOE bit is default to 0 and VDPOE bit is to 1
0	X	0	X	High impedance	After both YUV output enable bits are programmed
0	X	X	0	High impedance	After both YUV output enable bits are programmed
0	X	1	1	Active	After both YUV output enable bits are programmed

2.11.5 Color Killer Threshold Control

Address	06h

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold				

Automatic color killer:

00 = Automatic mode (default)
01 = Reserved
10 = Color killer enabled. The UV terminals are forced to a zero color state.
11 = Color killer disabled

Color killer threshold (ref. 0 dB = nominal burst amplitude):

11111 = –30 dB
10000 = –24 dB (default)
00000 = –18 dB

2.11.6 Luminance Processing Control 1

Address	07h

7	6	5	4	3	2	1	0
Luma bypass mode	Pedestal not present	Reserved	Luma bypass during vertical blank	Luminance signal delay with respect to chrominance signal			

Luma bypass mode select:

0 = Input video bypasses the chroma trap and comb filters. Chroma outputs are forced to zero. (default)
1 = Input video bypasses the whole luma processing.
Raw A/D data is output alternatively as UV data and Y data at SCLK rate. The output data is properly clipped to comply to CCIR601 coding range. Only valid for 10-bit YUV output format (YUV output format = 100 or 111 at register 0D)

Pedestal not present:

0 = 7.5 IRE pedestal is present on the analog video input signal (default)
1 = Pedestal is not present on the analog video input signal

Luminance bypass mode during vertical blanking:

0 = No (default)
1 = Yes

When the luminance bypass is enabled, the luminance comb and notch filters are turned off and the chrominance components of the output video are sent to a zero color state. Luminance bypass will occur for the duration of the vertical blanking as defined by register 18 and 19. This feature may be used to prevent distortion of test and data signals present during the vertical blanking interval.

Luma signal delay with respect to chroma signal in pixel clock increments (range –8 to 7 pixel clocks):

1111 = –8 pixel clocks delay
1011 = –4 pixel clocks delay
1000 = –1 pixel clocks delay
0000 = 0 pixel clocks delay (default)
0011 = 3 pixel clocks delay
0111 = 7 pixel clocks delay

2.11.7 Luminance Processing Control 2

Address	08h

7	6	5	4	3	2	1	0
Reserved	Luminance filter select	Reserved		Peaking gain		Reserved	

Luminance filter select:

0 = Luminance comb filter enabled (default)
1 = Luminance chroma trap filter enabled

Peaking gain:

00 = Peaking disabled (default)
01 = 3 dB
10 = 6 dB
11 = 12 dB

Peaking frequency:

Square-pixel sampling rate:

NTSC	PAL	PAL M	PAL N
2.4 MHz	2.9 MHz	2.4 MHz	2.9 MHz

ITU-R BT.601 sampling rate:

All standards
2.6 MHz Refer to Figures 2–16, 2–17 and 2–18.

2.11.8 Brightness Control

Address	09h

7	6	5	4	3	2	1	0
Brightness control							

Brightness:

1 1 1 1 1 1 1 1 = 255 (bright)
1 0 0 0 1 0 1 1 = 139 (ITU-R BT.601 level)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (dark)

2.11.9 Color Saturation Control

Address	0Ah

7	6	5	4	3	2	1	0
Saturation control							

Saturation:

1 1 1 1 1 1 1 1 = 255 (maximum)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (no color)

2.11.10 Hue Control

Address	0Bh

7	6	5	4	3	2	1	0
Hue control							

Hue:

0 1 1 1 1 1 1 1 = 180 degrees
0 0 0 0 0 0 0 0 = 0 degrees (default)
1 0 0 0 0 0 0 0 = –180 degrees

2.11.11 Contrast Control

Address	0Ch

7	6	5	4	3	2	1	0
Contrast control							

Contrast:

1 1 1 1 1 1 1 1 = 255 (maximum contrast)
1 0 0 0 0 0 0 0 = 128 (default)
0 0 0 0 0 0 0 0 = 0 (minimum contrast)

2.11.12 Outputs and Data Rates Select

Address	0Dh

7	6	5	4	3	2	1	0
Reserved	YUV output code range	UV code format	YUV data path bypass		YUV output format		

YUV output code range:

0 = ITU-R BT.601 coding range (Y ranges from 16 to 235. Cr and Cb range from 16 to 240)
1 = Extended coding range (Y, Cr and Cb range from 1 to 254) (default)

UV code format:

0 = Offset binary code (2s complement + 128) (default)
1 = Straight binary code (2s complement)

YUV data path bypass:

00 = Normal operation. (default)
01 = YUV output pins connected to decimation filter output, decoder function bypassed, for test purpose only. Both Y and UV busses output data at PCLK rate.
10 = YUV output pins connected to A/D output, decoder function bypassed, for test purpose only. Both Y and UV busses output data at SCLK rate.
11 = Reserved

YUV output format:

000 = 20-bit 4:2:2 (default)
001 = Reserved
010 = Reserved
011 = Reserved
100 = 10-bit 4:2:2
101= Reserved
110 = Reserved
111 = 10-Bit ITU-R BT. 656 interface

Address	0Eh

7	6	5	4	3	2	1	0
Reserved						Luminance filter select	

Luminance Filter Stopband bandwidth (MHz):

	NTSC CCIR601	NTSC Square pixel	PAL CCIR601	PAL Square pixel
00 =	1.2129	1.1026	1.2129	1.3252
01 =	0.8701	0.7910	0.8701	0.9507
11 =	0.5010	0.4554	0.5010	0.5474

Luminance filter select[1:0] selects one of the four chroma trap filters to produce a luminance signal by removing the chrominance signal from the composite video signal. The stop band of the chroma trap filter is centered at the chroma subcarrier frequency with stopband bandwidth controlled by the two control bits. Refer to Figure 2–12, 2-13 and 2-14 for the frequency responses of the filters. The control 00 is the default mode.

2.11.13 Horizontal Sync HSYN Start NTSC/PAL

Address	7	6	5	4	3	2	1	0
16h	HSYN start for NTSC							
17h	HSYN start for PAL							

HSYN Start:

1 1 1 1 1 1 1 1 = –127 × 4 pixel clocks
1 0 0 0 0 0 0 0 = 0 pixel clocks (defaults)
0 0 0 0 0 0 0 0 = 128 × 4 pixel clocks

2.11.14 Vertical Blanking VBLK Start

Address	18h

7	6	5	4	3	2	1	0
VBLK start							

VBLK Start:

0 1 1 1 1 1 1 1 = 127 lines after start of vertical blanking interval
0 0 0 0 0 0 0 1= 1 line after start of vertical blanking interval
0 0 0 0 0 0 0 0 = same time as start of vertical blanking interval (default)
1 1 1 1 1 1 1 1 = 1 line before start of vertical blanking interval
1 0 0 0 0 0 0 0 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals as shown in Table 2–15. The setting in this register determines the timing of the GPCL signal when it is configured to output vertical blank(see register 03). The setting in this register is also used to determine the duration of the luma bypass function (see register 07).

Table 2–15. Vertical Blanking Interval Start and End

STANDARD	FIELD	START LINE NUMBER	END LINE NUMBER
NTSC	odd	1	21
	even	263.5	284.5
PAL	odd	623.5	23.5
	even	311	335
MPAL	odd	523	21
	even	260.5	284.5
NPAL	odd	623.5	23.5
	even	311	335

2.11.15 Vertical Blanking VBLK Stop

Address	19h

7	6	5	4	3	2	1	0
VBLK end							

VBLK End:

0 1 1 1 1 1 1 1 = 127 lines after end of vertical blanking interval
0 0 0 0 0 0 0 1= 1 line after end of vertical blanking interval
0 0 0 0 0 0 0 0 = same time as end of vertical blanking interval (default)
1 1 1 1 1 1 1 1 = 1 line before end of vertical blanking interval
1 0 0 0 0 0 0 0 = 128 lines before end of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals as shown in Table 2–16. The setting in this register determines the timing of the GPCL signal when it is configured to output vertical blank(see register 03). The setting in this register is also used to determine the duration of the luma bypass function (see register 07).

2.11.16 Chrominance Control 1

Address	1Ah

7	6	5	4	3	2	1	0
Chrominance Comb Filter Mode [2:0]			Color DTO Reset	Chrominance Adaptive Comb Filter Enable	Chrominance Comb Filter Enable	Automatic Color Gain Control	

Table 2–16. Chrominance Comb Filter Selection

ACE	CE	CM[2]	CM[1]	CM[0]	COMB FILTER SELECTION
0	0	X	X	X	Comb filter disabled
0	1	0	0	X	Fixed 3-line comb filter with (1/4, 1/2, 1/4) coefficients
0	1	0	1	X	Fixed 3-line comb filter with (1, 0, 1) coefficients
0	1	1	X	X	Fixed 2-line comb filter
1†	X	X	0†	0†	Adaptive between 3-line (1/4,1/2,1/4) comb filter and 2-line comb filter
1	X	X	0	1	Adaptive between 3-line (1/4,1/2,1/4) comb filter and no comb filter
1	X	X	1	0	Adaptive between 3-line (1,0,1) comb filter and 2-line comb filter
1	X	X	1	1	Adaptive between 3-line (1,0,1) comb filter and no comb filter

† Indicates default settings

Color DTO reset:

0 = Color subcarrier DTO not reset. (default)
1 = Color subcarrier DTO reset

Color subcarrier DTO is reset to zero and the color subcarrier DTO bit then immediately returns to zero.

When this bit is set, the subcarrier DTO phase reset bit is transmitted on the GCLO terminal on the next occurrence of a specified line (NTSC or PAL).

Automatic color gain control:

00 = ACC enabled (default)

01 = Reserved

10 = ACC disabled

11 = ACC frozen

2.11.17 Chrominance Control 2

Address	1Bh

Reserved	Chrominance Filter Select

Chrominance Output Bandwidth (MHz):

	NTSC CCIR601	NTSC Square Pixel	PAL CCIR601	PAL Square Pixel
00 =	1.2129	1.1026	1.2129	1.3252
01 =	0.8701	0.7910	0.8701	0.9507
10 =	0.7183	0.6712	0.7383	0.8066
11 =	0.5010	0.4554	0.5010	0.5474

Refer to Figures 2-6, 2-7, and 2-8 for the frequency responses of the filters. The control 00 is the default setting**.**

2.11.18 Interrupt Reset Register B

Address	1Ch

	7	6	5	4	3	2	1	0
Interrupt Reset Register B (1C)	Software Init Reset	Reserved	TVP Command Ready Reset	Field Rate Changed Reset	Line Alternation Changed Reset	Color Lock Changed Reset	H/V Lock Changed Reset	TV/VCR Changed Reset

TV/VCR Changed Reset	*0 = No effect on interrupt register B	1 = Reset TV/VCR changed bit
H/V Lock Changed Reset	*0 = No effect on interrupt register B	1 = Reset H/V lock changed bit
Color Lock Changed Reset	*0 = No effect on interrupt register B	1 = Reset color lock changed bit
Line Alternation Changed Reset	*0 = No effect on interrupt register B	1 = Reset line alternation changed bit
Field Rate Changed Reset	*0 = No effect on interrupt register B	1 = Reset field rate changed bit
TVP Command Ready Reset	*0 = No effect on interrupt register B	1 = Reset TVP command ready bit
Software Init	*0 = No effect on interrupt register B	1 = Reset software init bit

The interrupt reset register B is used by the external processor to reset the interrupt status bits in the interrupt register B. Bits loaded with a 1 will allow the corresponding interrupt status bit to reset to 0. Bits loaded with a 0 have no effect on the interrupt status bits.

2.11.19 Interrupt Enable Register B

Address	1Dh

	7	6	5	4	3	2	1	0
Interrupt Reset Register B (1D)	Software Init Complete	Reserved	TVP Command Ready	Field Rate Changed	Line Alternation Changed	Color Lock Changed	H/V Lock Changed	TV/VCR Changed

TV/VCR Changed	*0 = TV/VCR status has not changed	1 = TV/VCR mode detect not changed
H/V Lock Changed	*0 = H/V lock status has changed	1 = H/V lock status has changed
Color Lock Changed	*0 = Color lock status has changed	1 = Color lock status has changed
Line Alternation Changed	*0 = Line alternation has not changed	1 = Line alternation has changed
Field Rate Changed	*0 = Field rate has not changed	1 = Field rate has changed
TVP Command Ready	*0 = TVP is not ready to accept a new command	1 = TVP is ready to accept a new command
Software Init Complete	*0 = Software initialization has not completed	1 = Software initialization has completed.

The interrupt enable register B is used by the external processor to mask unnecessary interrupt sources for interrupt B. Bits loaded with a 1 will allow the corresponding interrupt condition to generate an interrupt on the external terminal. Conversely bits loaded with a 0 will mask the corresponding interrupt condition from generating an interrupt on the external terminal. Note this register only affects the external terminal; it does not affect the bits in the interrupt status register. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal, either perform a logical AND of the interrupt status register B with the interrupt enable register B or check the state of the interrupt B bit in the interrupt B active register.

2.11.20 Interrupt Configuration Register B

Address	1Eh

	7	6	5	4	3	2	1	0
Interrupt Configuration Register B	Reserved							Interrupt Polarity B

Interrupt Polarity 0 = Interrupt B is active low. *1 = Interrupt B is active high. Must be same as interrupt polarity A bit at bit 0 of interrupt configuration register A at address C2

The interrupt configuration register B is used to configure the polarity of interrupt B on the external interrupt terminal. Note that when the interrupt B is configured for active low the terminal will be driven low when active and 3-state when inactive (open-collector). Conversely, when the interrupt B is configured for active high it will be driven high for active and driven low for inactive.

2.11.21 Program RAM Write

Address	7Eh

7	6	5	4	3	2	1	0

The program RAM can be written via the program RAM write register at address 7E.

2.11.22 Microprocessor Reset Clear

Address	7Fh

7	6	5	4	3	2	1	0

A write with any data to this register must be performed to restart the internal microprocessor after the completion of the microcode download to the program RAM.

2.11.23 Major Software Revision Number

Address	80h

7	6	5	4	3	2	1	0
Major Revision Number							

This register contains the major software revision number.

2.11.24 Status Register 1

Address	81h

7	6	5	4	3	2	1	0
Peak white detect status	Line-alternating status	Field rate status	Lost lock detect	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Peak white detect status:

0 = Peak white is not detected.
1 = Peak white is detected.

Line-alternating status:

0 = Non line-alternating
1 = Line alternating

Field rate status:

0 = 60 Hz
1 = 50 Hz

Lost lock detect:

0 = No lost lock since status register 1 was last read.
1 = Lost lock since status register 1 was last read.

Color subcarrier lock status:

0 = Color subcarrier is not locked.
1 = Color subcarrier is locked.

Vertical sync lock status:

0 = Vertical sync is not locked.
1 = Vertical sync is locked.

Horizontal sync lock status:

1 = Horizontal sync is locked.

TV/VCR status:

0 = TV
1 = VCR

2.11.25 Status Register 2

Address	82h

7	6	5	4	3	2	1	0
Reserved		PAL switch polarity	Field sequence status	AGC and offset status	Reserved		

PAL switch polarity of first line of odd field:

0 = PAL switch is zero (Color burst phase = 135 degree)
1 = PAL switch is one (Color burst phase = 225 degree)

Field sequence status:

0 = Even field
1 = Odd field

Automatic gain and offset status:

0 = Automatic gain and offset is not frozen.
1 = Automatic gain and offset is frozen.

2.11.26 Status Register 3

Address	83h

7	6	5	4	3	2	1	0
AGC gain							

AGC gain (step size = 0.831%):

0 0 0 0 0 0 0 0 = –6 dB
0 1 0 0 0 0 0 0 = – 3 dB
1 0 0 0 0 0 0 0 = 0 dB
1 1 0 0 0 0 0 0 = 3 dB
1 1 1 1 1 1 1 1 = 6 dB

2.11.27 Status Register 4

Address	84h

7	6	5	4	3	2	1	0
Subcarrier to horizontal (SCH) phase							

SCH (color DTO subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field; step size 360 deg/256):

0 0 0 0 0 0 0 0 = 0.00 degree
0 0 0 0 0 0 0 1 = 1.41 degree
0 0 0 0 0 0 1 0 = 2.81 degree
1 1 1 1 1 1 1 0 = 357.2 degree
1 1 1 1 1 1 1 1 = 358.6 degree

2.11.28 Interrupt Status Register B

Address	85h

	7	6	5	4	3	2	1	0
Interrupt Status Register B (85)	Software Init	Reserved	TVP Command Ready	Field Rate Changed	Line Alternation Changed	Color Lock Changed	H/V Lock Changed	TV/VCR Changed

TV/VCR Changed	*0 = TV/VCR status has not changed	1 = TV/VCR mode detect not changed
H/V Lock Changed	*0 = H/Vlock status has changed	1 = H/V lock status has changed
Color Lock Changed	*0 = Color lock status has changed	1 = Color lock status has changed
Line Alternation Changed	*0 = Line alternation has not changed	1 = Line alternation has changed
Field Rate Changed	*0 = Field rate has not changed	1 = Field rate has changed
TVP Command Ready	*0 = TVP is not ready to accept a new command	1 = TVP is ready to accept a new command
Software Init	*0 = Software Init is not ready	1 = Software Init is ready

The interrupt status register B is polled by the external processor to determine the interrupt source for interrupt B. After an interrupt condition is set it can be reset by writing to interrupt reset register B at subaddress 1Ch with a 1 in the appropriate bit.

2.11.29 Interrupt B Active Register

Address	86h

	7	6	5	4	3	2	1	0
Interrupt B Active Register	0							Interrupt B

Interrupt B	0 = Interrupt B is not active.	*1 = Interrupt B is active.

The interrupt status register is polled by the external processor to determine if interrupt B is active.

2.11.30 Minor Software Revision Number

This register contains the minor revision number for the TVP5031 software. This is a number from 0 to 99.

Address	87h

7	6	5	4	3	2	1	0
Minor revision number							

2.11.31 Status Register 5

This register contains information about the detected video standard and the sampling rate for digital video output data.

d0 – (M)PAL video standard detected
d1 – (Combination-N)PAL video standard detected
d2 – Sampling rate
d7:d3 – Reserved

Address	88h

7	6	5	4	3	2	1	0
Reserved		Reserved	Reserved	Reserved	Sampling Rate	NPAL	MPAL

MPAL
0 = (M)PAL video standard is not detected
1 = (M)PAL video standard is detected

NPAL
0 = (Combination-N)PAL video standard is not detected
1 = (Combination-N)PAL video standard is detected

Sampling rate
0 = ITU-R BT.601
1 = Square pixel

2.11.32 Program RAM Read

Address	8Eh

7	6	5	4	3	2	1	0

The program RAM can be read via the program RAM read register at address 8E.

2.11.33 TXF Filter 1 Parameters

Address	7	6	5	4	3	2	1	0
90h	Filter 1 Mask_1[3:0]				Filter 1 Pattern_1[3:0]			
91h	Filter 1 Mask_2[3:0]				Filter 1 Pattern_2[3:0]			
92h	Filter 1 Mask_3[3:0]				Filter 1 Pattern_3[3:0]			
93h	Filter 1 Mask_4[3:0]				Filter 1 Pattern_4[3:0]			
94h	Filter 1 Mask_5[3:0]				Filter 1 Pattern_5[3:0]			

For an NABTS system, the packet prefix consists of five bytes: P1, P2, P3, CI and PS. Each byte contains 4 data bits interlaced with 4 Hamming protection bits.

Pattern_1[3:0] corresponds to P1[7], P1[5], P1[3], P1[1] (Packet address)
Pattern_2[3:0] corresponds to P2[7], P2[5], P2[3], P2[1] (Packet address)
Pattern_3[3:0] corresponds to P3[7], P3[5], P3[3], P3[1] (Packet address)
Pattern_4[3:0] corresponds to CI[7], CI[5], CI[3], CI[1] (Continuity index)
Pattern_5[3:0] corresponds to PS[7], PS[5], PS[3], PS[1] (Packet structure)

For a WST system (PAL or NTSC), the magazine and row address group consists of two bytes. The two bytes contain three bits of magazine number (M[2:0]) and 5 bits of row address (R[4:0]), interlaced with eight Hamming protection bits.

Pattern_1[3:0] corresponds to R[0], M[2], M[1], M[0] (Magazine and row LSB)
Pattern_2[3:0] corresponds to R[4], R[3], R2], R[1] (Upper bits of row address)
Pattern_3[3:0] is ignored
Pattern_4[3:0] is ignored
Pattern_5[3:0] is ignored

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of Mask_1 means that the TXF module should compare the LSB of nibble_1 in the pattern register to the first data bit of the transaction. A 0 in the LSB of Mask_1 means that the TXF module should ignore the first data bit of the transaction.

> **NOTE:** The TXF Filter 1 parameters can only be written and read when both the Filter 1 enable and the Filter 2 enable bits are 0. When reading the values, the values must be read consecutively, starting with the first value.

These registers hold the search parameters for Filter 1. The parameters are used to parse the first five bytes of NABTS Teletext transactions or the first two bytes if WST transactions. These bytes of teletext are expected to always contain four data bits interlaced with four Hamming protection bits. The protection bits are ignored by the filter.

2.11.34 TXF Filter 2 Parameters

Address	7	6	5	4	3	2	1	0
95h	Filter 2 Mask_1[3:0]				Filter 2 Pattern_1[3:0]			
96h	Filter 3 Mask_2[3:0]				Filter 2 Pattern_2[3:0]			
97h	Filter 2 Mask_3[3:0]				Filter 2 Pattern_3[3:0]			
98h	Filter 2 Mask_4[3:0]				Filter 2 Pattern_4[3:0]			
99h	Filter 2 Mask_5[3:0]				Filter 2 Pattern_5[3:0]			

For an NABTS system, the packet prefix consists of five bytes: P1, P2, P3, CI and PS. Each byte contains 4 data bits interlaced with 4 Hamming protection bits.

Pattern_1[3:0] corresponds to P1[7], P1[5], P1[3], P1[1] (Packet address)
Pattern_2[3:0] corresponds to P2[7], P2[5], P2[3], P2[1] (Packet address)
Pattern_3[3:0] corresponds to P3[7], P3[5], P3[3], P3[1] (Packet address)
Pattern_4[3:0] corresponds to CI[7], CI[5], CI[3], CI[1] (Continuity index)
Pattern_5[3:0] corresponds to PS[7], PS[5], PS[3], PS[1] (Packet structure)

For a WST system (PAL or NTSC), the magazine and row address group consists of two bytes. The two bytes contain three bits of magazine number (M[2:0]) and 5 bits of row address (R[4:0]), interlaced with eight Hamming protection bits.

Pattern_1[3:0] corresponds to R[0], M[2], M[1], M[0] (Magazine and row LSB)
Pattern_2[3:0] corresponds to R[4], R[3], R2], R[1] (Upper bits of row address)
Pattern_3[3:0] is ignored
Pattern_4[3:0] is ignored
Pattern_5[3:0] is ignored

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of Mask_1 means that the TXF module should compare the LSB of nibble_1 in the pattern register to the first data bit of the transaction. A 0 in the LSB of Mask_1 means that the TXF module should ignore the first data bit of the transaction.

NOTE: The TXF Filter 2 parameters can only be written and read when both the Filter 1 enable and the Filter 2 enable bits are 0. When reading the values, the values must be read consecutively, starting with the TXF Filter 1 parameters values.

These registers hold the search parameters for Filter 2. The parameters are used to parse the first five bytes of NABTS Teletext transactions or the first two bytes if WST transactions. These bytes of teletext are expected to always contain four data bits interlaced with four Hamming protection bits. The protection bits are ignored by the filter.

2.11.35 TXF Error Filtering Enables

Address	9Ah

	7	6	5	4	3	2	1	0
TXF Error Filtering Enables (R/W)	Reserved				LPC Error Enable	CCD Parity Error Enable	Teletext Parity Error Enable	Hamming Error Enable

Hamming error enable	0 = disable	1 = enable	default = 0
Teletext parity error enable	0 = disable	1 = enable	default = 0
CCD parity error enable	0 = disable	1 = enable	default = 0
LPC error enable	0 = disable	1 = enable	default = 0

These bits allow the TXP module to discard transactions based on bit errors. The hamming error enable allows error correction and detection of Hamming encoded bytes. The teletext parity error enable allows the TXP to discard Teletext transactions with parity errors. The CCD parity error enable allows the TXP to discard closed caption transactions with parity errors. The LPC error enable allows the TXP to discard Teletext transactions with longitudinal parity errors.

2.11.36 TXF Transaction Processing Enables

Address	9Bh

	7	6	5	4	3	2	1	0
TXF Error Filtering Enables (R/W)	Reserved			Filter 2 Enable	Filter 1 Enable	CCD Odd Field Enable	CCD Even Field Enable	Teletext Enable

Teletext enable	0 = disable	1 = enable	default = 0
CCD odd field enable	0 = disable	1 = enable	default = 0
CCD even field enable	0 = disable	1 = enable	default = 0
Filter 1 enable	0 = disable	1 = enable	default = 0
Filter 2 enable	0 = disable	1 = enable	default = 0

These bits are used to enable or disable certain features. The teletext enable allows the TXP module to receive teletext data. If this bit is 0 , all outputs from the TXP remain idle while teletext data is present. The CCD field enables allow the TXP to receive closed caption data during the odd, even, or both fields. The Filter 1 enable allows the TXF module to parse data based on the values in the Filter 1 parameters register. The Filter 2 enable allows the TXF module to parse data based on the values in the Filter 2 parameters register.

2.11.37 TTX Control Register

Address	A0h

	7	6	5	4	3	2	1	0
TTX Control Register	Reserved				Full-Field Enable	Custom Framing Code	CCD Enable	TTX Mode

TTX Mode 0 = NABTS 1 = WST

CCD ENABLE 0 = Closed caption is DISABLED 1 = Closed caption is ENABLED

Custom Sync 0 = Use default TTX sync pattern 1 = Use sync pattern register

Full Field Enable 0 = No TTX search after VBI area 1 = TTX search all lines after VBI

The TTX control register allows the operating parameters of the TDR to be controlled. Note that the TTX mode selection is independent of PAL/NTSC mode, which is selected by the TVP5020. This effectively controls the default framing code and data rate. Closed caption is affected by 525 lines vs 625 lines (but not NABTS/WST). For NTSC and PAL M, the CCD data search is on Line 21; for PAL B,G,I,N it is on Line 22. Custom framing code affects teletext data only - closed caption data always uses the default sync pattern.

2.11.38 Line Enable Registers A, B

	7	6	5	4	3	2	1	0
A1h – Line Enable Register A	Enable Line 17/280 (14/327	Enable Line 16/279 (13/326)	Enable Line 15/278 (12/325)	Enable Line 14/277 (11/324)	Enable Line 13/276 (10/323)	Enable Line 12/275 (9/322)	Enable Line 11/274 (8/321)	Enable Line 10/273 (7/320)

	7	6	5	4	3	2	1	0
A2h – Line Enable Register B	Enable Line 25/288 (22/335)	Enable Line 24/287 (21/334)	Enable Line 23/286 (20/333)	Enable Line 22/285 (19/332)	Enable Line 21/284 (18/331)	Enable Line 20/283 (17/330)	Enable Line 19/282 (16/329)	Enable Line 18/281 (15/328)

NOTE: Line numbers in parenthesis refer to 625 Line systems

Line Enable XX 0 = No TTX Search on Line XX 1 = Search Line XX for TTX Data

In both VBI only and full field modes, the vertical interval lines can be individually enabled or disabled. Only lines that are enabled are searched for the selected type of teletext data. This allows some amount of filtering on a physical location basis. If closed caption data is enabled, this overrides the enable/disable bit for Line 21 (22). If full field mode is enabled, *all lines after the vertical interval* are searched for the selected type of teletext data. The registers are initialized to 0x00 on reset.

2.11.39 Sync Pattern Register

Address	A3h

	7	6	5	4	3	2	1	0
Custom Sync Pattern	Framing Code [7:0]							

If the custom sync bit is set in the control register, the sync comparator uses the contents of the sync pattern register as the bit pattern for the teletext framing code. Otherwise, the default sync patterns are used. Relative to the sync pattern register, incoming bits are shifted in MSB first. To illustrate; the default WST framing code would be specified as 0xE4 and the default NABTS framing code would be specified as 0xE7 (although the MSB versus. LSB is ambiguous for the latter).

> **NOTE:**The custom sync option is only valid for NABTS or WST messages; closed caption always uses the EIA standard start bit pattern.

2.11.40 Teletext FIFO

Address	B0h

	7	6	5	4	3	2	1	0
Teletext FIFO (R)	Teletext Data FIFO [7:0]							

The teletext FIFO can be accessed via the regular teletext FIFO register at address B0.

Reading this location returns 1 byte from the FIFO that store teletext transactions. If the FIFO is empty, a read will return the same value as the previous read**.** *It is the driver software's or application software's responsibility to assure that the correct number of bytes per transaction are read out from the teletext FIFO.* The transaction length depends on the whether the data is NABTS, WST-NTSC or WST-PAL.

2.11.41 Closed Caption Data

Address	B2h

7	6	5	4	3	2	1	0
Closed Caption Data [7:0]							

The closed caption data contains two bytes per transaction. To retrieve both bytes this register must be read twice. The first read returns the first byte of the message; the second read returns the second byte. Further reads return the first byte until new data is received.

In order to distinguish between closed caption data received in the odd and even fields, software can test the field sequence status bit (Address 82h, bit 4).

2.11.42 Buffer Status

Address	B3h

	7	6	5	4	3	2	1	0
Buffer Status (R)	Reserved	CCD Avail	Tx Count [3:0]				FIFO Full	Teletext Data Avail

Teletext Avail — This bit indicates that at least one *complete* teletext transaction is in the FIFO. This bit is cleared when the FIFO is emptied.

FIFO Full — This bit indicates that the maximum number of complete teletext transactions is in the FIFO.

Tx Count — This value represents the number of *complete* teletext transactions in the FIFO.

CCD Avail — This status bit indicates that closed caption data has been received. The status bit is cleared when both of the two bytes have been read.

2.11.43 Interrupt Threshold

Address	B4h

	7	6	5	4	3	2	1	0
Interrupt Threshold (R/W)					Threshold Value [3:0]			

Threshold Value — This value determines how many teletext transactions must be received before the teletext threshold bit is set in the interrupt status register. The default value is 5.

2.11.44 Interrupt Line Number

Address	B5h

	7	6	5	4	3	2	1	0
Interrupt Line Number (R/W)			Data Required	Interrupt Line Number [4:0]				

Interrupt Line Number — This value determines which video line number will be used to generate the teletext data, CC even field and CC odd field bits in the interrupt status register. The register value is examined at the start of the line. Since there is no line 0 a value of all zeros in this register will disable the three interrupt signals that use this condition. The default value is 24 (18h).

Data Required — If this bit is set HIGH, the teletext data bit will only be set if there is data in the FIFO. This bit does not affect the CC even field and CC odd field bits**.** The default value for this bit is 1.

2.11.45 FIFO Control

Address	B6h

	7	6	5	4	3	2	1	0
FIFO Control (R/W)	Reserved			CCD Reset	Read in Progress	RAM Test	TTX PHI Output Enable	FIFO Reset

FIFO Reset — When a 1 is written to this register bit, the FIFO is flushed. This is done by clearing the read and write pointers to zero, clearing the Tx count to zero and clearing all status flags. This bit is automatically cleared back to 0.

TTX PHI Output Enable — A 1 in this register enables access to the teletext data in the FIFO through the parallel host port and disables access from the output formatter. A 0 disables access from the parallel host and enables access from the output formatter. The default value is one.

RAM TEST — Setting this bit high allows the micro to write data into the FIFO. In this mode, data from the TXP is ignored. This allows the micro to test the RAM by writing and reading test patterns. The default value is zero.

Read in Progress — This bit indicates that the first byte of a teletext transaction has been read, but the last byte has not been read. This bit can be used to verify data alignment as it is read from the FIFO.

CCD Reset — When a 1 is written to this register bit, the closed caption register is reset. Also, the status flag is cleared to 0. This bit is automatically cleared back to 0.

2.11.46 FIFO RAM Test

Address	B7h

	7	6	5	4	3	2	1	0
FIFO RAM Test (W)								

FIFO RAM test register provides diagnostic capability into the internal teletext FIFO. This register can be written sequentially with a block of data. The data is read back using the Teletext FIFO data register at address B0h to verify the correct operation of the FIFO.

2.11.47 Interrupt Status Register A

Address	C0h

	7	6	5	4	3	2	1	0
Interrupt Status Register A (R/W)	TvpLOCK State	TvpLOCK Interrupt	Cycle Complete	Bus Error	CC Odd Field	CC Even Field	Teletext Threshold	Teletext Data

Teletext Data *0 = Teletext data buffer empty or we have not reached the video line number that equals the interrupt line number register

1 = Teletext data buffer contains a complete transaction and the video line number = interrupt line number register

Note this bit can be configured to occur whenever the video line number = interrupt line number register regardless of the data.

Teletext Threshold *0 = Threshold not reached

1 = Teletext data in buffer has reached configurable threshold

CC Even Field *0 = Buffer empty

1 = Even field closed caption buffer contains data

CC Odd Field *0 = Buffer empty

1 = Odd field closed caption buffer contains data

Bus Error *0 = No bus error

1 = PHI interface detected an illegal access

Cycle Complete *0 = Read or write cycle in progress

1 = Read or write cycle complete

tvpLOCK Interrupt *0 = A transition has not occurred on the tvpLOCK signal

1 = A transition has occurred on the tvpLOCK signal

Note, an interrupt will be generated on any transition of the lock signal.

tvpLOCK State *0 = TVP not locked to video

1 = TVP locked to video signal

Reflects the present state of the tvpLOCK.

The interrupt status register A is polled by the external processor to determine the interrupt source. After an interrupt condition is set, it can be reset by writing to this register with a 1 in the appropriate bit(s).

2.11.48 Interrupt Enable Register A

Address	C1h

	7	6	5	4	3	2	1	0
Interrupt Enable Register A (R/W)	tvpLOCK State	tvpLOCK Interrupt Enable	Cycle Complete Enable	Bus Error Enable	CC Odd Field Enable	CC Even Field Enable	Teletext Threshold Enable	Teletext Data Enable

The interrupt enable register A is used by the external processor to mask unnecessary interrupt sources for interrupt A. Bits loaded with a 1 will allow the corresponding interrupt condition to generate an interrupt on the external terminal. Conversely bits loaded with a 0 will mask the corresponding interrupt condition from generating an interrupt on the external terminal. Note this register only affects the interrupt A on external terminal, it does not affect the bits in the interrupt status register A. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal, either perform a logical AND of the interrupt status register B with the interrupt enable register B or check the state of the interrupt B bit in the interrupt B active register.

Address	C2h

	7	6	5	4	3	2	1	0
Interrupt Configuration Register A (R/W)	Reserved					YUV Output Enable A	Interrupt A	Interrupt Polarity A

Interrupt Polarity 0 = Interrupt is active low

1 = Interrupt is active high

Interrupt A 0 = Interrupt terminal is not active

1 = Interrupt terminal is active

Reflects state of Interrupt A on the external terminal. This bit is read only.

YUV Output Enable A 0 = YUV terminals are 3-state

1 = YUV terminals are active if other conditions are met

The interrupt configuration register A is used to configure the polarity of the external in interrupt terminal. Note that when the interrupt is configured for active low the terminal will be driven low when active and 3-state when inactive (open-collector). Conversely, when the terminal is configured for active high it will be driven high for active and driven low for inactive.

2.11.49 Parallel Host Interface Teletext FIFO

Address	10b

7	6	5	4	3	2	1	0

This read-only register is only accessible when the PHI interface is enabled. To access this register, use the direct address of 10. Notice almost all the PHI registers are accessed through an indirect address scheme, by writing the indirect address to address 00 and then write to or read from address 01. This register contains the same information as the teletext FIFO register at indirect address B0 and is the recommended way of reading data from the teletext FIFO due to its efficiency.

2.11.50 Parallel Host Interface Status/Interrupt A

Address	11b

7	6	5	4	3	2	1	0

This read-write register is only accessible when the PHI interface is enabled. To access this register, use the direct address of 11. Notice almost all the PHI registers are accessed through an indirect address scheme, by writing the indirect address to address 00 and then write to or read from address 01. This register contains the same information as the interrupt status register A at indirect address C0. This is the recommended way of reading the interrupt/status information due to its efficiency. After an interrupt condition is set, it can be reset by writing to this register with a 1 in the appropriate bit(s).

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Digital power supply voltage, DV_{DD} . . . . . –0.3 V to 3.6 V
Analog power supply voltage, AV_{DD} . . . . . –0.5 V to 3.6 V
Digital input voltage, Vi . . . . . –0.3 V to DVdd+0.3 V
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Maximum total power dissipation, P_d . . . . . 2.5 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Digital supply voltage, DV_{DD}	3	3.3	3.6	V
Analog supply voltage, AV_{DD}	3.1	3.3	3.5	V
Analog input voltage, V_i(p-p) (ac coupling necessary)	0.5	1	1.26	V
Digital input voltage high, V_{IH}	2			V
Digital input voltage low, V_{IL}			0.8	V
Input voltage high, VC0 and VC1 in I^2C mode, V_{IH} (I^2C)	2.3			V
Input voltage low, VC0 and VC1 in I^2C mode, V_{IL} (I^2C)			1	V
Output current, Vout = 2.4 V, I_{OH}	–4	–8		mA
Output current, Vout = 0.4 V, I_{OL}	6	8		mA
Operating free-air temperature, T_A	0		70	°C

3.2.1 Crystal Specifications

	MIN	NOM	MAX	UNIT
Frequency		14.31818		MHz
Frequency tolerance			±50	ppm

3.3 Electrical Characteristics Over Recommended Voltage and Temperature Ranges, DV_{DD} = 3.3 V, AV_{DD} = 3.3 V, T_A = 70°C (unless otherwise noted)

3.3.1 DC Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(D)}$	Digital supply current			120	160	mA
$I_{DD(A)}$	Analog supply current			80	100	mA
I_{lkg}	Input leakage current				10	μA
C_i	Input capacitance	By design			8	pF
V_{OH}	Output voltage high		2.4			V
V_{OL}	Output voltage low				0.4	V

NOTE 1: Measured with a load of 10 kΩ in parallel with 15 pF.

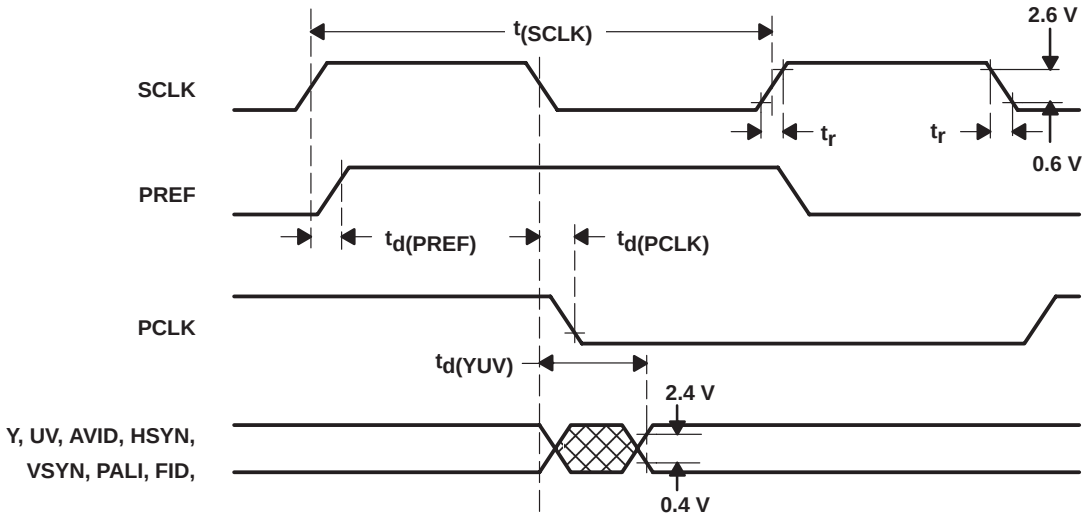
3.3.2 Analog Processing and A/D Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_i	Input impedance, analog video inputs	By design	200			kΩ
C_i	Input capacitance, analog Video inputs	By design			10	pF
$V_{i(pp)}$	Input voltage range	$C_{coupling}$ = 0.1 μF	0.50	1	1.41	V
$G_{(Cont)}$	Gain control range		–5		5	dB
$E_{D(DC)}$	DC differential nonlinearity	A/D only		0.75	1	LSB
f(response)	Frequency response	Multiburst (60 IRE)		–0.9	–3	dB
	Noise spectrum	Luminance ramp (100 kHz full; tilt-null)		–57		dB
	Differential phase	Modulated ramp		0.7		°(pk-pk)
	Differential gain	Modulated ramp		0.5%		

3.3.3 Clocks, Video Data, Sync Timing

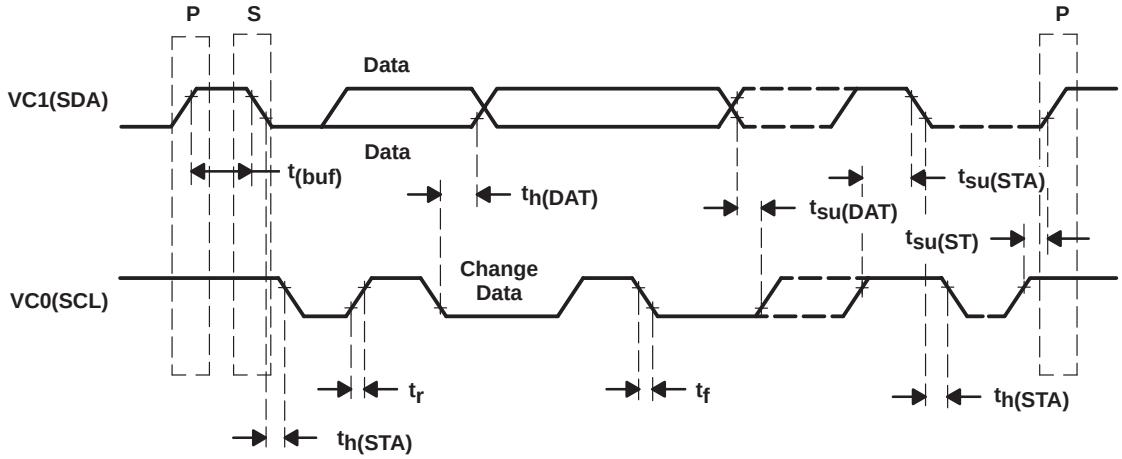
PARAMETER		TEST CONDITIONS (see NOTE 2)	MIN	TYP	MAX	UNIT
$t_{(SCLK)}$	Duty cycle PCLK, SCLK		40%	50%	60%	
$t_{r\ (SCLK)}$	Rise time SCLK	10% to 90%		3		ns
$t_{f(SCLK)}$	Fall time SCLK	90% to 10%		2		ns
$t_{r(PCLK)}$	Rise time PCLK	10% to 90%		3		ns
$t_{f(PCLK)}$	Fall time PCLK	90% to 10%		2		ns
$t_{d(PREF)}$	Delay time, SCLK rising edge to PREF				5	ns
$t_{d(PCLK)}$	Delay time, SCLK falling edge to PCLK	See Note 3	–2		3	ns
$t_{d}(YUV)$	Delay time, SCLK falling edge to Y, UV	See Note 3	–2		7	ns
$t_{d}(OUT)$	Delay time, SCLK falling edge to digital outputs except PCLK, PREF, Y, UV				7	ns

NOTES: 2. C_L = 50 pF
3. SCLK falling edge may occur up to 2 ns after PREF, Y, UV output transitions.



3.3.4 I²C Host Port Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(buf)}$	Bus free time between stop and start		1.3			µS
$t_{su(STA)}$	Setup time for a (repeated) start condition		0.6			µS
$t_{h(STA)}$	Hold time (repeated) start condition		0.6			µS
$t_{su(STO)}$	Setup time for a stop condition		0.6			µS
$t_{su(DAT)}$	Data setup time		100			ns
$t_{h(DAT)}$	Data hold time		0		0.9	µS
t_r	Rise time VC1(SDA) and VC0(SCL) signal				250	nS
t_f	Fall time VC1(SDA) and VC0(SCL) signal				250	nS
	Capacitive load for each bus line				400	pF
	I²C clock frequency				400	kHz



3.3.5 Parallel Host Interface A

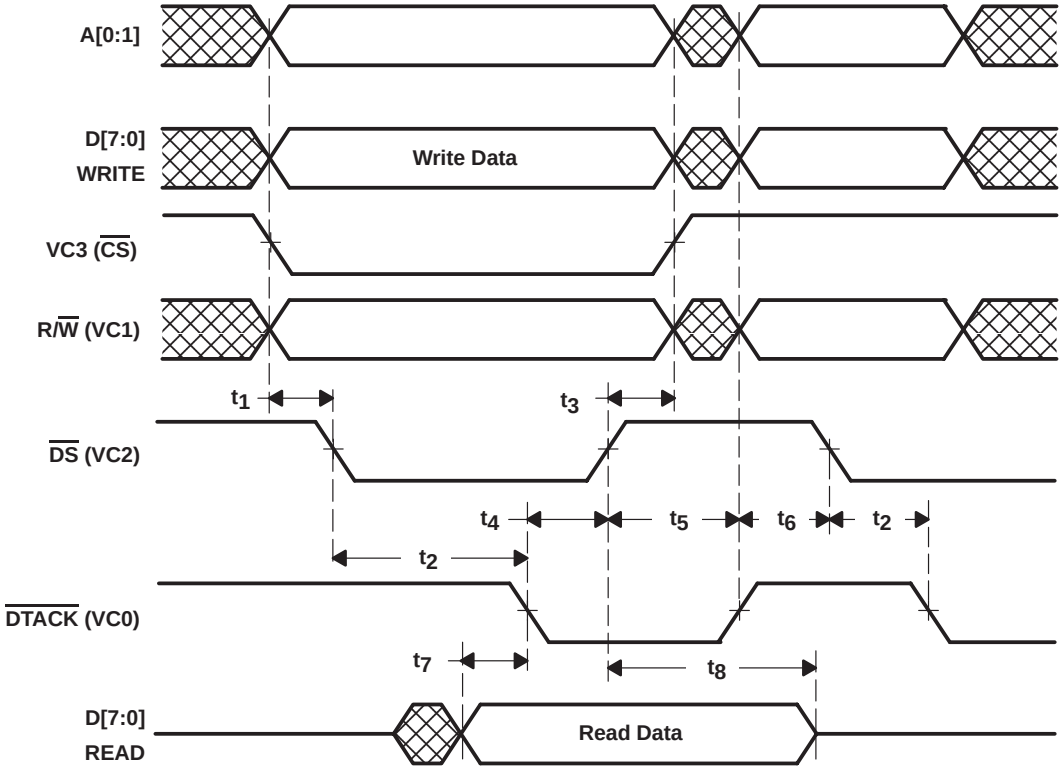


Figure 3–1. Parallel Host Interface A Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	A[1:0],D[0:7],VC1 setup until VC2 low		5			ns
t_2	Delay VC0 low after VC2 low		0			ns
t_3	A[1:0], D[0:7],VC1 hold after VC0 low		5			ns
t_5	Delay VC0 high after VC2 high		0			ns
t_6	Delay VC2 low(next cycle) after VC0 high		5			ns
t_8	(Read cycle) D[7:0] setup until VC0 low		10			ns

3.3.6 Parallel Host Interface B

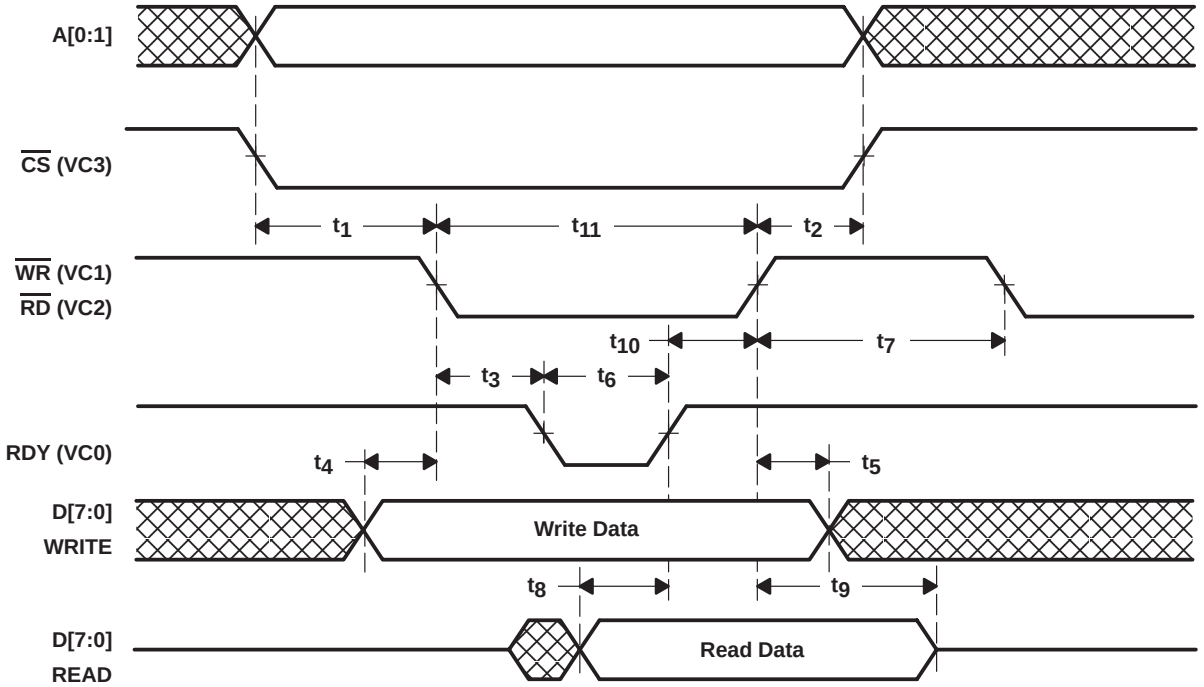


Figure 3–2. Parallel Host Interface B Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Delay VC1 or VC2 active after valid A[1:0]		10			ns
t_2	A[1:0] hold after VC1 or VC2 inactive		10			ns
t_3	Delay VC0 low after VC1 or VC2 active				28	ns
t_4	D[7:0] setup until VC1 active		5			ns
t_5	D[7:0] hold after VC1 inactive		10			ns
t_6	VC0 inactive pulse width		10			ns
t_7	VC1 inactive until any command active		80			ns
t_8	(Read cycle) VC1 low until D[7:0] non 3-state		5			ns
t_9	(Read cycle) D[7:0] setup until VC0 inactive		0			ns
t_{10}	(Read cycle) D[7:0] hold after VC1 inactive		0		15	ns
t_{11}	Hold VC1 active after VC0 active		0			ns

3.3.7 Parallel Host Interface C

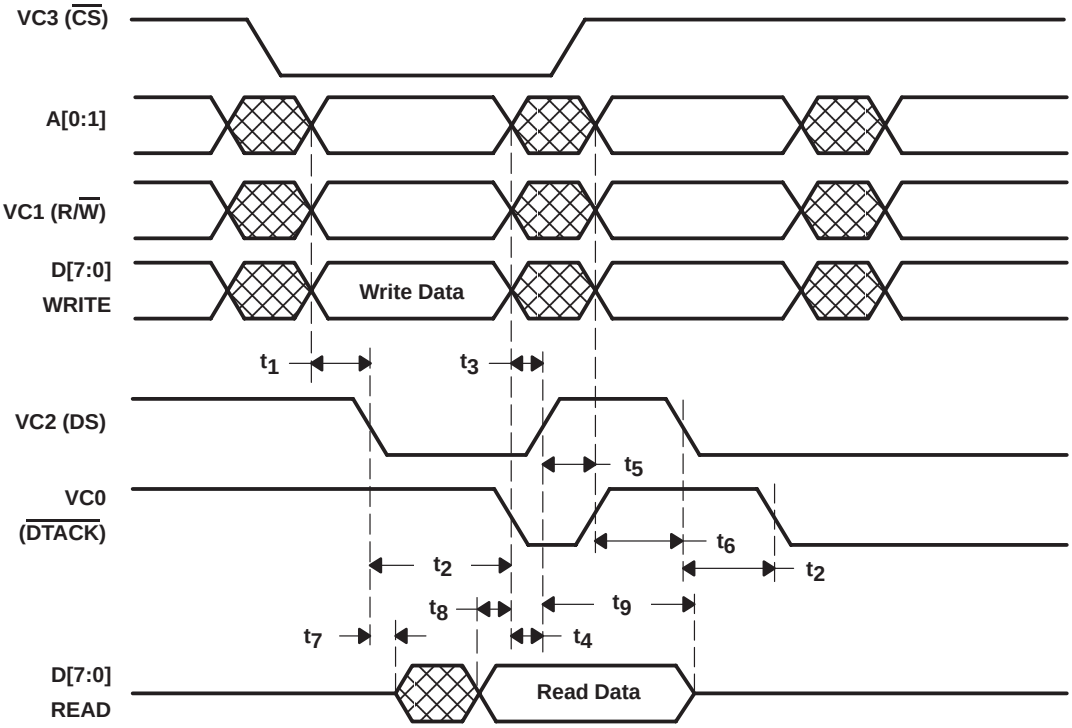
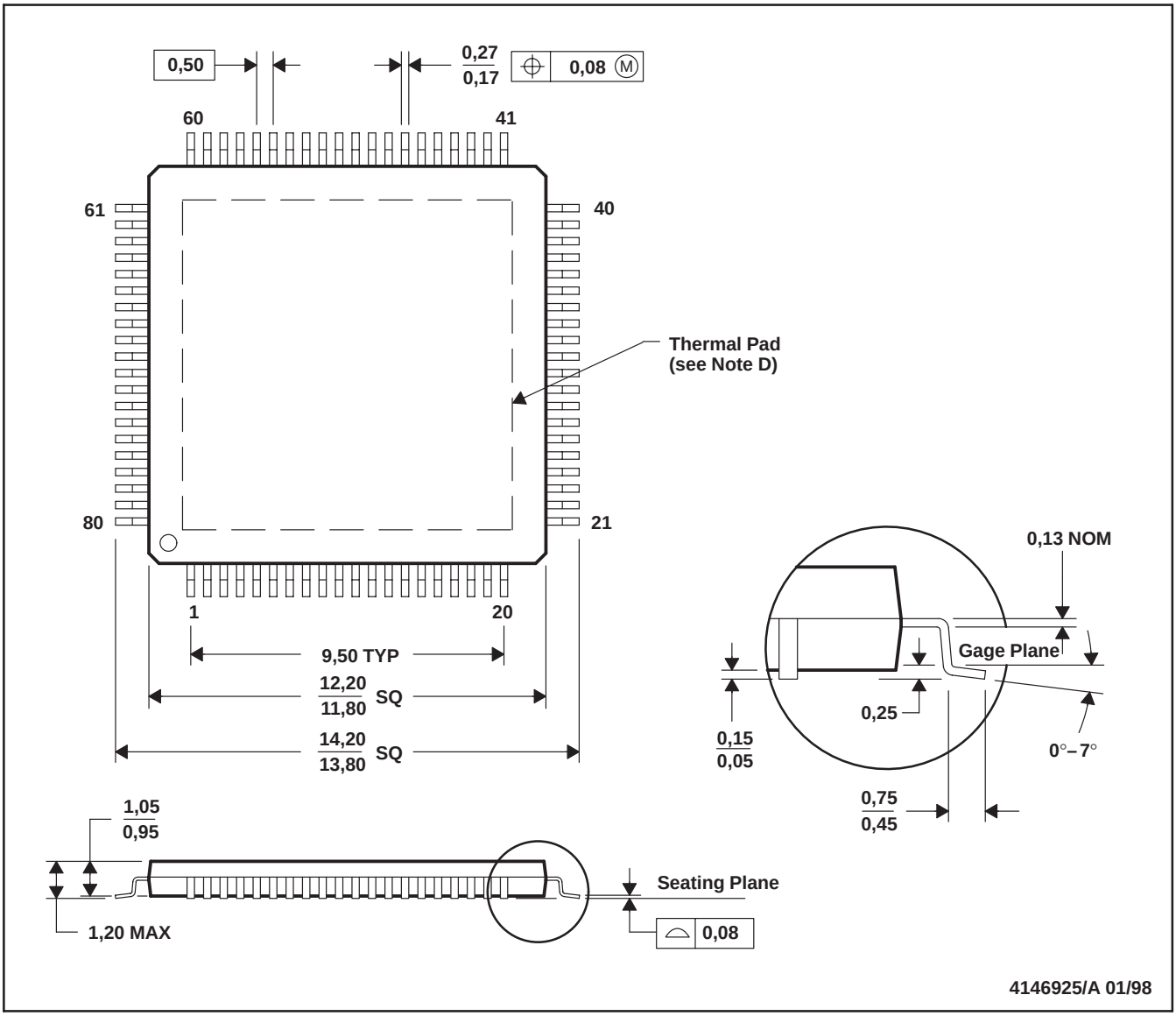


Figure 3–3. Parallel Host Interface C Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	A[1:0],D[0:7],VC1 setup until VC2 low		5			ns
t_2	Delay VC0 low after VC2 low		0			ns
t_3	A[1:0], D[0:7],VC1 hold after VC0 low		5			ns
t_5	Delay VC0 high after VC2 high		0			ns
t_6	Delay VC2 low(next cycle) after VC0 high		5			ns
t_8	(Read cycle) D[7:0] setup until VC0 low		10			ns
t_9	(Read cycle) D[7:0] hold after VC2 high		0			ns

4 Mechanical Data

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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