

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4018B

MSI

Presettable divide-by-N counter

Product specification
File under Integrated Circuits, IC04

January 1995

Presettable divide-by-N counter

HEF4018B
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PRESETTABLE DIVIDE-BY-N COUNTER

The HEF4018B is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs (P₀ to P₄), five active LOW buffered outputs ($\overline{O}_0$ to $\overline{O}_4$), and an overriding asynchronous master reset input (MR). Information on P₀ to P₄ is asynchronously loaded into the counter while PL is HIGH, independent of CP and D inputs. When P_L is LOW, the counter advances on the LOW to HIGH transition of CP. By connecting $\overline{O}_0$ to $\overline{O}_4$ to D, the counter operates as a divide-by-n counter (n = 2 to 10; see also function selection below). Each register stage is a D-type master-slave flip-flop with a set-direct/clear-direct input. An internal code correction circuit provides automatic code correction of the counter. From any illegal code the counter is in a proper counting mode within 11 clock pulses. A HIGH on MR resets the counter ($\overline{O}_0$ to $\overline{O}_4$ = HIGH) independent of all other inputs.

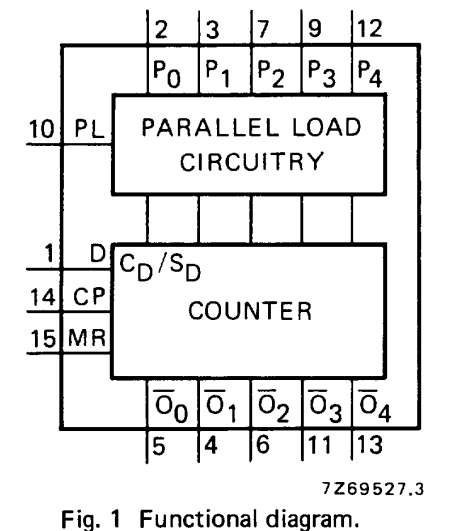


Fig. 1 Functional diagram.

FUNCTION SELECTION

counter mode; divide by	connect D input to	remarks
10 8 6 4 2	$\overline{O}_4$ $\overline{O}_3$ $\overline{O}_2$ $\overline{O}_1$ $\overline{O}_0$	no external components needed
9 7 5 3	$\overline{O}_3 \cdot \overline{O}_4$ $\overline{O}_2 \cdot \overline{O}_3$ $\overline{O}_1 \cdot \overline{O}_2$ $\overline{O}_0 \cdot \overline{O}_1$	AND gate needed; counter skips all HIGH states

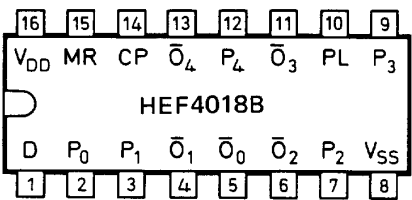


Fig. 2 Pinning diagram.

HEF4018BP(N): 16-lead DIL; plastic (SOT38-1)
 HEF4018BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
 HEF4018BT(D): 16-lead SO; plastic (SOT109-1)
 (): Package Designator North America

PINNING

PL parallel load input
 P₀ to P₄ parallel inputs
 D data input
 CP clock input (LOW to HIGH edge triggered)
 MR master reset input
 $\overline{O}_0$ to $\overline{O}_4$ buffered output (active LOW)

APPLICATION INFORMATION

Some examples of applications for the HEF4018B are:

- Programmable divide-by-n counter
- Programmable frequency division
- Timers

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Presetable divide-by-N counter

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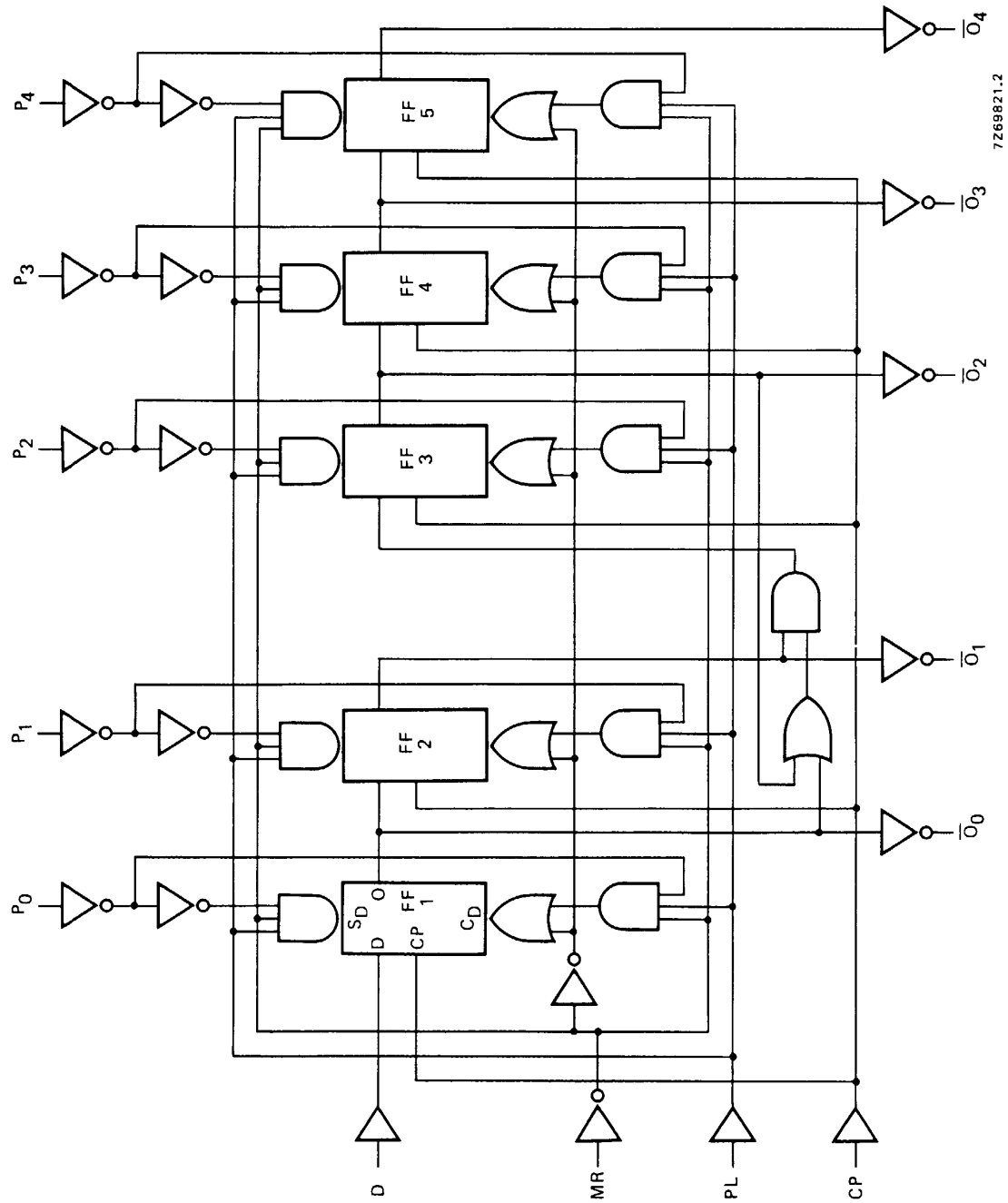


Fig. 3 Logic diagram.

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A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$3450 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
CP → $\bar{O}$	5	t _{PHL}		185	370	ns	158 ns + (0,55 ns/pF) C _L
HIGH to LOW	10			65	135	ns	54 ns + (0,23 ns/pF) C _L
	15			50	95	ns	42 ns + (0,16 ns/pF) C _L
	5	t _{PLH}		145	295	ns	118 ns + (0,55 ns/pF) C _L
LOW to HIGH	10			55	110	ns	44 ns + (0,23 ns/pF) C _L
	15			40	85	ns	32 ns + (0,16 ns/pF) C _L
PL → $\bar{O}$	5	t _{PHL}		205	415	ns	178 ns + (0,55 ns/pF) C _L
HIGH to LOW	10			70	140	ns	59 ns + (0,23 ns/pF) C _L
	15			50	105	ns	42 ns + (0,16 ns/pF) C _L
	5	t _{PLH}		175	350	ns	148 ns + (0,55 ns/pF) C _L
LOW to HIGH	10			65	125	ns	54 ns + (0,23 ns/pF) C _L
	15			50	95	ns	42 ns + (0,16 ns/pF) C _L
MR → $\bar{O}$	5	t _{PLH}		140	280	ns	113 ns + (0,55 ns/pF) C _L
LOW to HIGH	10			55	105	ns	44 ns + (0,23 ns/pF) C _L
	15			40	80	ns	32 ns + (0,16 ns/pF) C _L
Output transition times	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
HIGH to LOW	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
LOW to HIGH	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L

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	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Set-up time D $\rightarrow$ CP	5 10 15	t_{su}	130 40 30	65 20 15	ns ns ns	see also waveforms Figs 4, 5 and 6
Hold time D $\rightarrow$ CP	5 10 15	t_{hold}	20 5 5	-45 -15 -10	ns ns ns	
Minimum clock pulse width; LOW	5 10 15	t_{WCPL}	140 50 40	70 25 20	ns ns ns	
Minimum MR pulse width; HIGH	5 10 15	t_{WMRH}	100 35 25	50 20 15	ns ns ns	
Minimum PL pulse width; HIGH	5 10 15	t_{WPLH}	145 50 35	75 25 20	ns ns ns	
Recovery time for MR	5 10 15	t_{RMR}	135 40 25	70 20 15	ns ns ns	
Recovery time for PL	5 10 15	t_{RPL}	170 55 40	85 30 20	ns ns ns	
Maximum clock pulse frequency	5 10 15	f_{max}	2 6 8	4 11 16	MHz MHz MHz	

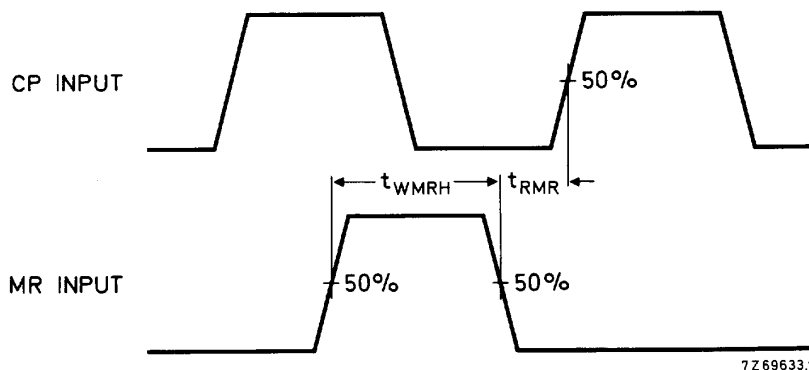


Fig. 4 Waveforms showing minimum MR pulse width and MR recovery time.

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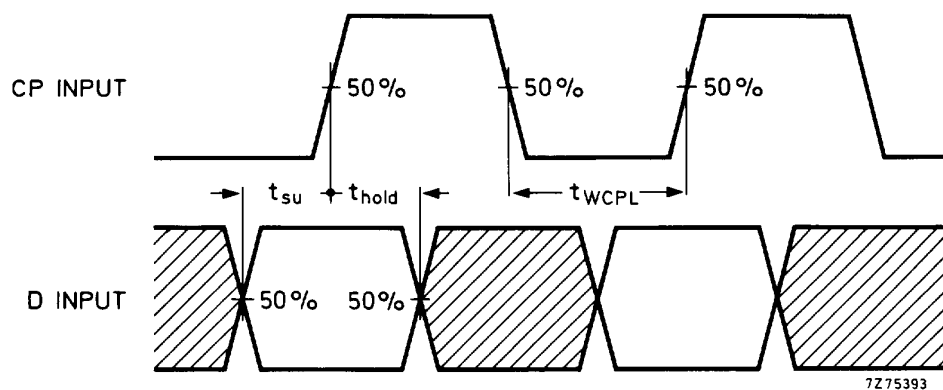
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Fig. 5 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.

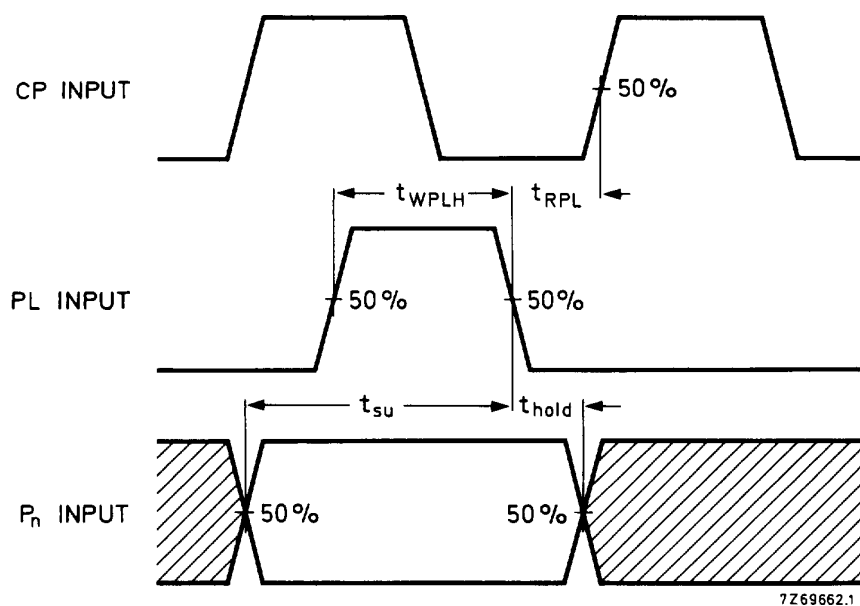


Fig. 6 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

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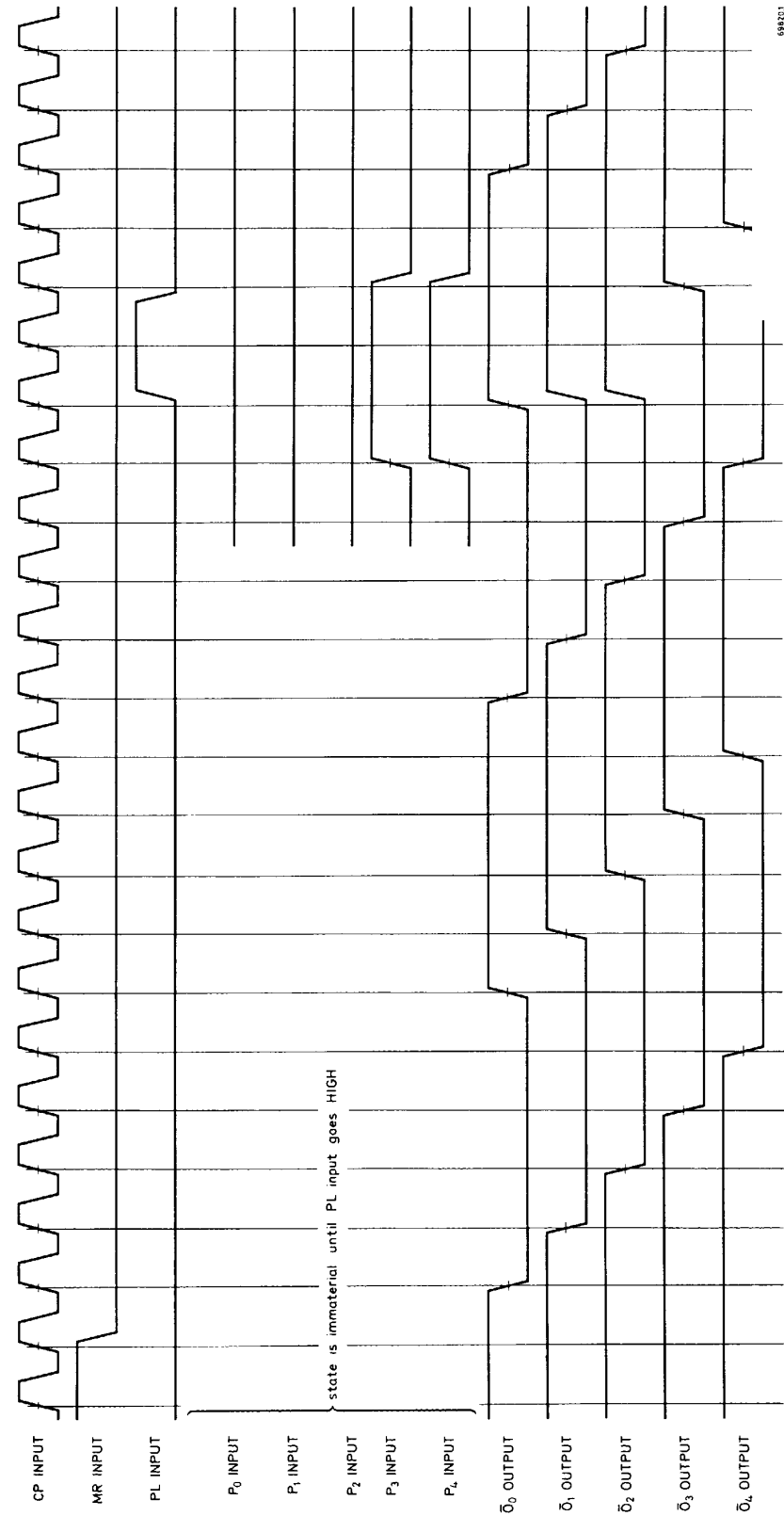


Fig. 7 Timing diagram.

Note

D input connected to $\overline{Q}_4$ for decade counter configuration.