PSMN013-100YSE

N-channel 100 V 13 mΩ standard level MOSFET in LFPAK56

18 December 2012 Product data sheet

1. General description

Standard level N-channel MOSFET in a LFPAK56 package qualified to 175 °C. Part of NXP's "NextPower Live" portfolio, the PSMN013-100YSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, whilst offering a low $R_{DS(on)}$ characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on a 48 V backplane / supply rail.

2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low $R_{DS(on)}$ for low conduction losses

3. Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	100	V
I_D	drain current	T_{mb} = 100 °C; V_{GS} = 10 V; Fig. 1		-	-	58	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	238	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	11	13	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 20 A; V_{DS} = 50 V; Fig. 14; Fig. 15		-	26	-	nC
$Q_{G(tot)}$	total gate charge			-	75	-	nC

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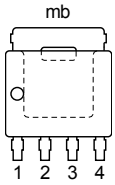
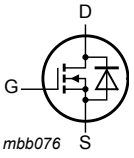
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche Ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 82 A; $V_{sup} \leq$ 100 V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	-	125	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100YSE	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-100YSE	13100

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq$ 25 °C; $T_j \leq$ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq$ 25 °C; $T_j \leq$ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_j = 25 °C; Fig. 1		-	82	A

Symbol	Parameter	Conditions		Min	Max	Unit
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 1		-	58	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C; Fig. 4		-	330	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	238	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	330	A
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 82 A; $V_{sup} \leq 100$ V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	125	mJ

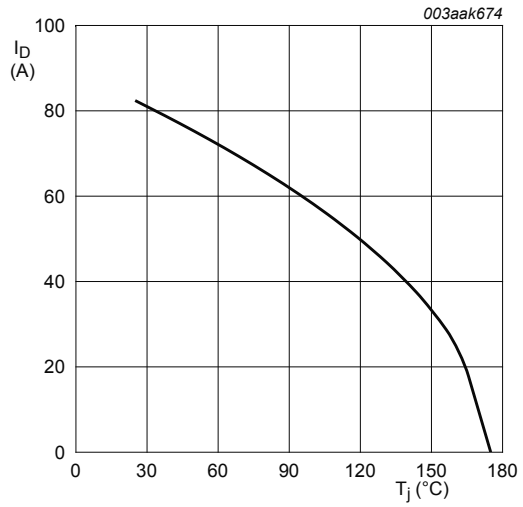


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

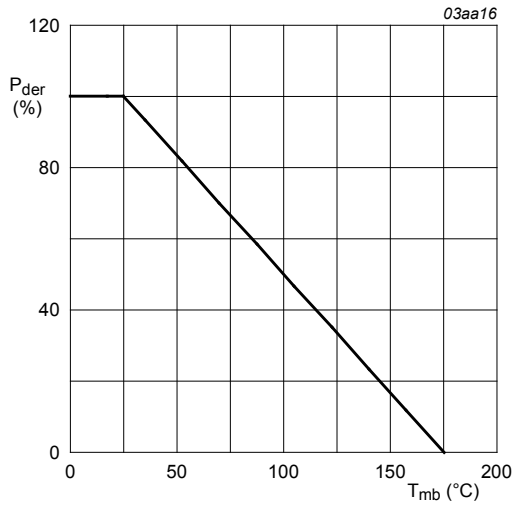


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

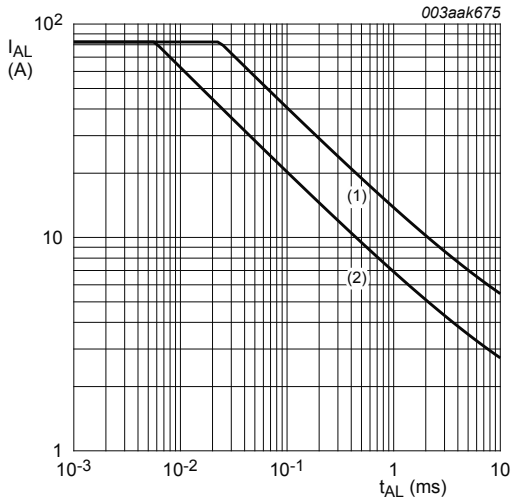


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

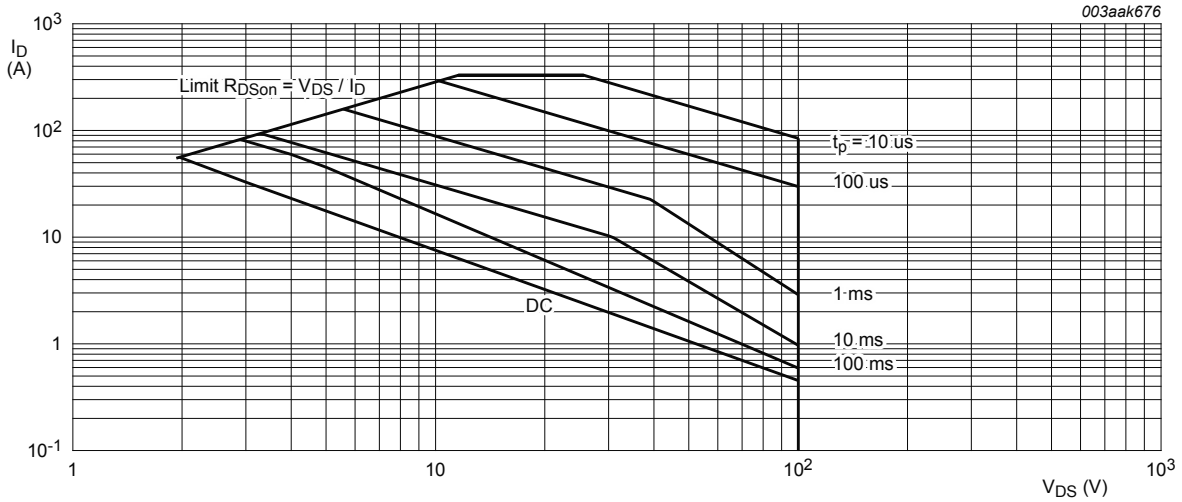


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} *is a single pulse*

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.56	0.63	K/W

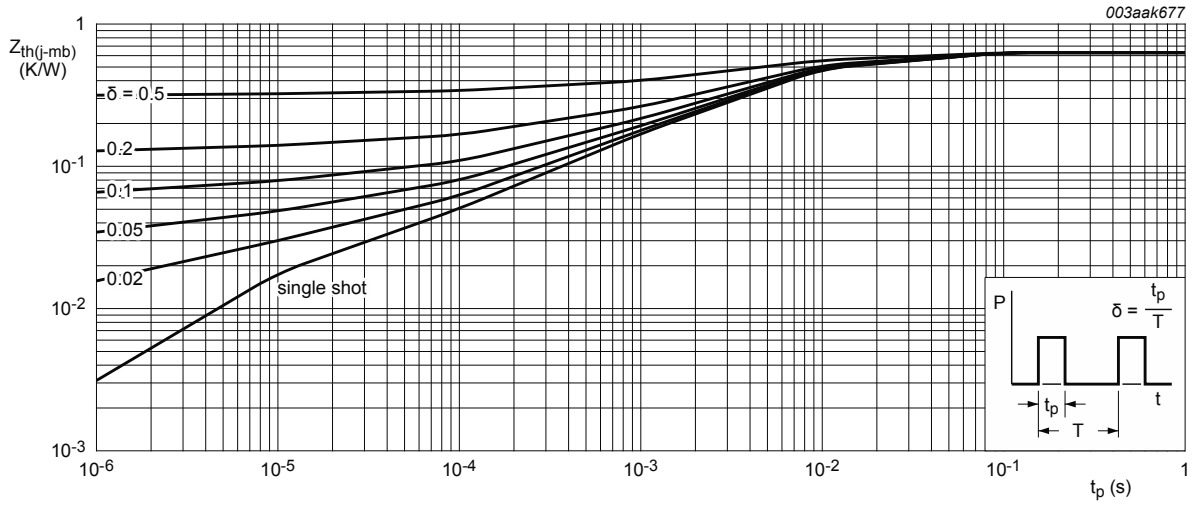


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		2	3	4	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 11		1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 11		-	-	4.6	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.03	2	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C; Fig. 12		-	11	13	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 100 °C; Fig. 12; Fig. 13		-	-	23	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 175 °C; Fig. 12; Fig. 13		-	-	36	mΩ
R_G	gate resistance	f = 1 MHz		0.33	0.66	1.32	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	75	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	60	-	nC
Q_{GS}	gate-source charge	I_D = 20 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	16	-	nC
Q_{GD}	gate-drain charge			-	26	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 20 A; V_{DS} = 50 V; Fig. 14; Fig. 15		-	4.7	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	3775	-	pF
C_{oss}	output capacitance			-	265	-	pF
C_{rss}	reverse transfer capacitance			-	192	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2.9 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	16	-	ns
t_r	rise time			-	23	-	ns
$t_{d(off)}$	turn-off delay time			-	42	-	ns
t_f	fall time			-	21	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 20 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.82	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/μs; V_{GS} = 0 V; V_{DS} = 50 V		-	61	-	ns
Q_r	recovered charge			-	146	-	nC

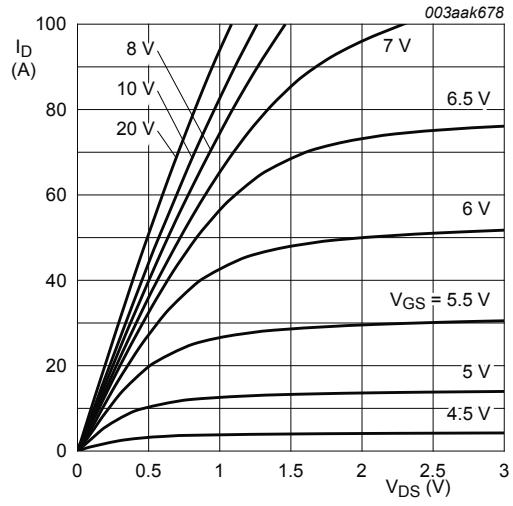


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

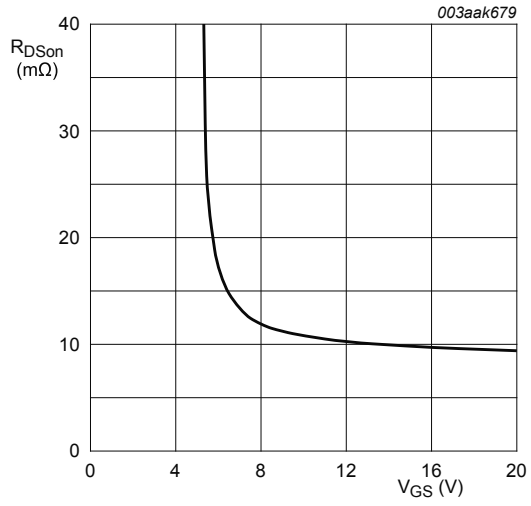


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 20A$

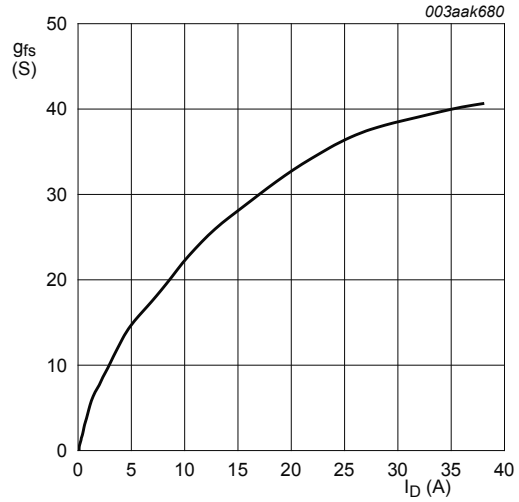


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

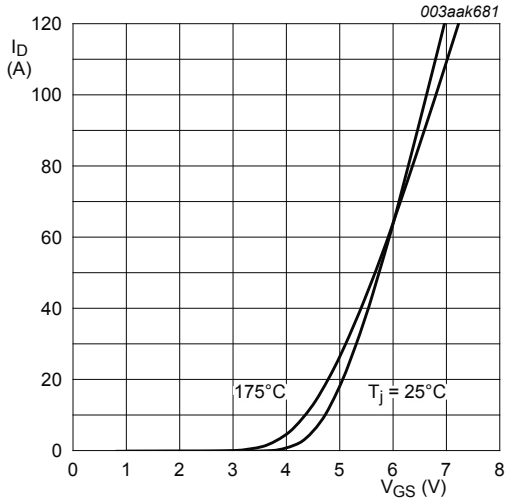


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

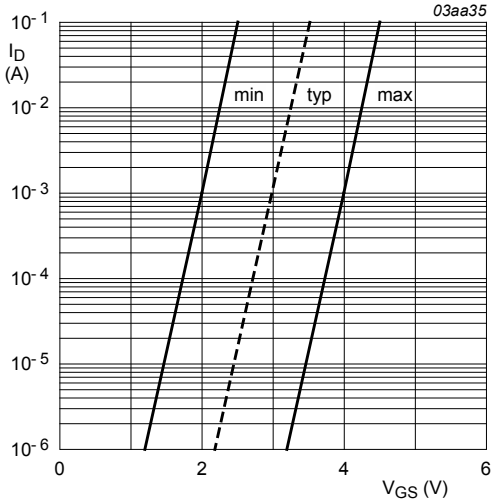


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\,°C; V_{DS} = 5V$

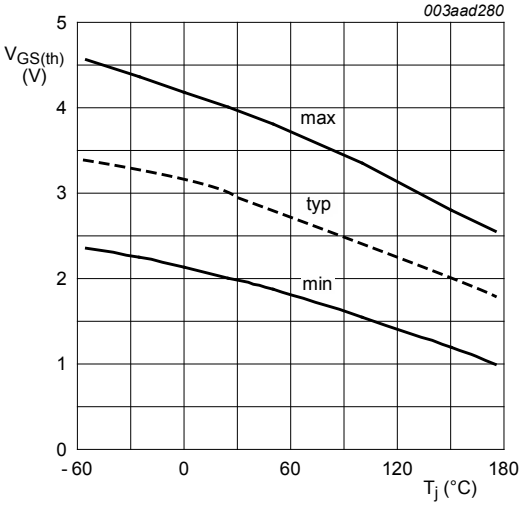


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\,\text{mA};\ V_{DS} = V_{GS}$

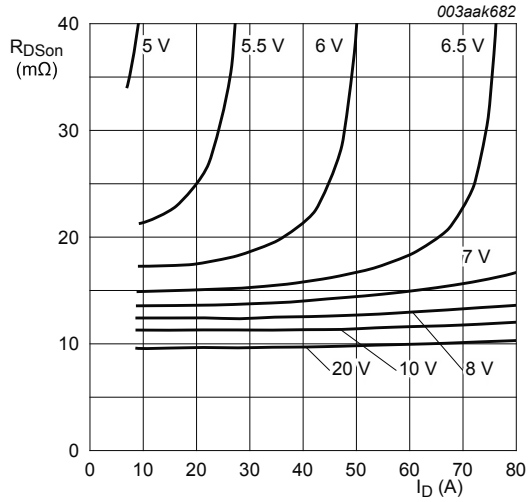


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

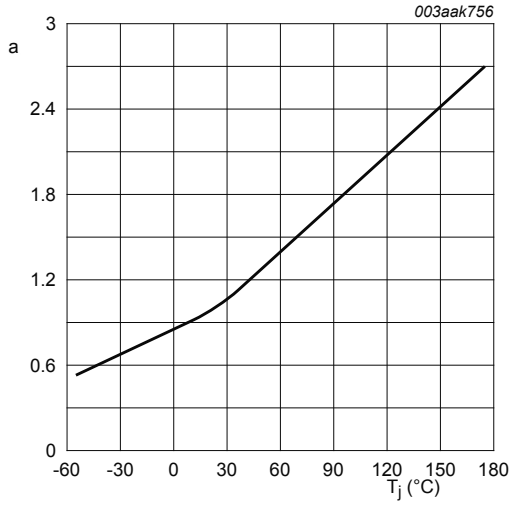


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

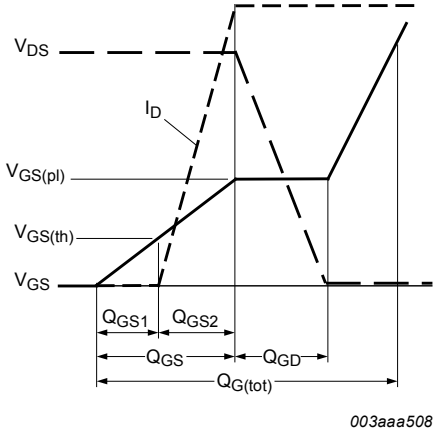


Fig. 14. Gate charge waveform definitions

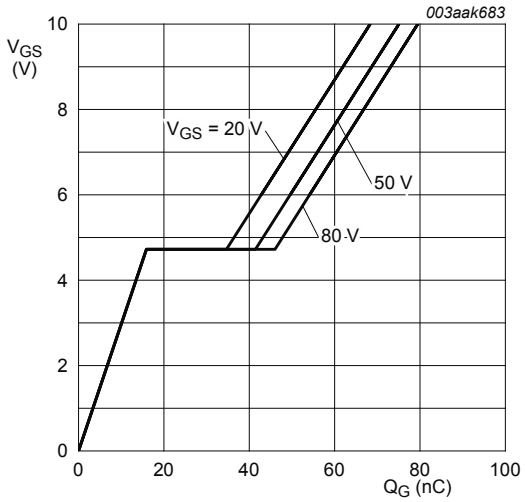


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 20A$

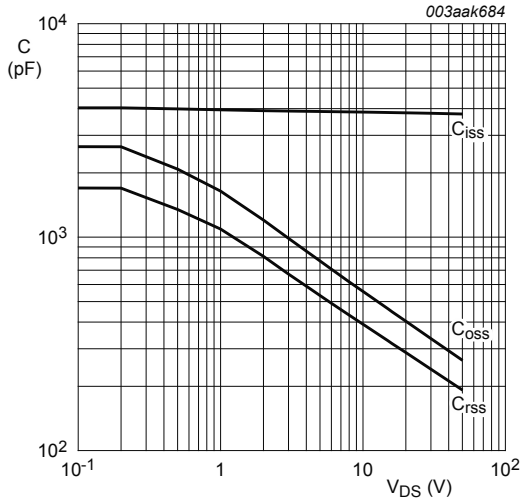


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

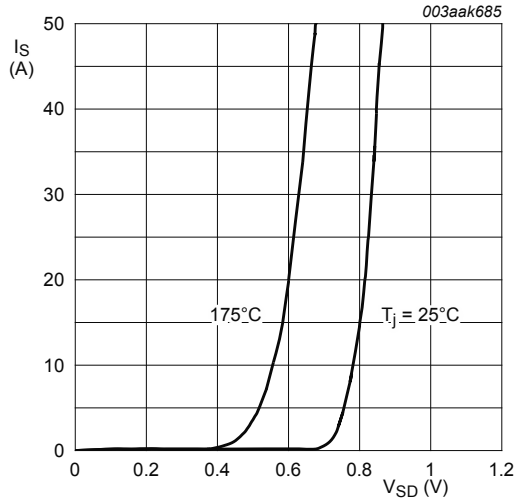
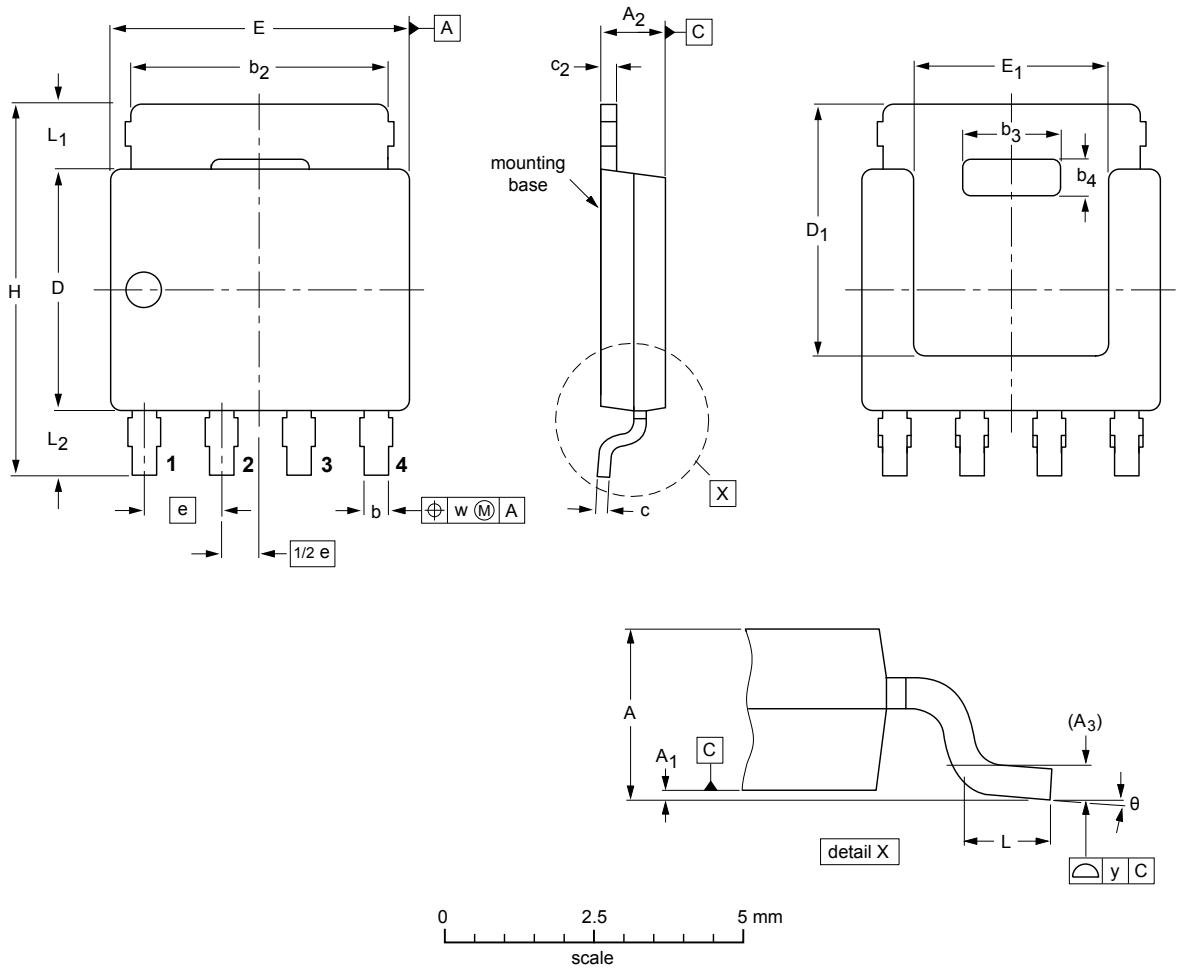


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

11. Package outline

Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1^{(1)}$ max	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~06-03-16~~ 11-03-25

Fig. 18. Package outline LFPAK; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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