

## 100 MHz Differential Buffer for PCI Express and SATA

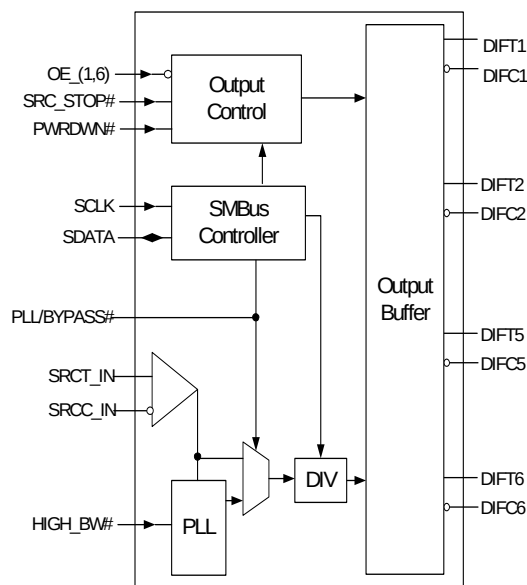
### Features

- CK409 or CK410 companion buffer
- Four differential 0.7V clock pairs
- Individual OE controls
- Low CTC jitter (< 50 ps)
- Programmable bandwidth
- SRC\_STOP# power management control
- SMBus Block/Byte/Word Read and Write support
- 3.3V operation
- PLL Bypass-configurable
- Divide by 2 programmable outputs
- 28-pin SSOP package

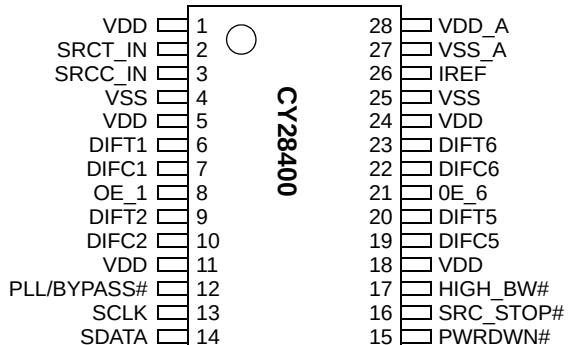
### Functional Description

The CY28400 is a differential buffer and serves as a companion device to the CK409 or CK410 clock generator. The device is capable of distributing the Serial Reference Clock (SRC) in PCI Express and SATA implementations.

### Block Diagram



### Pin Configuration



28 SSOP

## Pin Descriptions

| Pin                  | Name                | Type   | Description                                                                                                                              |
|----------------------|---------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------|
| 2,3                  | SRCT_IN, SRCC_IN    | I,DIF  | <b>0.7V differential SRC inputs from the clock synthesizer</b>                                                                           |
| 6,7,9,10,19,20,22,23 | DIFT/C(2:1) & (6:5) | O,DIF  | <b>0.7V differential clock outputs</b>                                                                                                   |
| 8,21                 | OE_1, OE_6          | I,SE   | <b>3.3V LVTTL active LOW input for three-stating differential outputs</b> (DIFT2 and DIFT5 are unaffected by the assertion of OE inputs) |
| 17                   | HIGH_BW#            | I,SE   | <b>3.3V LVTTL input for selecting PLL bandwidth</b>                                                                                      |
| 16                   | SRC_STOP#           | I,SE   | <b>3.3V LVTTL input for SRC_STOP#, active LOW</b>                                                                                        |
| 15                   | PWRDWN#             | I,SE   | <b>3.3V LVTTL input for Power Down, active LOW</b>                                                                                       |
| 13                   | SCLK                | I,SE   | <b>SMBus slave clock input</b>                                                                                                           |
| 14                   | SDATA               | I/O,OC | <b>Open collector SMBus data</b>                                                                                                         |
| 26                   | IREF                | I      | <b>A precision resistor is attached to this pin to set the differential output current</b>                                               |
| 12                   | PLL/BYPASS#         | I      | <b>3.3V LVTTL input for selecting fan-out or PLL operation</b>                                                                           |
| 28                   | VDD_A               | 3.3V   | <b>3.3V power supply for PLL</b>                                                                                                         |
| 27                   | VSS_A               | GND    | <b>Ground for PLL</b>                                                                                                                    |
| 4,25                 | VSS                 | 3.3V   | <b>Ground for outputs</b>                                                                                                                |
| 1,5,11,18,24         | VDD                 | GND    | <b>3.3V power supply for outputs</b>                                                                                                     |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11011100 (DCh).

**Table 1. Command Code Definition**

| Bit   | Description                                                                                                                 |
|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 7     | 0 = Block read or block write operation<br>1 = Byte read or byte write operation                                            |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol |                                                                | Block Read Protocol |                                                                |
|----------------------|----------------------------------------------------------------|---------------------|----------------------------------------------------------------|
| Bit                  | Description                                                    | Bit                 | Description                                                    |
| 1                    | Start                                                          | 1                   | Start                                                          |
| 2:8                  | Slave address – 7 bits                                         | 2:8                 | Slave address – 7 bits                                         |
| 9                    | Write = 0                                                      | 9                   | Write = 0                                                      |
| 10                   | Acknowledge from slave                                         | 10                  | Acknowledge from slave                                         |
| 11:18                | Command Code – 8 bits<br>'00000000' stands for block operation | 11:18               | Command Code – 8 bits<br>'00000000' stands for block operation |
| 19                   | Acknowledge from slave                                         | 19                  | Acknowledge from slave                                         |

**Table 2. Block Read and Block Write Protocol** (continued)

| Block Write Protocol |                                    | Block Read Protocol |                                   |
|----------------------|------------------------------------|---------------------|-----------------------------------|
| Bit                  | Description                        | Bit                 | Description                       |
| 20:27                | Byte Count from master – 8 bits    | 20                  | Repeat start                      |
| 28                   | Acknowledge from slave             | 21:27               | Slave address – 7 bits            |
| 29:36                | Data byte 0 from master – 8 bits   | 28                  | Read = 1                          |
| 37                   | Acknowledge from slave             | 29                  | Acknowledge from slave            |
| 38:45                | Data byte 1 from master – 8 bits   | 30:37               | Byte count from slave – 8 bits    |
| 46                   | Acknowledge from slave             | 38                  | Acknowledge from host             |
| ....                 | Data bytes from master/Acknowledge | 39:46               | Data byte 0 from slave – 8 bits   |
| ....                 | Data Byte N – 8 bits               | 47                  | Acknowledge from host             |
| ....                 | Acknowledge from slave             | 48:55               | Data byte 1 from slave – 8 bits   |
| ....                 | Stop                               | 56                  | Acknowledge from host             |
|                      |                                    | ....                | Data bytes from slave/Acknowledge |
|                      |                                    | ....                | Data byte N from slave – 8 bits   |
|                      |                                    | ....                | Acknowledge from host             |
|                      |                                    | ....                | Stop                              |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                                                                                                                                               | Byte Read Protocol |                                                                                                                                               |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                 | Description                                                                                                                                   | Bit                | Description                                                                                                                                   |
| 1                   | Start                                                                                                                                         | 1                  | Start                                                                                                                                         |
| 2:8                 | Slave address – 7 bits                                                                                                                        | 2:8                | Slave address – 7 bits                                                                                                                        |
| 9                   | Write = 0                                                                                                                                     | 9                  | Write = 0                                                                                                                                     |
| 10                  | Acknowledge from slave                                                                                                                        | 10                 | Acknowledge from slave                                                                                                                        |
| 11:18               | Command Code – 8 bits<br>'100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed |
| 19                  | Acknowledge from slave                                                                                                                        | 19                 | Acknowledge from slave                                                                                                                        |
| 20:27               | Data byte from master – 8 bits                                                                                                                | 20                 | Repeat start                                                                                                                                  |
| 28                  | Acknowledge from slave                                                                                                                        | 21:27              | Slave address – 7 bits                                                                                                                        |
| 29                  | Stop                                                                                                                                          | 28                 | Read = 1                                                                                                                                      |
|                     |                                                                                                                                               | 29                 | Acknowledge from slave                                                                                                                        |
|                     |                                                                                                                                               | 30:37              | Data byte from slave – 8 bits                                                                                                                 |
|                     |                                                                                                                                               | 38                 | Acknowledge from master                                                                                                                       |
|                     |                                                                                                                                               | 39                 | Stop                                                                                                                                          |

**Byte 0: Control Register 0**

| Bit | @Pup | Name     | Description                                                      |
|-----|------|----------|------------------------------------------------------------------|
| 7   | 0    |          | PWRDWN# drive mode<br>0 = Driven when stopped, 1 = Three-state   |
| 6   | 0    |          | SRC_STOP# drive mode<br>0 = Driven when stopped, 1 = Three-state |
| 5   | 0    |          | Reserved                                                         |
| 4   | 0    |          | Reserved                                                         |
| 3   | 0    |          | Reserved                                                         |
| 2   | 1    | HIGH_BW# | HIGH_BW#<br>0 = High Bandwidth, 1 = Low bandwidth                |

**Byte 0: Control Register 0** (continued)

| Bit | @Pup | Name        | Description                                                     |
|-----|------|-------------|-----------------------------------------------------------------|
| 1   | 1    | PLL/Bypass# | PLL/Bypass#<br>0 = Fanout buffer, 1 = PLL mode                  |
| 0   | 1    |             | SRC_DIV/2<br>0 = Divided by 2 mode, 1 = Normal (output = input) |

**Byte 1: Control Register 1**

| Bit | @Pup | Name    | Description                                                      |
|-----|------|---------|------------------------------------------------------------------|
| 7   | 1    |         | Reserved                                                         |
| 6   | 1    | DIFT/C6 | DIFT/C6 Output Enable<br>0 = Disabled (three-state), 1 = Enabled |
| 5   | 1    | DIFT/C5 | DIFT/C5 Output Enable<br>0 = Disabled (three-state), 1 = Enabled |
| 4   | 1    |         | Reserved                                                         |
| 3   | 1    |         | Reserved                                                         |
| 2   | 1    | DIFT/C2 | DIFT/C2 Output Enable<br>0 = Disabled (three-state), 1 = Enabled |
| 1   | 1    | DIFT/C1 | DIFT/C1 Output Enable<br>0 = Disabled (three-state), 1 = Enabled |
| 0   | 1    |         | Reserved                                                         |

**Byte 2: Control Register 2**

| Bit | @Pup | Name | Description                                                                                       |
|-----|------|------|---------------------------------------------------------------------------------------------------|
| 7   | 0    |      | Reserved                                                                                          |
| 6   | 0    |      | Allow Control DIFT/C6 with assertion of SRC_STOP#<br>0 = Free-running, 1 = Stopped with SRC_STOP# |
| 5   | 0    |      | Allow Control DIFT/C5 with assertion of SRC_STOP#<br>0 = Free-running, 1 = Stopped with SRC_STOP# |
| 4   | 0    |      | Reserved                                                                                          |
| 3   | 0    |      | Reserved                                                                                          |
| 2   | 0    |      | Allow Control DIFT/C2 with assertion of SRC_STOP#<br>0 = Free-running, 1 = Stopped with SRC_STOP# |
| 1   | 0    |      | Allow Control DIFT/C1 with assertion of SRC_STOP#<br>0 = Free-running, 1 = Stopped with SRC_STOP# |
| 0   | 0    |      | Reserved                                                                                          |

**Byte 3: Control Register 3**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7   | 0    |      | Reserved    |
| 6   | 0    |      | Reserved    |
| 5   | 0    |      | Reserved    |
| 4   | 0    |      | Reserved    |
| 3   | 0    |      | Reserved    |
| 2   | 0    |      | Reserved    |
| 1   | 0    |      | Reserved    |
| 0   | 0    |      | Reserved    |

**Byte 4: Vendor ID Register**

| Bit | @Pup | Name | Description         |
|-----|------|------|---------------------|
| 7   | 0    |      | Revision Code Bit 3 |
| 6   | 0    |      | Revision Code Bit 2 |
| 5   | 0    |      | Revision Code Bit 1 |
| 4   | 0    |      | Revision Code Bit 0 |
| 3   | 1    |      | Vendor ID Bit 3     |
| 2   | 0    |      | Vendor ID Bit 2     |
| 1   | 0    |      | Vendor ID Bit 1     |
| 0   | 0    |      | Vendor ID Bit 0     |

**Byte 5: Control Register 5**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7   | 0    |      | Reserved    |
| 6   | 0    |      | Reserved    |
| 5   | 0    |      | Reserved    |
| 4   | 0    |      | Reserved    |
| 3   | 0    |      | Reserved    |
| 2   | 0    |      | Reserved    |
| 1   | 0    |      | Reserved    |
| 0   | 0    |      | Reserved    |

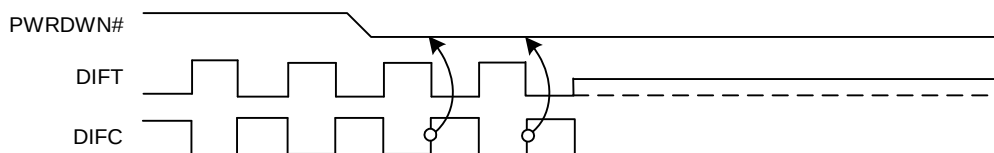
**PWRDWN# Clarification<sup>[1]</sup>**

The PWRDWN# pin is used to shut off all clocks cleanly and instruct the device to evoke power savings mode. Additionally, PWRDWN# should be asserted prior to shutting off the input clock or power to ensure all clocks shut down in a glitch-free manner. PWRDWN# is an asynchronous active LOW input. This signal is synchronized internal to the device prior to powering down the clock buffer. PWRDWN# is an

asynchronous input for powering up the system. When PWRDWN# is asserted LOW, all clocks will be held HIGH or three-stated (depending on the state of the control register drive mode and OE bits) prior to turning off the VCO. All clocks will start and stop without any abnormal behavior and must meet all AC and DC parameters. This means no glitches, frequency shifting or amplitude abnormalities among others.

**PWRDWN# Assertion**

When PWRDWN# is sampled LOW by two consecutive rising edges of DIFC, all DIFT outputs will be held HIGH or three-stated (depending on the state of the control register drive mode and OE bits) on the next DIFC HIGH-to-LOW transition. When the SMBus power-down drive mode bit is programmed to '0', all clock outputs will be held with the DIFT pin driven HIGH at 2 x Iref and DIFC three-state. However, if the control register PWRDWN# drive mode bit is programmed to '1', then both DIFT and the DIFC are three-stated.


**Figure 1. PWRDWN# Assertion Diagram**
**Note:**

1. Disabling of the SRCT\_IN input clock prior to assertion of PWRDWN# is an undefined mode and not recommended. Operation in this mode may result in glitches excessive frequency shifting.

## PWRDWN#—Deassertion

The power-up latency is less than 1 ms. This is the time from the deassertion of the PWRDWN# pin or the ramping of the power supply or the time from valid SRC\_IN input clocks until the time that stable clocks are output from the buffer chip (PLL locked). If the control register PWRDWN# three-state bit is programmed to '1', all differential outputs will be driven HIGH in less than 300  $\mu$ s of PWRDWN# deassertion to a voltage greater than 200 mV.

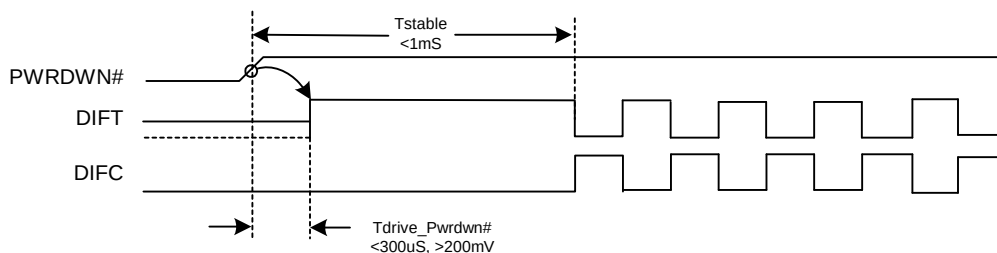


Figure 2. PWRDWN# Deassertion Diagram

Table 4. Buffer Power-up State Machine

| State            | Description                                                                                                          |
|------------------|----------------------------------------------------------------------------------------------------------------------|
| 0                | 3.3V Buffer power off                                                                                                |
| 1                | After 3.3V supply is detected to rise above 1.8V–2.0V, the buffer enters state 1 and initiates a 0.2-ms–0.3-ms delay |
| 2 <sup>[3]</sup> | Buffer <b>waits for a valid clock on the SRC_IN input</b> and PWRDWN# deassertion                                    |
| 3 <sup>[2]</sup> | Once the PLL is locked to the SRC_IN input clock, the buffer enters state 3 and enables outputs for normal operation |

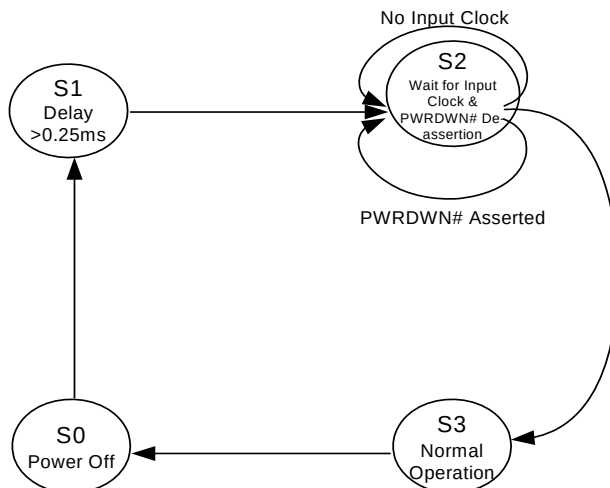


Figure 3. Buffer Power-up State Diagram

### Notes:

- The total power-up latency from power on to all outputs active is less than 1 ms (assuming a valid clock is present on SRC\_IN input).
- If power is valid and PWRDWN# is deasserted but no input clocks are present on the SRC\_IN input, DIF clocks will remain disabled. Only after valid input clocks are detected, valid power, PWRDWN# deasserted with the PLL locked and stable are the DIF outputs enabled.

## SRC\_STOP# Clarification

The SRC\_STOP# signal is an active LOW input used for clean stopping and starting the DIF outputs (valid clock must be present on SRCT\_IN). The SRC\_STOP# signal is a de-bounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

**Table 5. SRC\_STOP# Functionality<sup>[4]</sup>**

| SRC_STOP# | DIFT              | DIFC   |
|-----------|-------------------|--------|
| 1         | Normal            | Normal |
| 0         | Iref * 6 or Float | Low    |

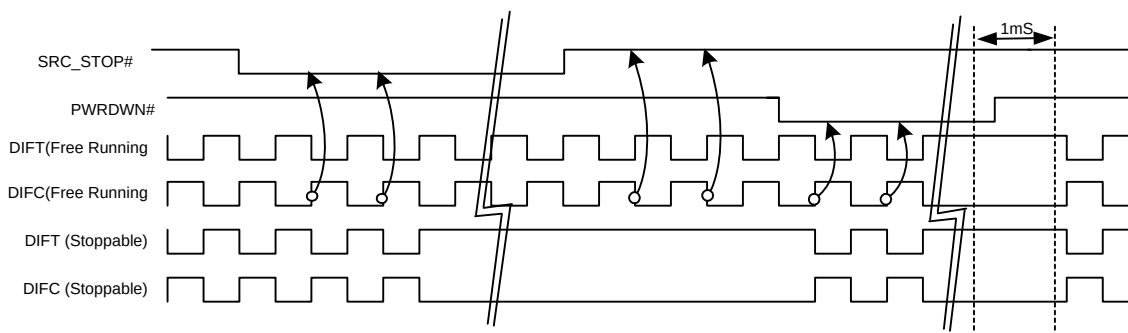
## SRC\_STOP# Assertion

The impact of asserting the SRC\_STOP# pin is all DIF outputs that are set in the control registers to stoppable via assertion of SRC\_STOP# are stopped after their next transition. When

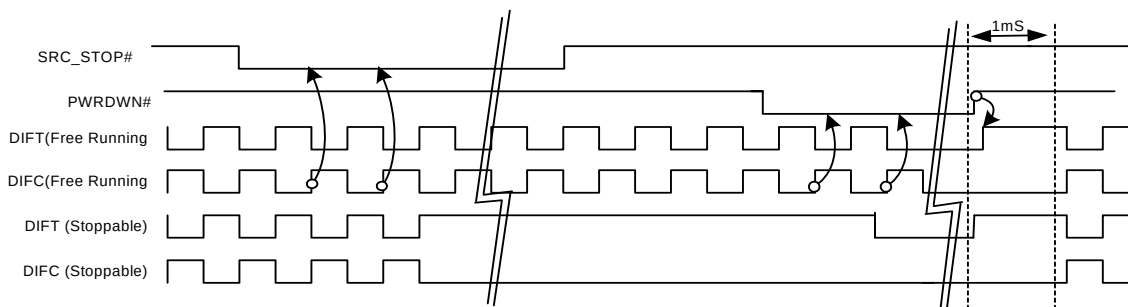
the control register SRC\_STOP# three-state bit is programmed to '0', the final state of all stopped DIFT/C signals is DIFT clock = HIGH and DIFC = LOW. There is to be no change to the output drive current values, DIFT will be driven HIGH with a current value equal  $6 \times I_{ref}$ , and DIFC will not be driven. When the control register SRC\_STOP# three-state bit is programmed to '1', the final state of all stopped DIF signals is LOW, both DIFT clock and DIFC clock outputs will not be driven.

## SRC\_STOP# Deassertion

All differential outputs that were stopped will resume normal operation in a glitch-free manner. The maximum latency from the deassertion to active outputs is between 2–6 DIFT/C clock periods (two clocks are shown) with all DIFT/C outputs resuming simultaneously. If the control register three-state bit is programmed to '1' (three-state), then all stopped DIFT outputs will be driven high within 10 ns of SRC\_STOP# deassertion to a voltage greater than 200 mV.



**Figure 4. SRC\_STOP# = Driven, PWRDWN# = Driven**



**Figure 5. SRC\_STOP# = Driven, PWRDWN# = Three-state**

**Note:**

4. In the case where OE is asserted HIGH, the output will always be three-stated regardless of SRC\_STOP# drive mode register bit state.

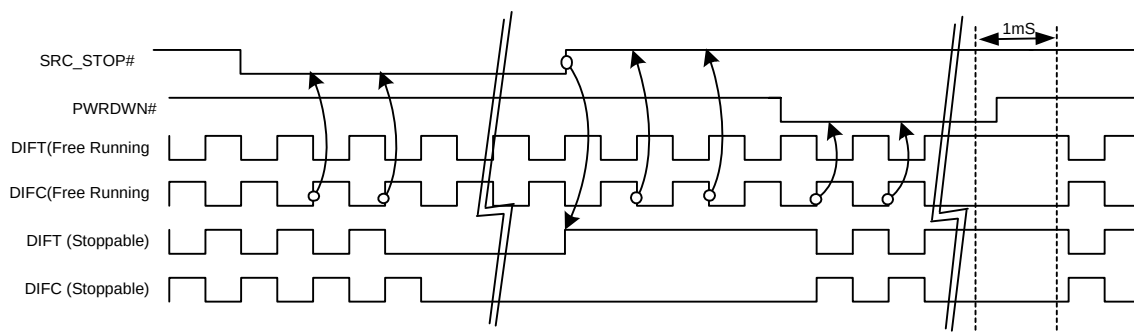


Figure 6. SRC\_STOP# = Three-state, PWRDWN# = Driven

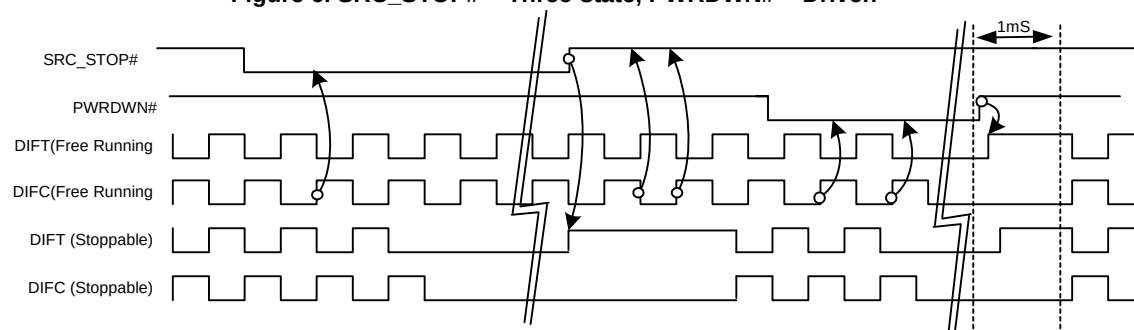


Figure 7. SRC\_STOP# = Three-state, PWRDWN# = Three-state

## Output Enable Clarification

The outputs may be disabled in two ways, via writing a '0' to the SMBus register bit corresponding to output of interest or by asserting an OE input pin LOW. In both methods, if SMBus registered bit has been written LOW or the OE pin is LOW or both, the output of interest will be three-stated. The assertion and deassertion of this signal is asynchronous.

Table 6. OE Functionality

| OE (Pin) | OE (SMBus Bit) | DIFT        | DIFC        |
|----------|----------------|-------------|-------------|
| 1        | 1              | Normal      | Normal      |
| 1        | 0              | Three-state | Three-state |
| 0        | 1              | Three-state | Three-state |
| 0        | 0              | Three-state | Three-state |

## OE Assertion (Transition from '0' to '1')

All differential outputs that were three-stated will resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2–6 DIF clock periods. In addition, DIFT clocks will be driven HIGH within 10 ns of OE assertion to a voltage greater than 200 mV.

## OE Deassertion (Transition from '1' to '0')

The impact of deasserting OE is that each corresponding output will transition from normal operation to three-state in a glitch-free manner. The maximum latency from the deassertion to three-stated outputs is between 2–6 DIF clock periods.

## SRC\_DIV2# Clarification

The SRC\_DIV2# feature is used to configure the DIF output mode to be equal to the SRCT\_IN input frequency or half the input frequency in a glitch-free manner. The SRC\_DIV2# function may be implemented by writing a '0' to SMBus register bit.

## SRC\_DIV2# Assertion

The impact of writing a '0' to the SRC\_DIV2 register bit is that all DIF outputs will transition cleanly in a glitch-free manner from normal operation (output frequency equal to input) to half the input frequency within 2–6 DIF clock periods.

## SRC\_DIV2# Deassertion

The impact of writing a '0' to the SRC\_DIV2 register bit is that all DIF outputs will transition cleanly in a glitch-free manner from divide by 2 mode to normal (output frequency is equal to the input frequency) operation within 2–6 DIF clock periods.

## PLL/BYPASS# Clarification

The PLL/Bypass# input is used to select between bypass mode (no PLL) and PLL mode. In bypass mode, the input clock is passed directly to the output stage resulting in 50 ps additive jitter (50 ps + input jitter) on DIF outputs. In the case of PLL mode, the input clock is pass through a PLL to reduce high-frequency jitter. The BYPASS# mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the PLL/BYPASS# pin LOW. In both methods, if the SMBus register bit has been written low or PLL/BYPASS# pin is LOW or both, the device will be configure for BYPASS operation.

## HIGH\_BW# Clarification

The HIGH\_BW# input is used to set the PLL bandwidth. This mode is intended to minimize PLL peaking when two or more buffers are cascaded by staggering device bandwidths. The PLL low-bandwidth mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the HIGH\_BW# pin is LOW or both, the device will be configured for low-bandwidth operation.



**Absolute Maximum Conditions**

| Parameter          | Description                       | Condition                   | Min. | Max.                  | Unit |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V <sub>DD</sub>    | Core Supply Voltage               |                             | −0.5 | 4.6                   | V    |
| V <sub>DD_A</sub>  | Analog Supply Voltage             |                             | −0.5 | 4.6                   | V    |
| V <sub>IN</sub>    | Input Voltage                     | Relative to V <sub>SS</sub> | −0.5 | V <sub>DD</sub> + 0.5 | VDC  |
| T <sub>S</sub>     | Temperature, Storage              | Non-functional              | −65  | 150                   | °C   |
| T <sub>A</sub>     | Temperature, Operating Ambient    | Functional                  | 0    | 70                    | °C   |
| T <sub>J</sub>     | Temperature, Junction             | Functional                  | −    | 150                   | °C   |
| Θ <sub>JC</sub>    | Dissipation, Junction to Case     | Mil-Spec 883E Method 1012.1 | −    | TBD                   | °C/W |
| Θ <sub>JA</sub>    | Dissipation, Junction to Ambient  | JEDEC (JESD 51)             | −    | TBD                   | °C/W |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015    | 2000 | −                     | V    |
| UL-94              | Flammability Rating               | At 1/8 in.                  | V−0  |                       |      |
| MSL                | Moisture Sensitivity Level        |                             | 1    |                       |      |

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

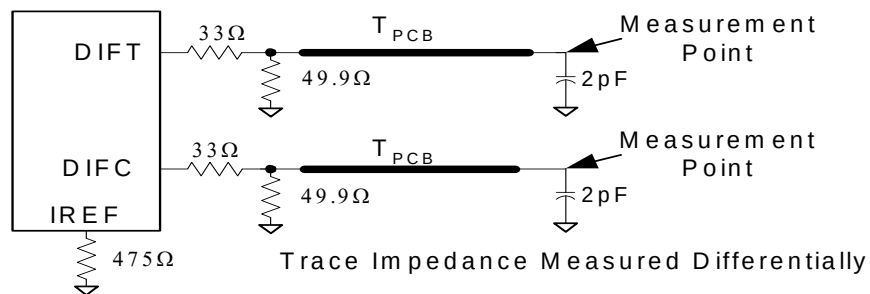
| Parameter                           | Description                   | Condition                                                                  | Min.                  | Max.                  | Unit |
|-------------------------------------|-------------------------------|----------------------------------------------------------------------------|-----------------------|-----------------------|------|
| V <sub>DD_A</sub> , V <sub>DD</sub> | 3.3V Operating Voltage        | 3.3 ± 5%                                                                   | 3.135                 | 3.465                 | V    |
| V <sub>IL12C</sub>                  | Input Low Voltage             | SDATA, SCLK                                                                | −                     | 1.0                   | V    |
| V <sub>IH12C</sub>                  | Input High Voltage            | SDATA, SCLK                                                                | 2.2                   | −                     | V    |
| V <sub>IL</sub>                     | 3.3V Input Low Voltage        |                                                                            | V <sub>SS</sub> − 0.5 | 0.8                   | V    |
| V <sub>IH</sub>                     | 3.3V Input High Voltage       |                                                                            | 2.0                   | V <sub>DD</sub> + 0.5 | V    |
| I <sub>IL</sub>                     | Input Low Leakage Current     | Except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>   | −5                    |                       | μA   |
| I <sub>IH</sub>                     | Input High Leakage Current    | Except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub> |                       | 5                     | μA   |
| I <sub>OZ</sub>                     | High-impedance Output Current |                                                                            | −10                   | 10                    | μA   |
| C <sub>IN</sub>                     | Input Pin Capacitance         |                                                                            | 2                     | 5                     | pF   |
| C <sub>OUT</sub>                    | Output Pin Capacitance        |                                                                            | 3                     | 6                     | pF   |
| L <sub>IN</sub>                     | Pin Inductance                |                                                                            | −                     | 7                     | nH   |
| I <sub>DD3.3V</sub>                 | Dynamic Supply Current        | At max. load and 100 MHz per <i>Figure 8</i>                               | −                     | 215                   | mA   |
| I <sub>PD3.3V</sub>                 | Power-down Supply Current     | PD asserted, Outputs driven                                                | −                     | 40                    | mA   |
| I <sub>PD3.3V</sub>                 | Power-down Supply Current     | PD asserted, Outputs Three-stated                                          | −                     | 5                     | mA   |

**AC Electrical Specification**

| Parameter                       | Description                          | Condition                                                                                           | Min.   | Max.    | Unit |
|---------------------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------|--------|---------|------|
| <b>DIF at 0.7V</b>              |                                      |                                                                                                     |        |         |      |
| T <sub>DC</sub>                 | DIFT and DIFC Duty Cycle             | Measured at crossing point V <sub>OX</sub>                                                          | 45     | 55      | %    |
| T <sub>SKEW</sub>               | Any DIFT/C to DIFT/C Clock Skew, SSC | Measured at crossing point V <sub>OX</sub>                                                          | −      | 150     | ps   |
| T <sub>PERIOD</sub>             | Average Period                       | Measured at crossing point V <sub>OX</sub> at 100 MHz                                               | 9.9970 | 10.0533 | ns   |
| T <sub>CCJ</sub>                | DIFT/C Cycle to Cycle Jitter         | Measured at crossing point V <sub>OX</sub>                                                          | −      | 50      | ps   |
| T <sub>R</sub> / T <sub>F</sub> | DIFT and DIFC Rise and Fall Times    | Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V                                   | 175    | 700     | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                   | Determined as a fraction of 2*(T <sub>R</sub> − T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> ) | −      | 20      | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                  |                                                                                                     | −      | 125     | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                  |                                                                                                     | −      | 125     | ps   |
| V <sub>HIGH</sub>               | Voltage High                         | Measured SE                                                                                         | 660    | 850     | mv   |
| V <sub>LOW</sub>                | Voltage Low                          | Measured SE                                                                                         | −150   | −       | mv   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing |                                                                                                     | 250    | 550     | mv   |

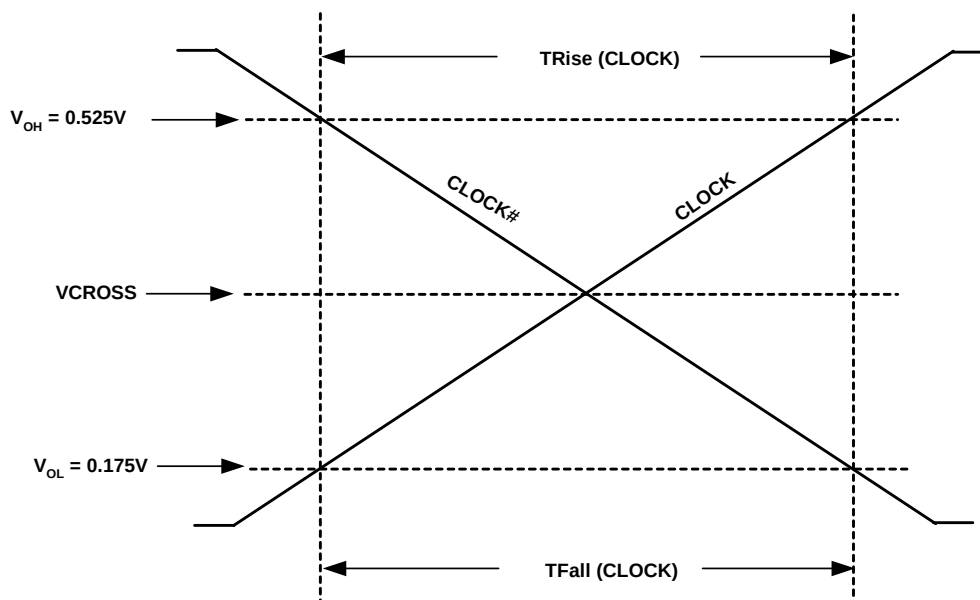
**AC Electrical Specification** (continued)

| Parameter        | Description                            | Condition                           | Min. | Max.             | Unit |
|------------------|----------------------------------------|-------------------------------------|------|------------------|------|
| $\Delta V_{OX}$  | Vcross Variation over all edges        |                                     | –    | 140              | mV   |
| $V_{OVS}$        | Maximum Overshoot Voltage              |                                     | –    | $V_{HIGH} + 0.3$ | V    |
| $V_{UDS}$        | Minimum Undershoot Voltage             |                                     | –    | –0.3             | V    |
| $V_{RB}$         | Ring Back Voltage                      | Measured SE                         | 0.2  | N/A              | V    |
| $t_{PD(PLL)}$    | Input to output skew in PLL mode       | Measured at crossing point $V_{OX}$ | –    | $\pm 250$        | ps   |
| $t_{PD(NONPLL)}$ | Input to output skew in Non - PLL mode | Measured at crossing point $V_{OX}$ | 2.5  | 6.5              | ns   |



**Figure 8. Differential Clock Termination**

**Switching Waveforms**



**Figure 9. Single-Ended Measurement Points for TRise and TFall**

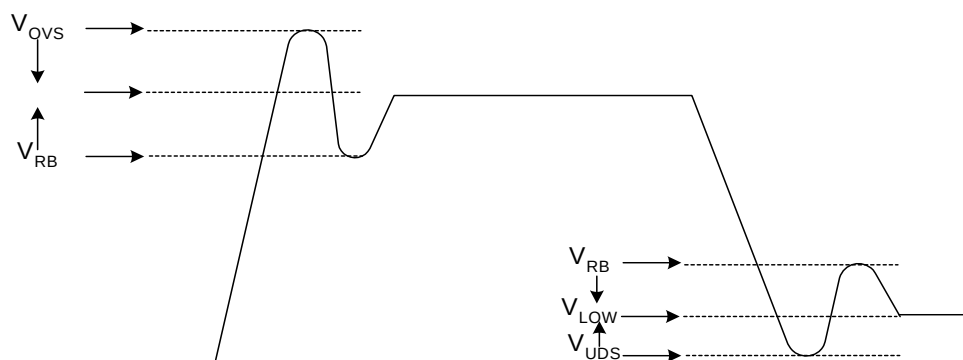


Figure 10. Single-ended Measurement Points for  $V_{OVS}$ ,  $V_{UDS}$  and  $V_{RB}$

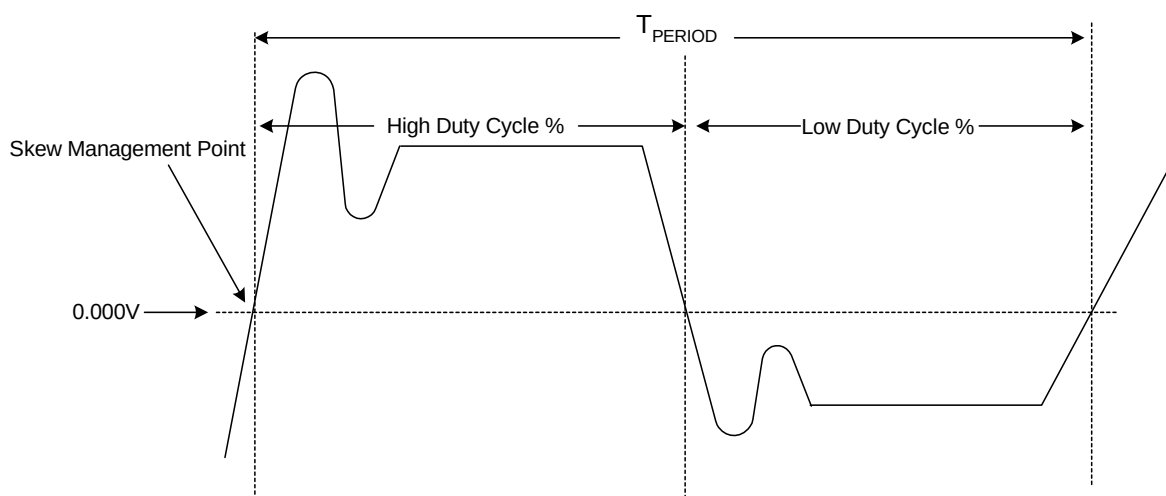


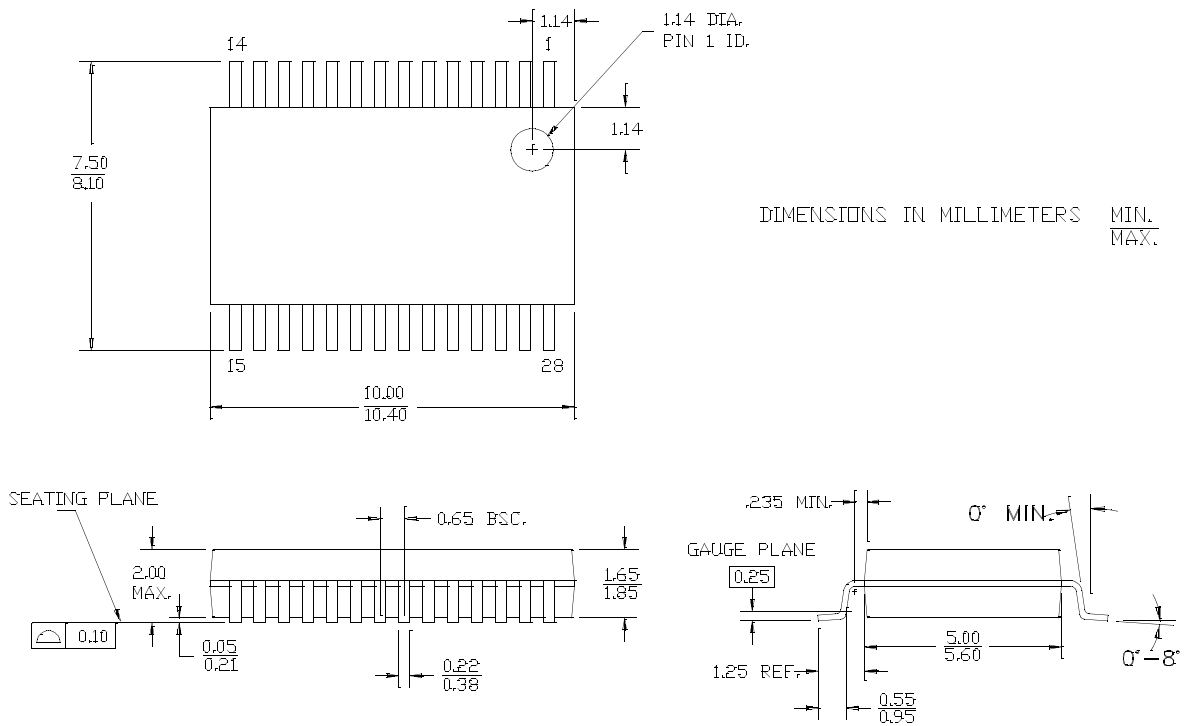
Figure 11. Differential (Clock-CLock#) Measurement Points (Tperiod, Duty Cycle and Jitter)

## Ordering Information

| Ordering Code    | Package Type              | Operating Range          |
|------------------|---------------------------|--------------------------|
| CY28400OC        | 28-pin SSOP               | Commercial, 0°C to 70 °C |
| CY28400OCT       | 28-pin SSOP (Tape & Reel) | Commercial, 0°C to 70 °C |
| <b>Lead-free</b> |                           |                          |
| CY28400OXC       | 28-pin SSOP               | Commercial, 0°C to 70 °C |
| CY28400OXCT      | 28-pin SSOP (Tape & Reel) | Commercial, 0°C to 70 °C |

## Package Drawing and Dimensions

### 28-Lead (5.3 mm) Shrunk Small Outline Package O28



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