

SN54AS825A, SN74AS825A  
8-BIT BUS-INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

- Functionally Equivalent to AMD's AM29825
- Improved  $I_{OH}$  Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

### description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

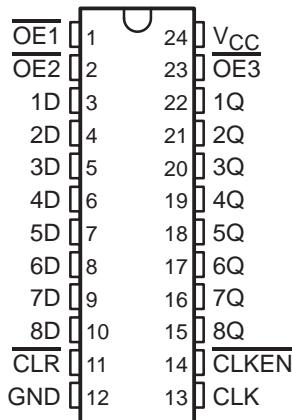
With the clock-enable ( $\overline{CLKEN}$ ) input low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking  $\overline{CLKEN}$  high disables the clock buffer, latching the outputs. These devices have noninverting data (D) inputs. Taking the clear ( $\overline{CLR}$ ) input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-enable ( $\overline{OE1}$ ,  $\overline{OE2}$ , and  $\overline{OE3}$ ) inputs can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

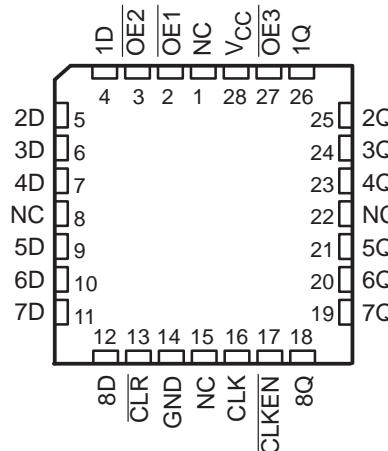
The output enables do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS825A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS825A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54AS825A . . . JT PACKAGE  
SN74AS825A . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS825A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

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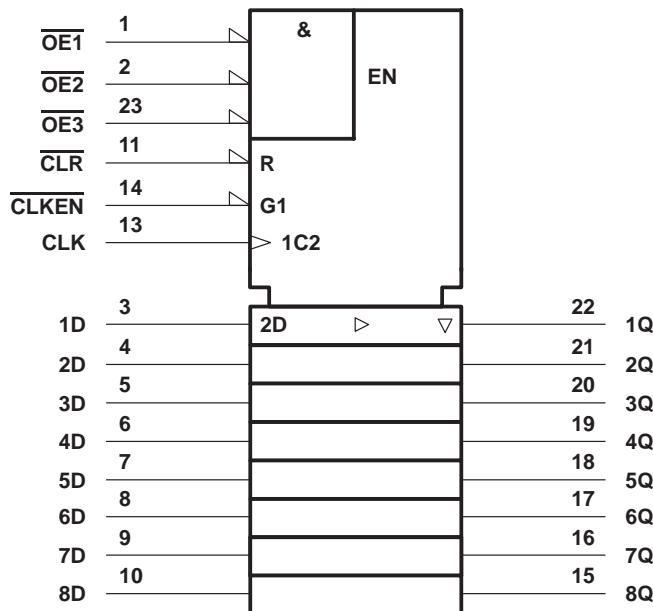
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**FUNCTION TABLE  
(each flip-flop)**

INPUTS					OUTPUT Q
<u>OE<sub>1</sub></u>	<u>CLR</u>	<u>CLKEN</u>	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q <sub>0</sub>
H	X	X	X	X	Z

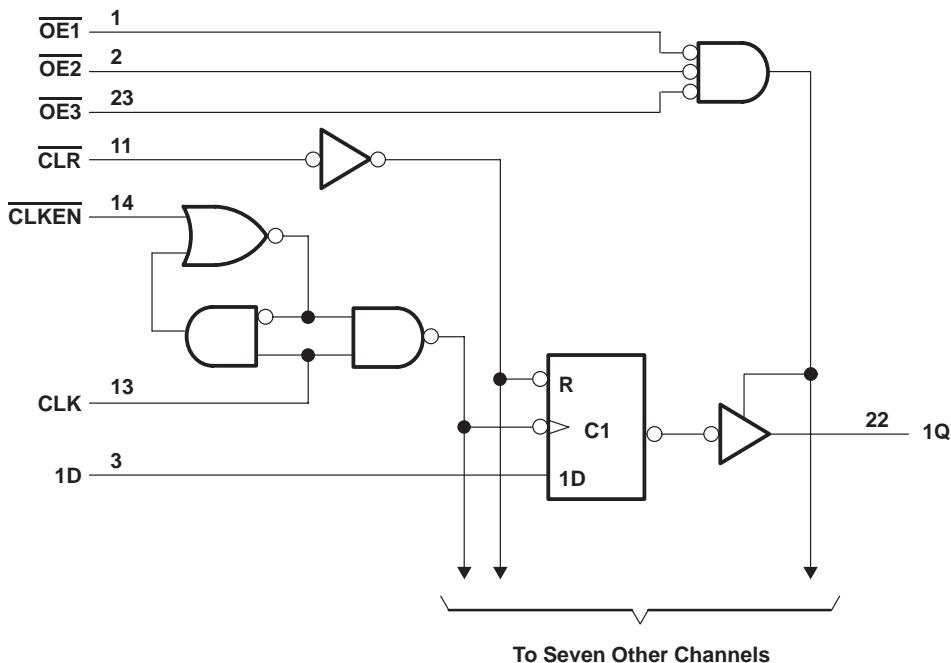
† OE = H if any of OE<sub>1</sub>, OE<sub>2</sub>, or OE<sub>3</sub> are high.  
OE = L if all of OE<sub>1</sub>, OE<sub>2</sub>, or OE<sub>3</sub> are low.

**logic symbol‡**



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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**recommended operating conditions**

			SN54AS825A			SN74AS825A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
I <sub>OH</sub>	High-level output current				-24			-24	mA
I <sub>OL</sub>	Low-level output current				32			48	mA
t <sub>w</sub> *	Pulse duration	CLR low		7		4			ns
		CLK high or low		9.5		8			
t <sub>su</sub> *	Setup time before CLK↑	CLR inactive		8		8			ns
		Data		7		6			
		CLKEN high or low		10		6			
t <sub>h</sub> *	Hold time after CLK↑	CLKEN low or data		0		0			ns
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54AS825A			SN74AS825A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> - 2			V <sub>CC</sub> - 2			V
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -15 mA	2.4	3.2	2.4	3.2		
		I <sub>OH</sub> = -24 mA	2		2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 32 mA	0.3	0.5				V
		I <sub>OL</sub> = 48 mA			0.35	0.5		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		50		50			µA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-50		-50			µA
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.1		0.1			mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20		20			µA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-0.5		-0.5			mA
I <sub>O‡</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30	-112	-30	-112			mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	Outputs high	45	73	45	73		mA
		Outputs low	56	90	56	90		
		Outputs disabled	59	95	59	95		

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

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**switching characteristics (see Figure 1)**

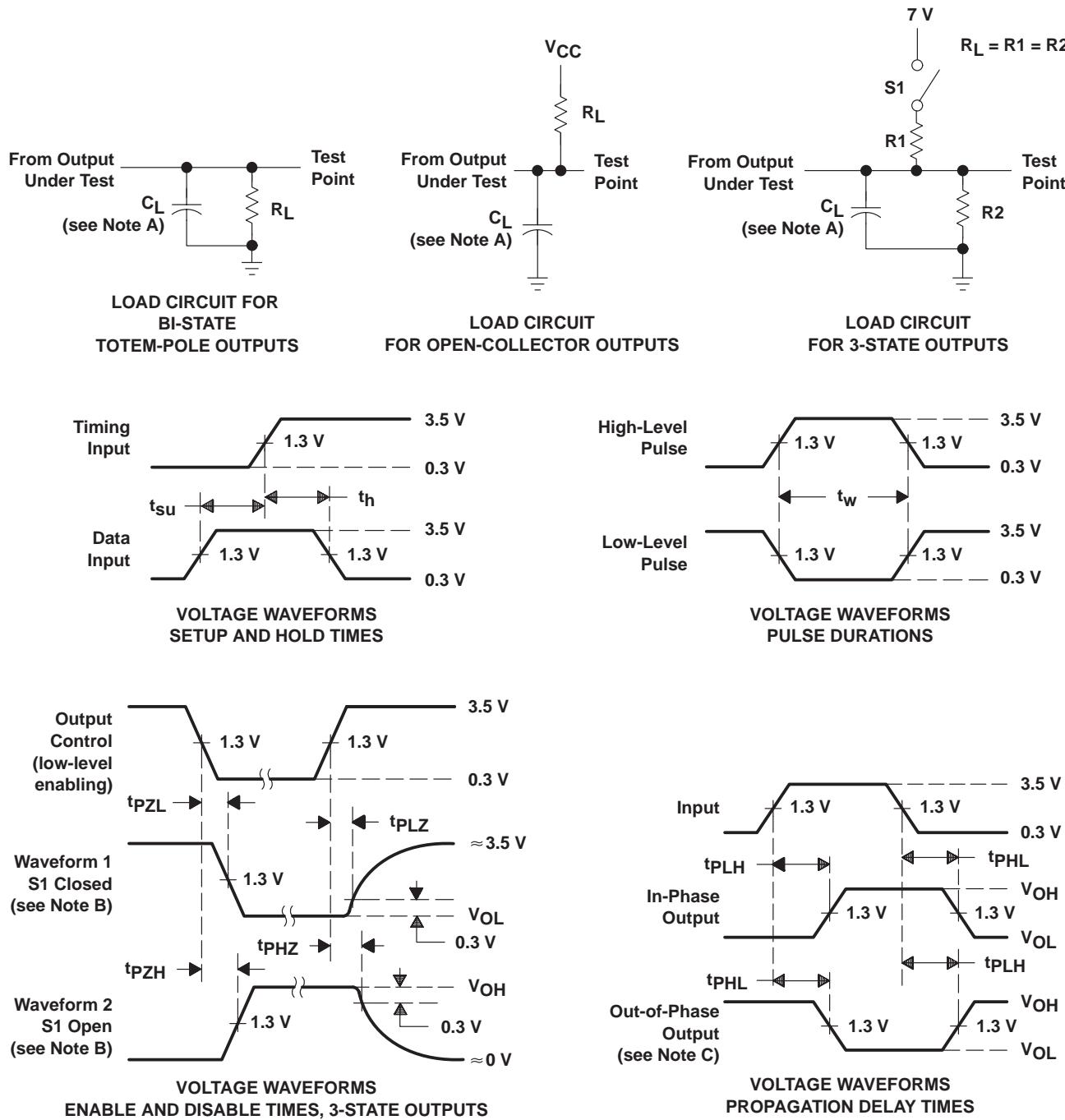
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R1 = 500\text{ }\Omega,$ $R2 = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS825A		SN74AS825A			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	CLK	Any Q	3.5	9	3.5	7.5	ns	
$t_{PHL}$			3.5	13.5	3.5	13		
$t_{PHL}$	$\overline{\text{CLR}}$	Any Q	3.5	16.5	3.5	15.5	ns	
$t_{PZH}$	$\overline{\text{OE}}$	Any Q	4	12	4	11	ns	
$t_{PZL}$			4	13	4	12		
$t_{PHZ}$	$\overline{\text{OE}}$	Any Q	1	10	1.5	8	ns	
$t_{PLZ}$			1	10	1.5	8		

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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