R8A66162SP

32-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

REJ03F0263-0100
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DESCRIPTION

The R8A66162SP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel - output shift register, equipped with direct set input and output latches.
The R8A66162SP guarantees sufficient 24mA (Vcc=5.0V case) output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output. The parallel outputs are open-drain outputs.
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products. Furthermore, pin layout ensures the realization of an easy printed circuit. R8A66162SP is the succession product of M66313FP.

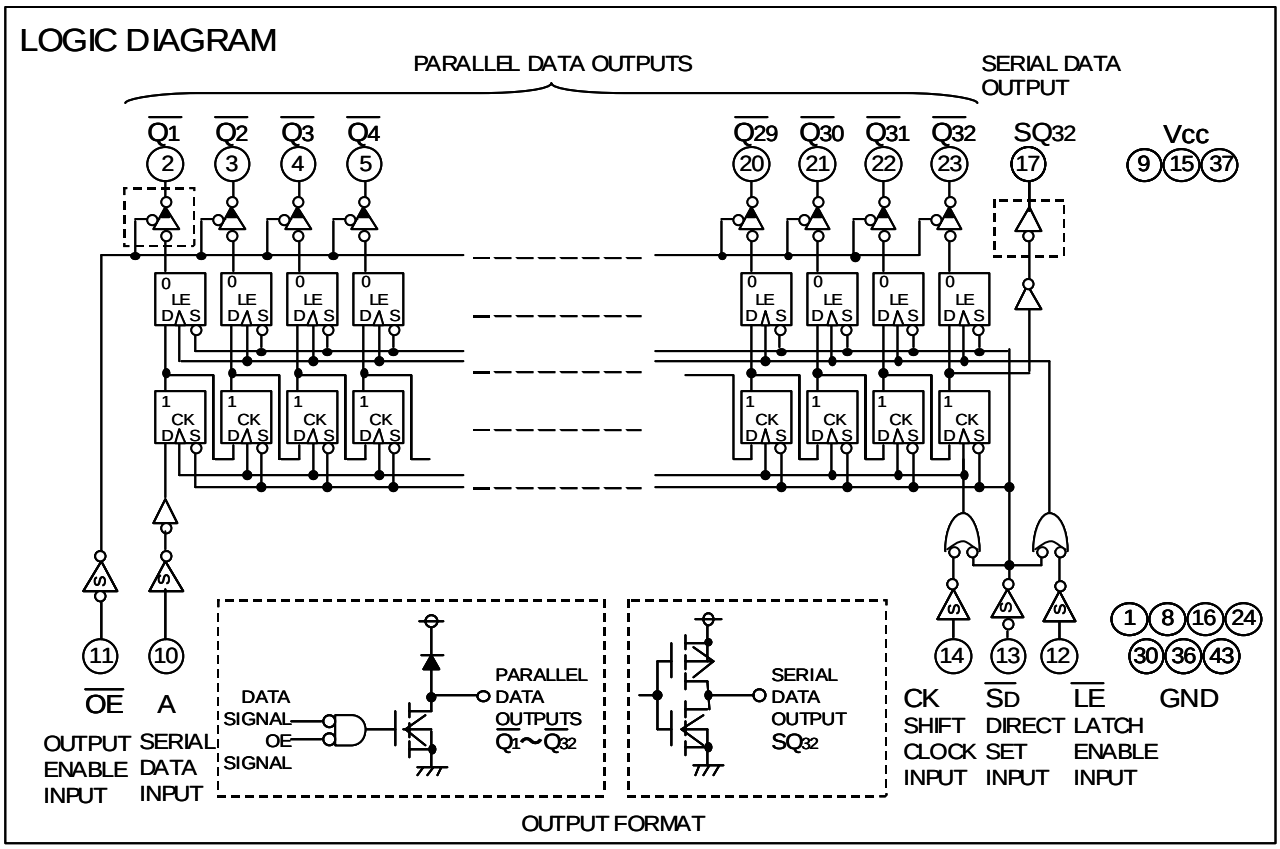
FEATURES

- Anode common LED drive
- Vcc 5V or 3.3V single power supply
- High output current: All parallel outputs $\overline{Q_1}$~$\overline{Q_{32}}$ I_{OL}=24mA (at V_{CC}=5.0V), I_{OL}=12mA (at V_{CC}=3.3V), LEDs can be turned on simultaneously.
- Low power dissipation: 200uW/package (max) (V_{CC}=5.0V, Ta=25°C, quiescent state)
- High noise margin: Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input ($\overline{SD}$)
- Open-drain output ($\overline{Q_1}$~$\overline{Q_{32}}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range (Ta=-40°C~+85°C)
- Pin configuration for easy layout on PCB. (Pin configuration allows easy cascade connection or LED connection)

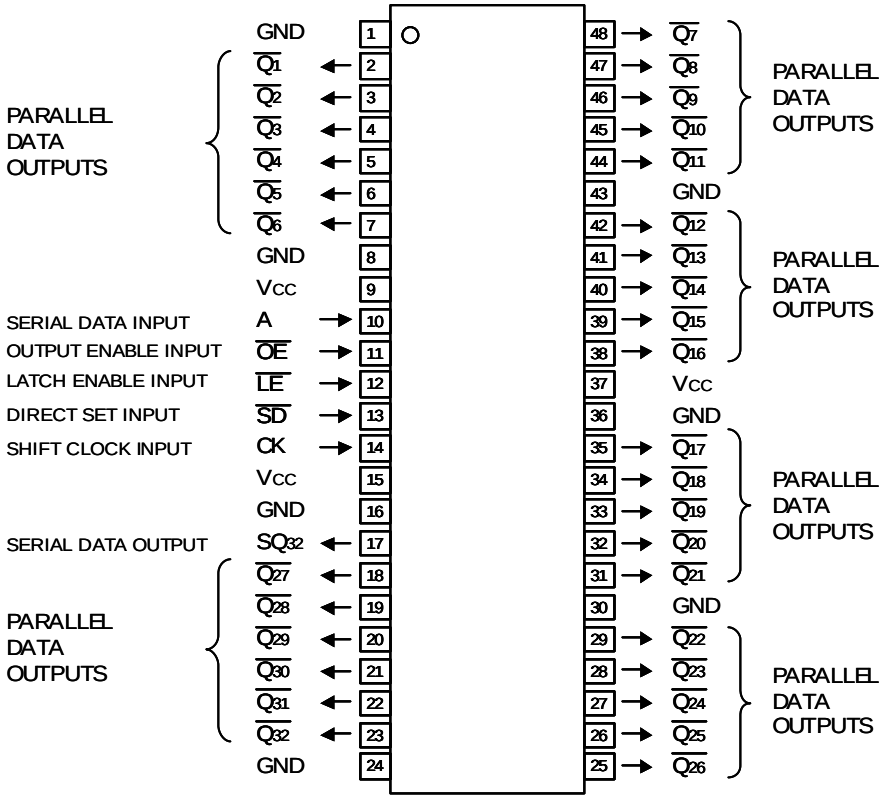
APPLICATION

- LED array drive, The various LED display modules
- PPC, Printer, VCR, Mini-compo, Button-Telephone etc. All of LED display equipments

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



FUNCTIONAL DESCRIPTION

The employment of silicon gate CMOS process of the R8A66162SP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.
Each shift register bit consists of a flip-flop for shifting and an output latch.
The shift operation takes place when the shift clock input CK changes from low-level to high-level.
The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.
If the latch-enable input $\overline{LE}$ is turned high-level, the content of the shift register at that instant is latched.
The parallel data outputs $\overline{Q_1}$~$\overline{Q_{32}}$ are open-drain outputs.
To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the 32nd bit.
If the direct set input $\overline{SD}$ is turned low-level, $\overline{Q_1}$~$\overline{Q_{32}}$ and SQ_{32} are set. Then shift register and latches are set.
If the high-level input is applied to the output enable input $\overline{OE}$, $\overline{Q_1}$~$\overline{Q_{32}}$ are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift operation is not affected when $\overline{OE}$ is changed.

FUNCTION TABLE (Note: 1)

OPERATION MODE	INPUT					PARALLEL OUTPUTS																																		SERIAL OUTPUT
	$\overline{SD}$	CK	$\overline{LE}$	A	$\overline{OE}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	$\overline{Q_5}$	$\overline{Q_6}$	$\overline{Q_7}$	$\overline{Q_8}$	$\overline{Q_9}$	$\overline{Q_{10}}$	$\overline{Q_{11}}$	$\overline{Q_{12}}$	$\overline{Q_{13}}$	$\overline{Q_{14}}$	$\overline{Q_{15}}$	$\overline{Q_{16}}$	$\overline{Q_{17}}$	$\overline{Q_{18}}$	$\overline{Q_{19}}$	$\overline{Q_{20}}$	$\overline{Q_{21}}$	$\overline{Q_{22}}$	$\overline{Q_{23}}$	$\overline{Q_{24}}$	$\overline{Q_{25}}$	$\overline{Q_{26}}$	$\overline{Q_{27}}$	$\overline{Q_{28}}$	$\overline{Q_{29}}$	$\overline{Q_{30}}$	$\overline{Q_{31}}$	$\overline{Q_{32}}$	SQ_{32}
SET	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
SHIFT	H	↑	L	H	L	L	$\overline{Q^0_1}$	$\overline{Q^0_2}$	$\overline{Q^0_3}$	$\overline{Q^0_4}$	$\overline{Q^0_5}$	$\overline{Q^0_6}$	$\overline{Q^0_7}$	$\overline{Q^0_8}$	$\overline{Q^0_9}$	$\overline{Q^0_{10}}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	q^0_{31}
	H	↑	L	L	L	Z	$\overline{Q^0_1}$	$\overline{Q^0_2}$	$\overline{Q^0_3}$	$\overline{Q^0_4}$	$\overline{Q^0_5}$	$\overline{Q^0_6}$	$\overline{Q^0_7}$	$\overline{Q^0_8}$	$\overline{Q^0_9}$	$\overline{Q^0_{10}}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	q^0_{31}
LATCH	H	X	H	X	L	$\overline{Q^0_1}$	$\overline{Q^0_2}$	$\overline{Q^0_3}$	$\overline{Q^0_4}$	$\overline{Q^0_5}$	$\overline{Q^0_6}$	$\overline{Q^0_7}$	$\overline{Q^0_8}$	$\overline{Q^0_9}$	$\overline{Q^0_{10}}$	$\overline{Q^0_{11}}$	$\overline{Q^0_{12}}$	$\overline{Q^0_{13}}$	$\overline{Q^0_{14}}$	$\overline{Q^0_{15}}$	$\overline{Q^0_{16}}$	$\overline{Q^0_{17}}$	$\overline{Q^0_{18}}$	$\overline{Q^0_{19}}$	$\overline{Q^0_{20}}$	$\overline{Q^0_{21}}$	$\overline{Q^0_{22}}$	$\overline{Q^0_{23}}$	$\overline{Q^0_{24}}$	$\overline{Q^0_{25}}$	$\overline{Q^0_{26}}$	$\overline{Q^0_{27}}$	$\overline{Q^0_{28}}$	$\overline{Q^0_{29}}$	$\overline{Q^0_{30}}$	$\overline{Q^0_{31}}$	$\overline{Q^0_{32}}$	q_{32}
OUTPUT DIS-ABLE	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_{32}

Note 1. ↑ : Transition from low-to-high-level
$\overline{Q}^0$: Shows the status of output $\overline{Q}$ before CK input changes
X : Irrelevant
q^0 : The content of shift register before CK changes
q : The content of shift register
Z : High-impedance state

ABSOLUTE MAXIMUM RATINGS (Ta=-40~85°C, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
Vcc	Supply voltage			-0.5~+7.0	V
V_I	Input voltage			-0.5~Vcc+0.5	V
V_O	Output voltage			-0.5~Vcc+0.5	V
I_O	Output current per output pin	$\overline{Q_1}$~$\overline{Q_{32}}$		50	mA
		SQ_{32}		±25	
Icc	Supply/GND current		Vcc, GND	-920, +20	mA
P_d	Power dissipation			650	mW
T_{stg}	Storage temperature range			-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-40~85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage	5.0V support	4.5	5.0	5.5	V
		3.3V support	3.0	3.3	3.6	V
V_I	Input voltage		0		Vcc	V
V_O	Output voltage		0		Vcc	V
T_{opr}	Operating temperature range		-40		85	°C

ELECTRICAL CHARACTERISTICS

■5.0V version support specifications (Ta=-40~85°C, Vcc=4.5V~5.5V, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{T+}	Positive going threshold voltage				0.35xVcc		0.70xVcc	V
V_{T-}	Negative going threshold voltage				0.20xVcc		0.55xVcc	V
V_{OH}	High level output voltage	SQ_{32}	$V_I=V_{T+}$, V_{T-} Vcc=4.5V	I_{OH}=-20uA	Vcc-0.1			V
				I_{OH}=-4mA	3.66			
V_{OL}	Low level output voltage	$\overline{Q_1}$~$\overline{Q_{32}}$	$V_I=V_{T+}$, V_{T-} Vcc=4.5V	I_{OL}=20uA			0.10	V
				I_{OL}=24mA			0.50	
				I_{OL}=28mA			0.55(Note2)	
		SQ_{32}		I_{OL}=20uA			0.10	
				I_{OL}=4mA			0.53	
I_{IH}	High level input current		V_I=Vcc	Vcc=5.5V			5	uA
I_{IL}	Low level input current		V_I=GND	Vcc=5.5V			-5	uA
I_O	Maximum output leakage current	$\overline{Q_1}$~$\overline{Q_{32}}$	$V_I=V_{T+}$, V_{T-} Vcc=5.5V	V_O=Vcc			10	uA
				V_O=GND			-10	
Icc	Quiescent supply current		V_I=Vcc, GND	Vcc=5.5V			400	uA

Note2 : Ta = -40~70°C

■3.3V version support specifications (Ta=-40~85°C, Vcc=3.0V~3.6V, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{T+}	Positive going threshold voltage				0.35xVcc		0.70xVcc	V
V_{T-}	Negative going threshold voltage				0.20xVcc		0.55xVcc	V
V_{OH}	High level output voltage	SQ_{32}	$V_I=V_{T+}$, V_{T-} Vcc=3.0V	I_{OH}=-20uA	Vcc-0.1			V
				I_{OH}=-2mA	2.60			
V_{OL}	Low level output voltage	$\overline{Q_1}$~$\overline{Q_{32}}$	$V_I=V_{T+}$, V_{T-} Vcc=3.0V	I_{OL}=20uA			0.10	V
				I_{OL}=12mA			0.54	
		SQ_{32}		I_{OL}=20uA			0.10	
				I_{OL}=2mA			0.40	
I_{IH}	High level input current		V_I=Vcc	Vcc=3.6V			5	uA
I_{IL}	Low level input current		V_I=GND	Vcc=3.6V			-5	uA
I_O	Maximum output leakage current	$\overline{Q_1}$~$\overline{Q_{32}}$	$V_I=V_{T+}$, V_{T-} Vcc=3.6V	V_O=Vcc			10	uA
				V_O=GND			-10	
Icc	Quiescent supply current		V_I=Vcc, GND	Vcc=3.6V			400	uA

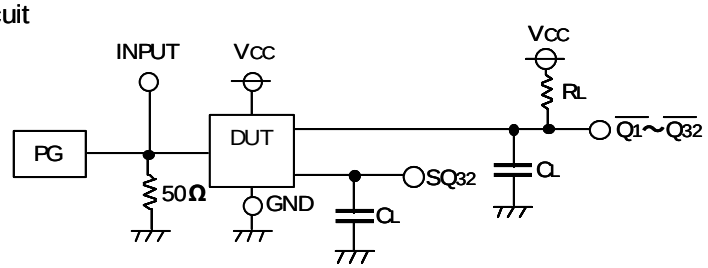
SWITCHING CHARACTERISTICS (Ta=-40~85°C, Vcc=5.0V or 3.3V, unless otherwise noted)

Symbol	Parameter		Test conditions	5.0V specification			3.3V specification			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{max}	Maximum clock frequency					4			3.3	MHz
tPZL	Output "Z-L" and "L-Z" propagation time	CK-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)				200			220	ns
tPLZ		CK-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)				250			270	ns
tPLH	Output "L-H" and "H-L" propagation time	CK-SQ_{32}				125			150	ns
tPHL						125			150	ns
tPZL	Output "Z-L" propagation time	$\overline{S_D}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)	C_L=50pF			200			220	ns
tPLH	Output "L-H" propagation time	$\overline{S_D}$-SQ_{32}	R_L=1kΩ			125			150	ns
tPZL	Output "Z-L" and "L-Z" propagation time	$\overline{LE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)	(Note3)			125			150	ns
tPLZ		$\overline{LE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)				200			220	ns
tPZL	Output "Z-L" and "L-Z" propagation time	$\overline{OE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned on)				125			150	ns
tPLZ		$\overline{OE}$-$\overline{Q_1}$~$\overline{Q_{32}}$ (Turned off)				200			220	ns
C_I	Input capacitance					10			10	pF
C_O	Output capacitance		$\overline{OE}$=Vcc			15			15	pF

TIMING REQUIREMENTS (Ta=-40~85°C, Vcc=5.0V or 3.3V, unless otherwise noted)

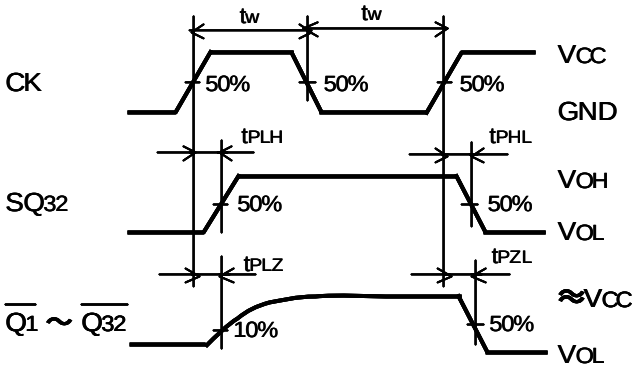
Symbol	Parameter	Test conditions	5.0V specification			3.3V specification			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_w	CK, $\overline{LE}$, $\overline{S_D}$ pulse width	(Note3)	125			150			ns
t_{su}	Setup time A to CK		125			150			ns
t_h	Hold time A to CK		15			20			ns
	Hold time $\overline{LE}$ to CK		70			80			ns
t_{rec}	Recovery time CK to $\overline{S_D}$		70			80			ns

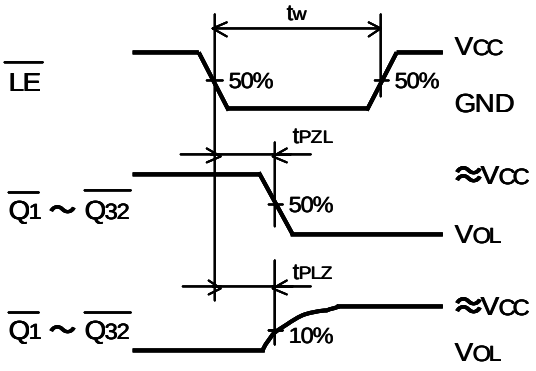
Note3. Test circuit

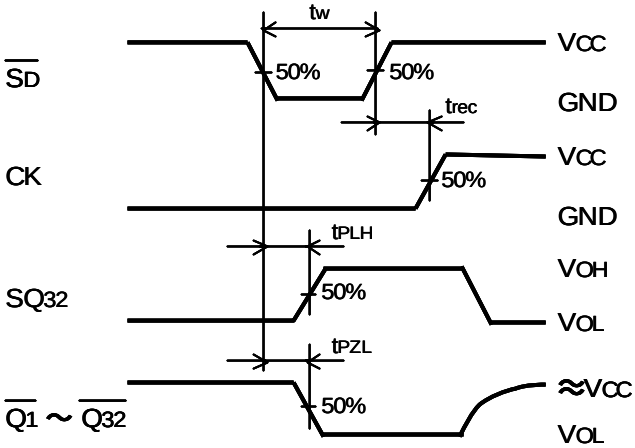


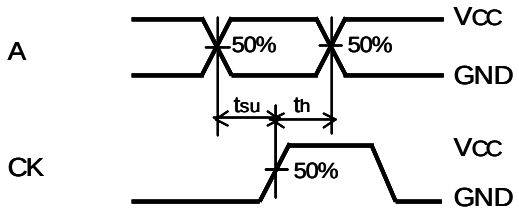
(1) The pulse generator(PG) has the following characteristics(10%~90%):tr=6ns,tf=6ns
(2) The capacitance CL includes stray wiring capacitance and the probe input capacitance.

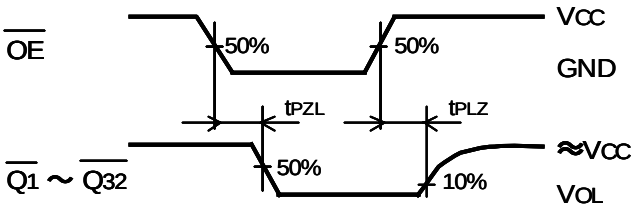
TIMING DIAGRAM

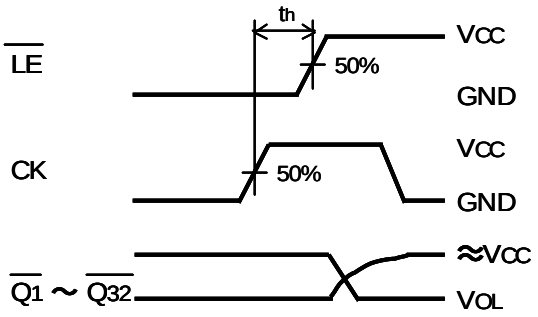






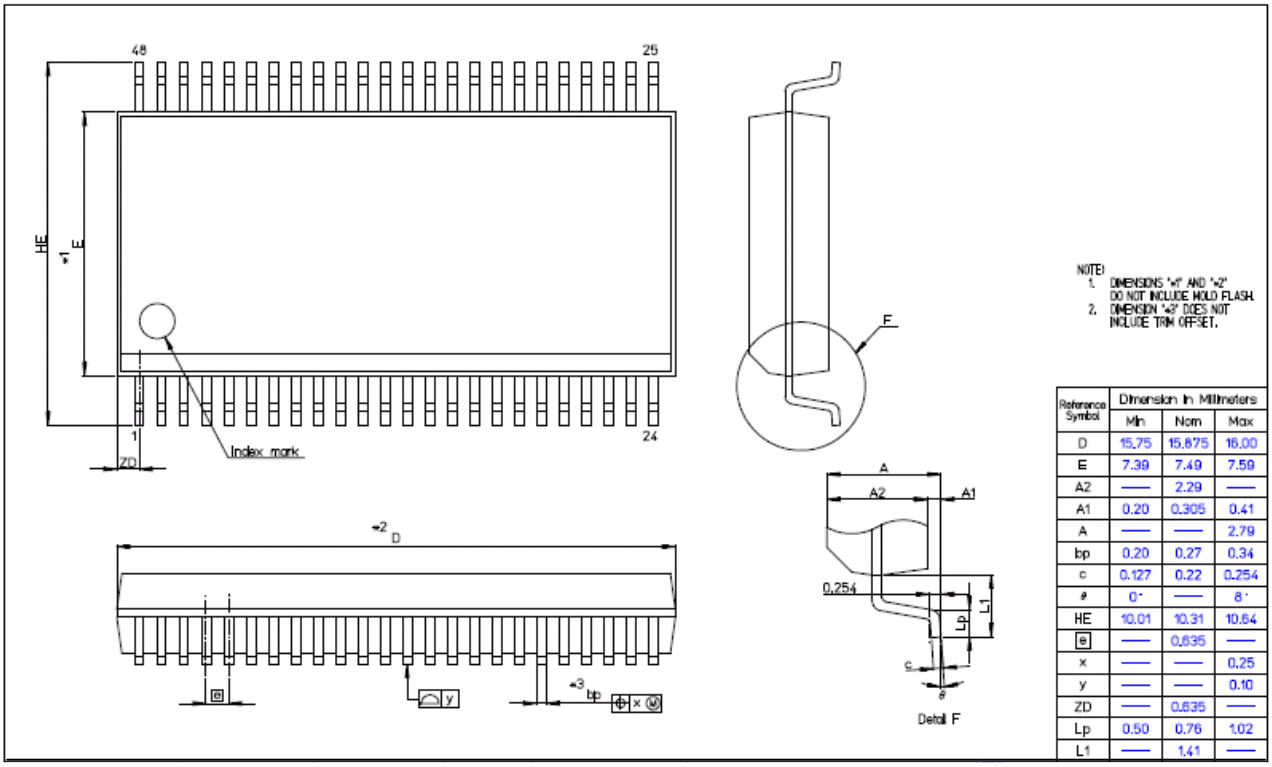






PACKAGE OUTLINE

Package	RENESAS Code	Previous Code
48pin SSOP	PRSP0048ZB-A	48P2X-A



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.75	15.875	16.00
E	7.39	7.49	7.59
A2	—	2.29	—
A1	0.20	0.305	0.41
A	—	—	2.79
bp	0.20	0.27	0.34
c	0.127	0.22	0.254
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	0.635	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.635	—
Lp	0.50	0.76	1.02
L1	—	1.41	—

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