Nonvolatile Memory, Dual 256-Position Digital Potentiometer

Data Sheet

AD5232

FEATURES

Dual-channel, 256-position resolution
10 kΩ, 50 kΩ, and 100 kΩ nominal terminal resistance
Nonvolatile memory maintenance of wiper settings
Predefined linear increment/decrement instructions
Predefined ±6 dB step log taper increment/decrement instructions
SPI-compatible serial interface
Wiper settings and EEMEM readback
3 V to 5 V single-supply operation
±2.5 V dual-supply operation
14 bytes of general-purpose user EEMEM
Permanent memory write protection
100-year typical data retention (T_A = 55°C)

APPLICATIONS

Mechanical potentiometer replacement
Instrumentation: gain and offset adjustment
Programmable voltage-to-current conversion
Programmable filters, delays, and time constants
Programmable power supply
Low resolution DAC replacement
Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD5232 device provides a nonvolatile, dual-channel, digitally controlled variable resistor (VR) with 256-position resolution. This device performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. The versatile programming of the AD5232, performed via a microcontroller, allows multiple modes of operation and adjustment.

In the direct program mode, a predetermined setting of the RDAC registers (RDAC1 and RDAC2) can be loaded directly from the microcontroller. Another important mode of operation allows the RDACx register to be refreshed with the setting previously stored in the corresponding EEMEM register (EEMEM1 and EEMEM2). When changes are made to the RDACx register to establish a new wiper position, the value of the setting can be saved into the EEMEMx register by executing an EEMEM save operation. After the settings are saved in the EEMEMx register, these values are automatically transferred to the RDACx register to set the wiper position at system power-on. Such operation is enabled by the internal preset strobe. The preset strobe can also be accessed externally.
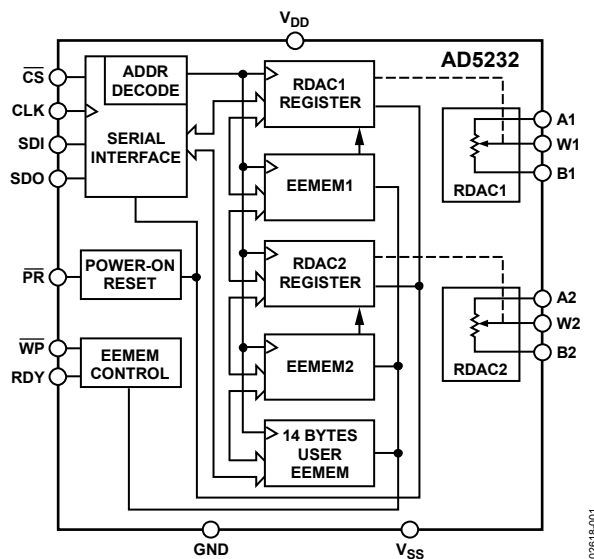
All internal register contents can be read via the serial data output (SDO). This includes the RDAC1 and RDAC2 registers, the corresponding nonvolatile EEMEM1 and EEMEM2 registers, and the 14 spare USER EEMEM registers that are available for constant storage.

The basic mode of adjustment is the increment and decrement command instructions that control the wiper position setting register (RDACx). An internal scratch pad RDACx register can be moved up or down one step of the nominal resistance between Terminal A and Terminal B. This step adjustment linearly changes the wiper to Terminal B resistance (R_{WB}) by one position segment of the device's end-to-end resistance (R_{AB}). For exponential/logarithmic changes in wiper setting, a left/right shift command instruction adjusts the levels in ±6 dB steps, which can be useful for audio and light alarm applications.

The AD5232 is available in a thin, 16-lead TSSOP package. All parts are guaranteed to operate over the extended industrial temperature range of −40°C to +85°C. An evaluation board, the EVAL-AD5232-10EBZ, is available.

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 3 V ± 10% or 5 V ± 10% and V_{SS} = 0 V, V_A = +V_{DD}, V_B = 0 V, −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE		Specifications apply to all VRs				
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC	−1	±1/2	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	−0.4		+0.4	% FS
Nominal Resistor Tolerance	ΔR_{AB}		−40		+20	%
Resistance Temperature Coefficient	ΔR_{AB}/ΔT			600		ppm/°C
Wiper Resistance	R_W	I_W = 100 µA, V_{DD} = 5.5 V, code = 0x1E		50	100	Ω
		I_W = 100 µA, V_{DD} = 3 V, code = 0x1E		200		Ω
POTENTIOMETER DIVIDER MODES						
Resolution	N		8			Bits
Differential Nonlinearity[3]	DNL		−1	±1/2	+1	LSB
Integral Nonlinearity[3]	INL		−0.4		+0.4	% FS
Voltage Divider Temperature Coefficient	ΔV_W/ΔT	Code = half scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−3		0	% FS
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		3	% FS
RESISTOR TERMINALS						
Terminal Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance Ax, Bx[5]	C_A, C_B	f = 1 MHz, measured to GND, code = half-scale		45		pF
Capacitance Wx[5]	C_W	f = 1 MHz, measured to GND, code = half scale		60		pF
Common-Mode Leakage Current[5, 6]	I_{CM}	V_W = V_{DD}/2		0.01	1	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V	2.0			V
Input Logic Low	V_{IL}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = −2.5 V		0.5		V
Output Logic High (SDO and RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±2.5	µA
Input Capacitance[5]	C_{IL}			4		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND		3.5	10	µA
Programming Mode Current	$I_{DD(PG)}$	V_{IH} = V_{DD} or V_{IL} = GND		35		mA
Read Mode Current[7]	$I_{DD(XFR)}$	V_{IH} = V_{DD} or V_{IL} = GND	0.9	3	9	mA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND,				
		V_{DD} = +2.5 V, V_{SS} = −2.5 V		3.5	10	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND		0.018	0.05	mW
Power Supply Sensitivity[5]	PSS	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 9]						
Bandwidth		−3 dB, BW_10kΩ, R = 10 kΩ		500		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.022		%
		V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 50 kΩ, 100 kΩ		0.045		%
V_W Settling Time	t_S	V_{DD} = 5 V, V_{SS} = 0 V, V_A = V_{DD}, V_B = 0 V, V_W = 0.50% error band, Code 0x00 to Code 0x80 for R_{AB} = 10 kΩ/50 kΩ/100 kΩ		0.65/3/6		μs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f= 1 kHz		9		nV/√Hz
Crosstalk (C_{W1}/C_{W2})	C_T	V_A = V_{DD}, V_B = 0 V, measure V_W with adjacent VR making full-scale code change		−5		nV-sec
Analog Crosstalk (C_{W1}/C_{W2})	C_{TA}	V_{A1} = V_{DD}, V_{B1} = 0 V, measure V_{W1} with V_{W2} = 5 V p-p @ f = 10 kHz; $Code_1$ = 0x80; $Code_2$ = 0xFF		−70		dB
FLASH/EE MEMORY RELIABILITY						
Endurance[10]			100			kCycles
Data Retention[11]				100		Years

[1] Typical parameters represent average readings at 25°C and V_{DD} = 5 V.

[2] Resistor position nonlinearity (R-INL) error is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. I_W ~ 50 μA @ V_{DD} = 2.7 V and I_W ~ 400 μA @ V_{DD} = 5 V for the R_{AB} = 10 kΩ version, I_W ~ 50 μA for the R_{AB} = 50 kΩ version, and I_W ~ 25 μA for the R_{AB} = 100 kΩ version (see Figure 22).

[3] INL and DNL are measured at V_W with the RDACx configured as a potentiometer divider similar to a voltage output digital-to-analog converter. V_A = V_{DD} and V_B = V_{SS}. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions (see Figure 23).

[4] The A, B, and W resistor terminals have no limitations on polarity with respect to each other. Dual supply operation enables ground-referenced bipolar signal adjustment.

[5] Guaranteed by design; not subject to production test.

[6] Common-mode leakage current is a measure of the dc leakage from any A, B, or W terminal to a common-mode bias level of V_{DD}/2.

[7] Transfer (XFR) mode current is not continuous. Current is consumed while the EEMEMx locations are read and transferred to the RDACx register (see Figure 13).

[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).

[9] All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = −2.5 V, unless otherwise noted.

[10] Endurance is qualified to 100,000 cycles per JEDEC Std. 22, Method A117 and measured at −40°C, +25°C, and +85°C. Typical endurance at +25°C is 700,000 cycles.

[11] The retention lifetime equivalent at junction temperature (T_J) = 55°C, as per JEDEC Std. 22, Method A117. Retention lifetime, based on an activation energy of 0.6 eV, derates with junction temperature as shown in Figure 44 in the Flash/EEMEM Reliability section. The AD5232 contains 9,646 transistors. Die size = 69 mil × 115 mil, 7,993 sq. mil.

INTERFACE TIMING CHARACTERISTICS

All input control voltages are specified with $t_R = t_F = 2.5$ ns (10% to 90% of 3 V) and are timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD} = 3$ V and $V_{DD} = 5$ V.

Table 2.

Parameter[1,2]	Symbol	Conditions	Min	Typ[3]	Max	Unit
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulse Width	t_4, t_5	Clock level high or low	10			ns
Data Setup Time	t_6	From positive CLK transition	5			ns
Data Hold Time	t_7	From positive CLK transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[4]	t_{10}	$R_P = 2.2$ kΩ, $C_L < 20$ pF			50	ns
CLK to SDO Data Hold Time	t_{11}	$R_P = 2.2$ kΩ, $C_L < 20$ pF	0			ns
$\overline{CS}$ High Pulse Width[5]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[5]	t_{13}		4			t_{CYC}
RDY Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to RDY Fall Time	t_{15}			0.15	0.3	ms
Store/Read EEMEM Time[6]	t_{16}	Applies to Command Instruction 2, Command Instruction 3, and Command Instruction 9			25	ms
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulse Width (Asynchronous)	t_{PRW}	Not shown in timing diagram	50			ns
Preset Response Time to RDY High	t_{PRESP}	$\overline{PR}$ pulsed low to refresh wiper positions		70		μs

[1] Guaranteed by design; not subject to production test.
[2] See the Timing Diagrams section for the location of measured values.
[3] Typicals represent average readings at 25°C and $V_{DD} = 5$ V.
[4] Propagation delay depends on the value of V_{DD}, $R_{PULL-UP}$, and C_L.
[5] Valid for commands that do not activate the RDY pin.
[6] RDY pin low only for Command Instruction 2, Command Instruction 3, Command Instruction 8, Command Instruction 9, Command Instruction 10, and the $\overline{PR}$ hardware pulse: CMD_8 ~ 1 ms, CMD_9 = CMD_10 ~ 0.12 ms, and CMD_2 = CMD_3 ~ 20 ms. Device operation at $T_A = -40$°C and $V_{DD} < 3$ V extends the save time to 35 ms.

Timing Diagrams
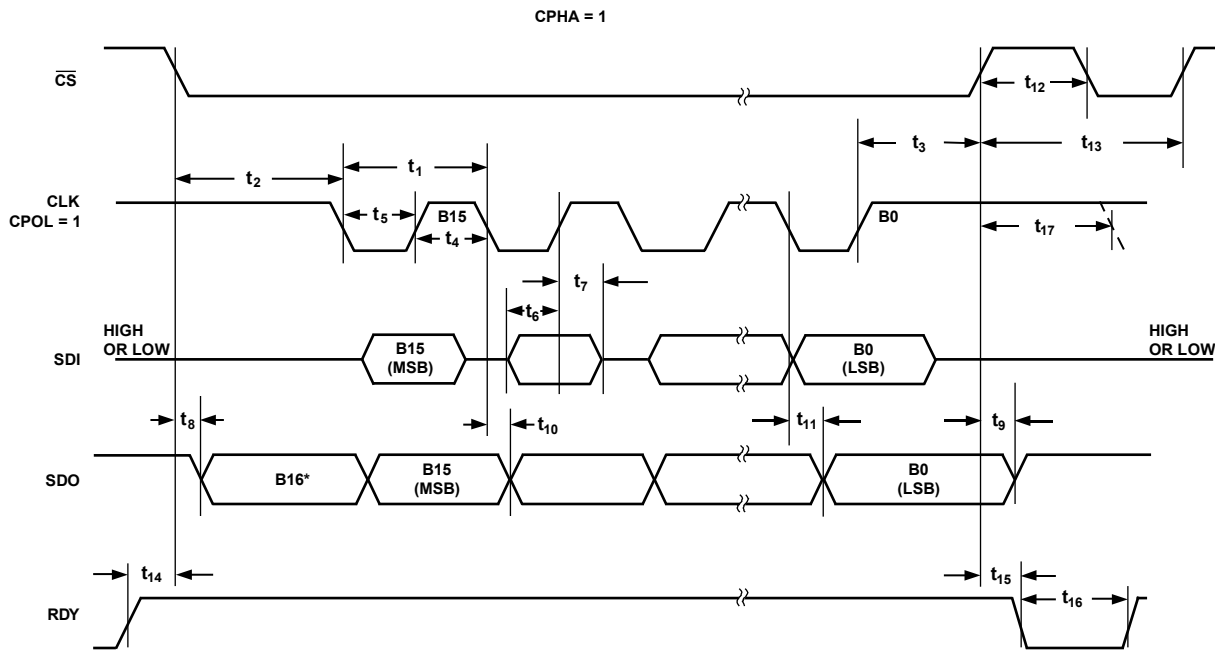
NOTES
1. B24 IS AN EXTRA BIT THAT IS NOT DEFINED, BUT IT IS USUALLY THE LSB OF THE CHARACTER THAT WAS PREVIOUSLY TRANSMITTED.
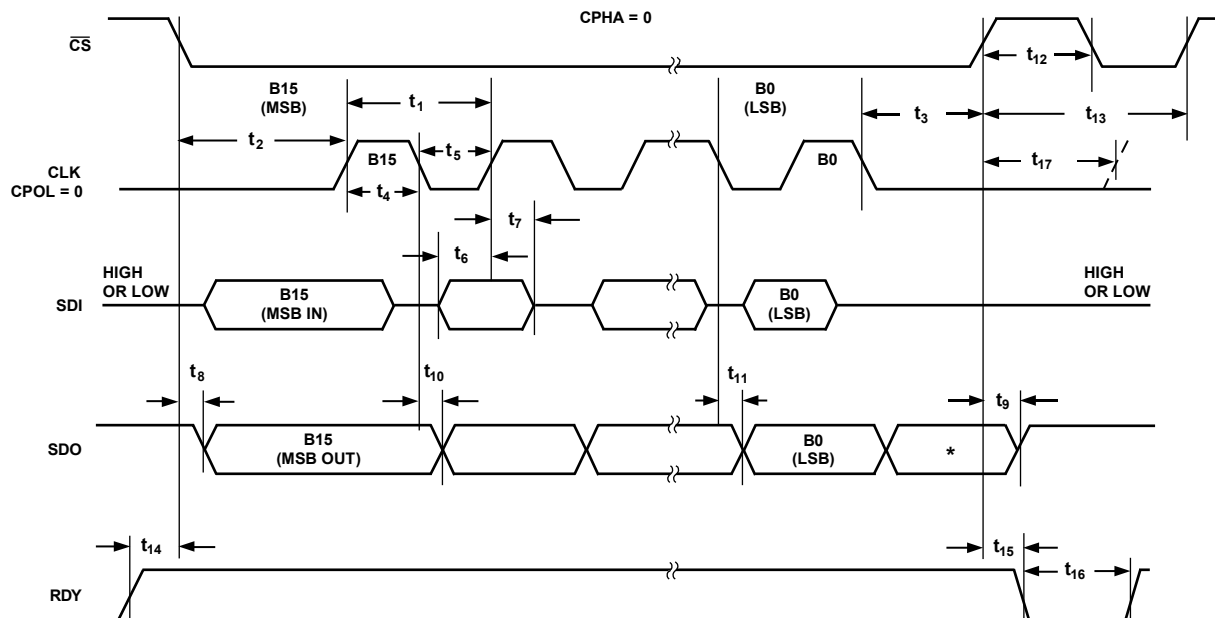2. THE CPOL = 1 MICROCONTROLLER COMMAND ALIGNS THE INCOMING DATA TO THE POSITIVE EDGE OF THE CLOCK.

Figure 2. CPHA = 1

NOTES
1. THIS EXTRA BIT IS NOT DEFINED, BUT IT IS USUALLY THE MSB OF THE CHARACTER THAT WAS JUST RECEIVED.
2. THE CPOL = 0 MICROCONTROLLER COMMAND ALIGNS THE INCOMING DATA TO THE POSITIVE EDGE OF THE CLOCK.

Figure 3. CPHA = 0

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +7 V
V_{SS} to GND	+0.3 V, −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
$A_X − B_X$, $A_X − W_X$, $B_X − W_X$	
Intermittent[1]	±20 mA
Continuous	±2 mA
Digital Inputs and Output Voltage to GND	−0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[2]	−40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Includes programming of nonvolatile memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead TSSOP (RU-16)	150	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
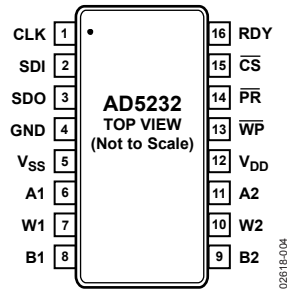
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input. The MSB is loaded first.
3	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. Command Instruction 9 and Command Instruction 10 activate the SDO output (see Table 8). Other commands shift out the previously loaded SDI bit pattern delayed by 16 clock pulses, allowing daisy-chain operation of multiple packages.
4	GND	Ground, Logic Ground Reference.
5	V_{SS}	Negative Power Supply. Connect to 0 V for single-supply applications.
6	A1	Terminal A of RDAC1.
7	W1	Wiper Terminal W of RDAC1, ADDR (RDAC1) = 0x0.
8	B1	Terminal B of RDAC1.
9	B2	Terminal B of RDAC2.
10	W2	Wiper Terminal W of RDAC2, ADDR (RDAC2) = 0x1.
11	A2	Terminal A of RDAC2.
12	V_{DD}	Positive Power Supply.
13	$\overline{WP}$	Write Protect. When active low, $\overline{WP}$ prevents any changes to the present register contents, except $\overline{PR}$, Command Instruction 1, and Command Instruction 8, which refresh the RDACx register from EEMEM. Execute an NOP instruction (Command Instruction 0) before returning $\overline{WP}$ to logic high.
14	$\overline{PR}$	Hardware Override Preset. Refreshes the scratch pad register with current contents of the EEMEMx register. Factory default loads Midscale 0x80 until EEMEMx is loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
15	$\overline{CS}$	Serial Register Chip Select, Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. This active-high, open-drain output requires a pull-up resistor. Identifies completion of Command Instruction 2, Command Instruction 3, Command Instruction 8, Command Instruction 9, Command Instruction 10, and $\overline{PR}$.

TYPICAL PERFORMANCE CHARACTERISTICS
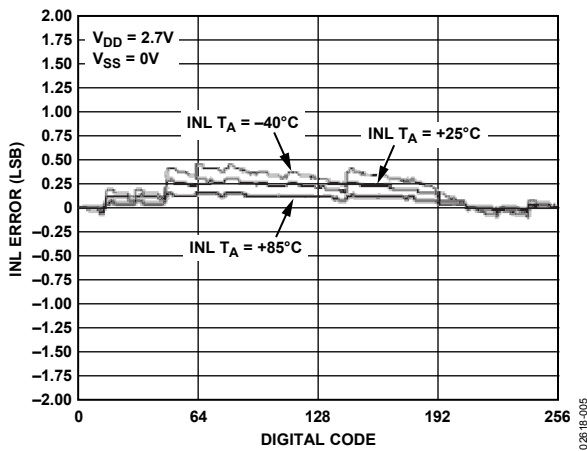
Figure 5. INL vs. Code; $T_A = -40°C$, $+25°C$, $+85°C$ Overlay
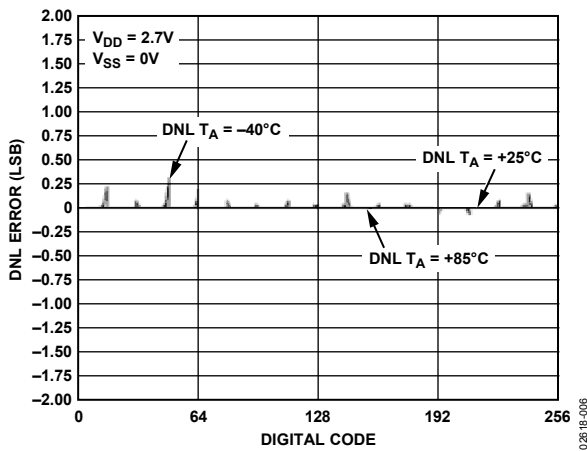
Figure 6. DNL vs. Code; $T_A = -40°C$, $+25°C$, $+85°C$ Overlay
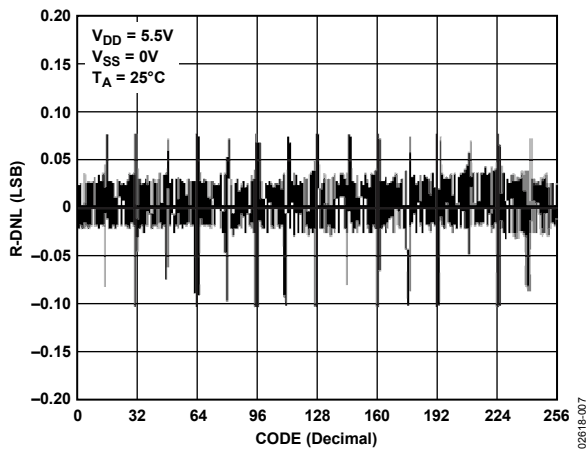
Figure 7. R-DNL vs. Code; $R_{AB} = 10 k\Omega$, $50 k\Omega$, $100 k\Omega$ Overlay
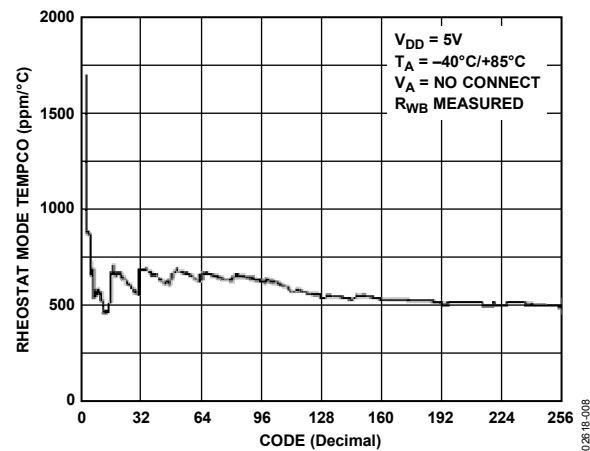
Figure 8. $\Delta R_{WB}/\Delta T$ vs. Code; $R_{AB} = 10 k\Omega$, $V_{DD} = 5 V$
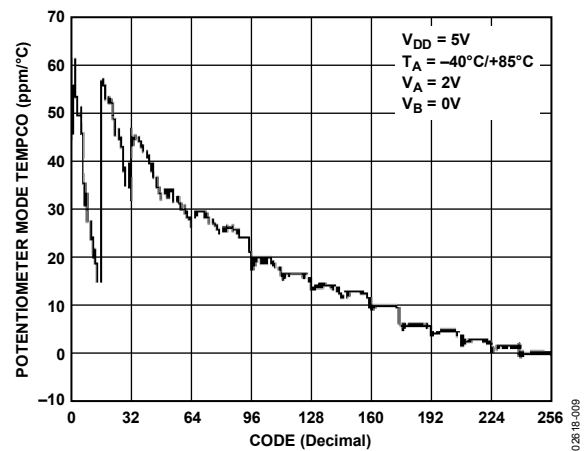
Figure 9. $\Delta V_{WB}/\Delta T$ vs. Code; $R_{AB} = 10 k\Omega$, $V_{DD} = 5 V$
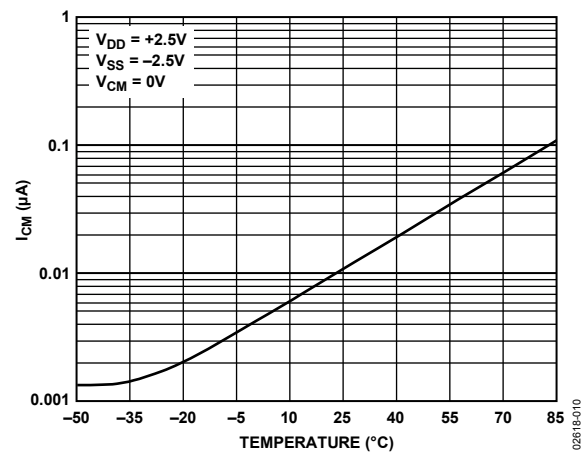
Figure 10. I_{CM} vs. Temperature (See Figure 30)
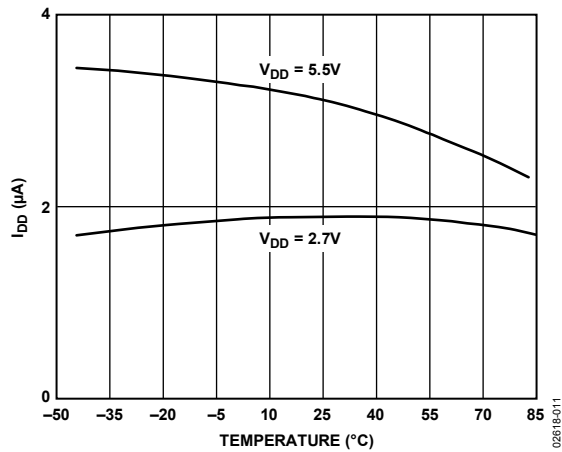
Figure 11. I_{DD} vs. Temperature
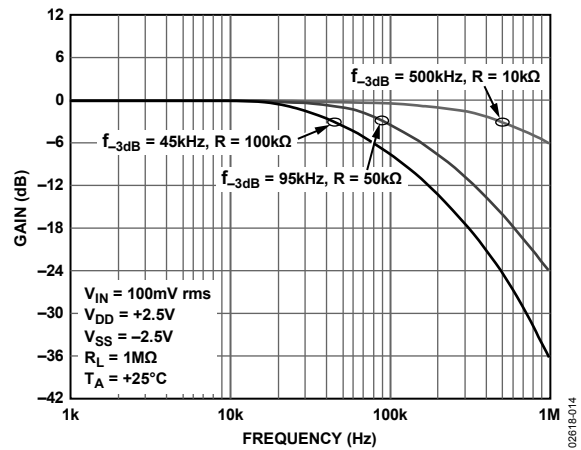
Figure 14. −3 dB Bandwidth vs. Resistance
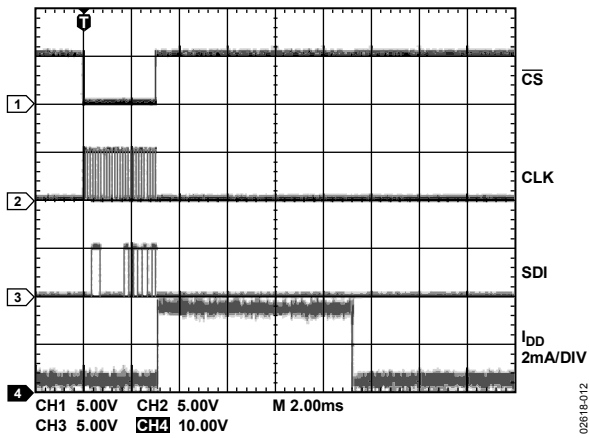
Figure 12. I_{DD} vs. Time (Save) Program Mode
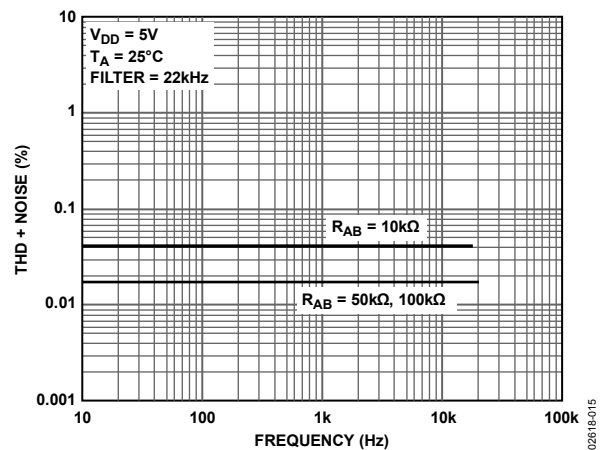
Figure 15. Total Harmonic Distortion + Noise vs. Frequency
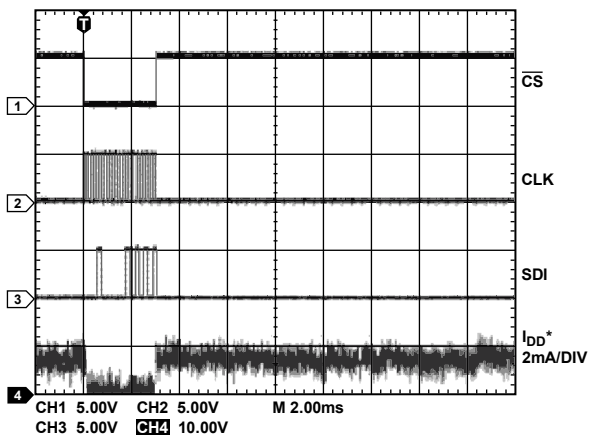
*SUPPLY CURRENT RETURNS TO MINIMUM POWER CONSUMPTION
IF COMMAND INSTRUCTION 0 (NOP) IS EXECUTED IMMEDIATELY
AFTER COMMAND INSTRUCTION 1 (READ EEMEM).

Figure 13. I_{DD} vs. Time Read Mode
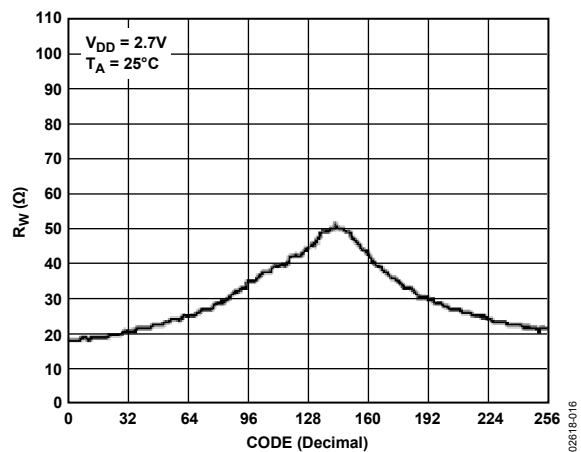
Figure 16. Wiper On Resistance vs. Code
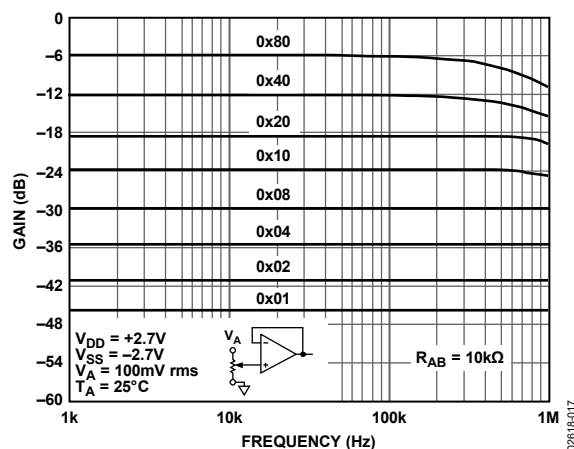
Figure 17. Gain vs. Frequency vs. Code, $R_{AB} = 10 k\Omega$

Figure 18. Gain vs. Frequency vs. Code, $R_{AB} = 50 k\Omega$

Figure 19. Gain vs. Frequency vs. Code, $R_{AB} = 100 k\Omega$

Figure 20. PSRR vs. Frequency

Figure 21. Analog Crosstalk vs. Frequency (See Figure 31)

TEST CIRCUITS

Figure 22 to Figure 32 define the test conditions that are used in the Specifications section.
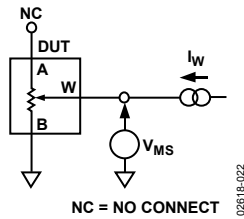
Figure 22. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)
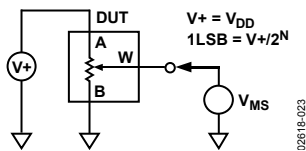
Figure 23. Potentiometer Divider Nonlinearity Error (INL, DNL)
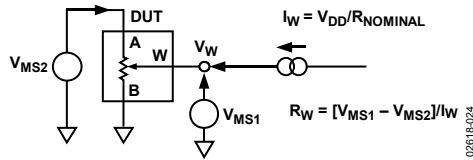
Figure 24. Wiper Resistance
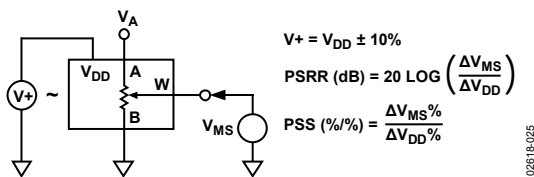
Figure 25. Power Supply Sensitivity (PSS, PSRR)
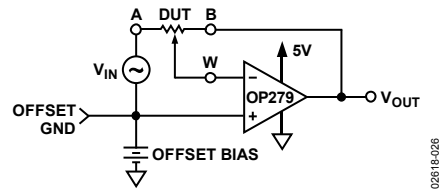
Figure 26. Inverting Gain
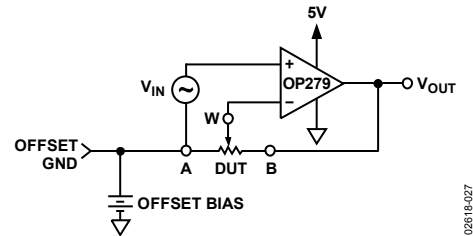
Figure 27. Noninverting Gain
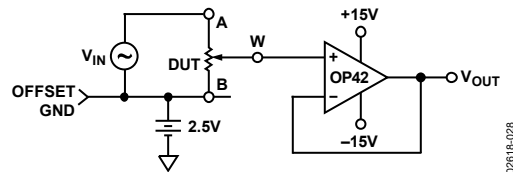
Figure 28. Gain vs. Frequency
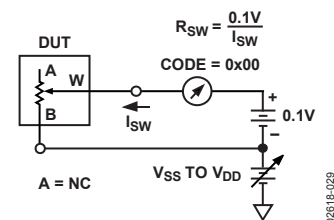
Figure 29. Incremental On Resistance
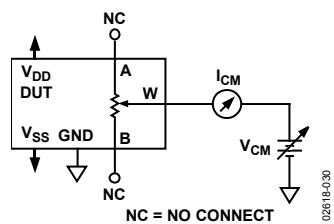
Figure 30. Common-Mode Leakage Current
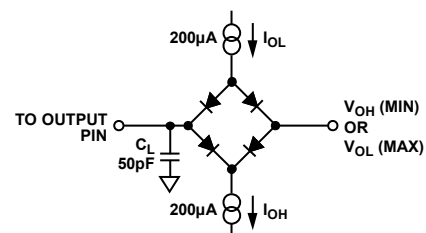
NOTES
1. THE DIODE BRIDGE TEST CIRCUIT IS EQUIVALENT TO THE APPLICATION CIRCUIT WITH $R_{PULL-UP}$ OF 2.2kΩ.

Figure 32. Load Circuit for Measuring V_{OH} and V_{OL}

$C_{TA} = 20 \, LOG \, [V_{OUT}/V_{IN}]$
NC = NO CONNECT
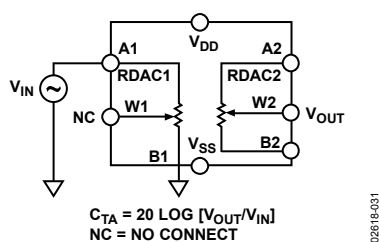
Figure 31. Analog Crosstalk

THEORY OF OPERATION

The AD5232 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$.

The basic voltage range is limited to a $|V_{DD} - V_{SS}| < 5.5$ V. The digital potentiometer wiper position is determined by the RDACx register contents. The RDACx register acts as a scratch pad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The scratch pad register can be programmed with any position value using the standard SPI serial interface mode by loading the complete representative data-word. When a desirable position is found, this value can be saved into a corresponding EEMEMx register. Thereafter, the wiper position is always set at that position for any future on-off-on power supply sequence. The EEMEM save process takes approximately 25 ms. During this time, the shift register is locked, preventing any changes from taking place. The RDY pin indicates the completion of this EEMEM save.

SCRATCH PAD AND EEMEM PROGRAMMING

The scratch pad register (RDACx register) directly controls the position of the digital potentiometer wiper. When the scratch pad register is loaded with all 0s, the wiper is connected to Terminal B of the variable resistor. When the scratch pad register is loaded with midscale code (1/2 of full-scale position), the wiper is connected to the middle of the variable resistor. When the scratch pad is loaded with full-scale code, which is all 1s, the wiper connects to Terminal A. Because the scratch pad register is a standard logic register, there is no restriction on the number of changes allowed. The EEMEMx registers have a program erase/write cycle limitation that is described in the Flash/EEMEM Reliability section.

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (by programming the scratch pad register) is accomplished by loading the serial data input register with Command Instruction 11, which includes the desired wiper position data. When the desired wiper position is found, the user loads the serial data input register with Command Instruction 2, which copies the desired wiper position data into the corresponding nonvolatile EEMEMx register. After 25 ms, the wiper position is permanently stored in the corresponding nonvolatile EEMEM location. Table 6 provides an application programming example listing the sequence of serial data input (SDI) words and the corresponding serial data output appearing at the serial data output (SDO) pin in hexadecimal format.

At system power-on, the scratch pad register is refreshed with the last value saved in the EEMEMx register. The factory preset EEMEM value is midscale. The scratch pad (wiper) register can be refreshed with the current contents of the nonvolatile EEMEMx register under hardware control by pulsing the PR pin.

The application programming example shown in Table 6 lists two digital potentiometers set to independent data values. The wiper positions are then saved in the corresponding nonvolatile EEMEMx registers.

Table 6. Application Programming Example

SDI	SDO	Action
0xB040	0xXXXX[1]	Loads 0x40 data into the RDAC1 register; Wiper W1 moves to 1/4 full-scale position.
0x20XX[1]	0xB040	Saves a copy of the RDAC1 register contents into the corresponding EEMEM1 register.
0xB180	0x20XX[1]	Loads 0x80 data into the RDAC2 register; Wiper W2 moves to 1/2 full-scale position.
0x21XX[1]	0xB180	Saves a copy of the RDAC2 register contents into the corresponding EEMEM2 register.

[1] X = don't care.

Note that the PR pulse first sets the wiper at midscale when it is brought to Logic 0. Then, on the positive transition to logic high, it reloads the DAC wiper register with the contents of EEMEMx. Many additional advanced programming commands are available to simplify the variable resistor adjustment process.

For example, the wiper position can be changed, one step at a time, by using the software controlled increment/decrement command instructions. The wiper position can be also be changed, 6 dB at a time, by using the shift left/right command instructions. After an increment, decrement, or shift command instruction is loaded into the shift register, subsequent CS strobes repeat this command instruction. This is useful for push-button control applications (see the Advanced Control Modes section). The SDO pin is available for daisy chaining and for readout of the internal register contents. The serial input data register uses a 16-bit instruction/address/data-word.

EEMEM PROTECTION

The write protect (WP) pin disables any changes of the scratch pad register contents, regardless of the software commands, except that the EEMEM setting can be refreshed using Instruction Command 8 and PR. Therefore, the WP pin provides a hardware EEMEM protection feature. Execute an NOP command (Command Instruction 0) before returning WP to logic high.

DIGITAL INPUT/OUTPUT CONFIGURATION

All digital inputs are ESD protected, high input impedance that can be driven directly from most digital sources. The PR and WP pins, which are active at logic low, must be biased to V_{DD} if they are not being used. No internal pull-up resistors are present on any digital input pins.

The SDO and RDY pins are open-drain, digital outputs when pull-up resistors are needed, but only if these functions are in use. A resistor value in the range of 1 kΩ to 10 kΩ optimizes the power and switching speed trade-off.

SERIAL DATA INTERFACE

The AD5232 contains a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK) and uses a 16-bit serial data-word that is loaded MSB first. The format of the SPI-compatible word is shown in Table 7. The chip select ($\overline{CS}$) pin must be held low until the complete data-word is loaded into the SDI pin. When $\overline{CS}$ returns high, the serial data-word is decoded according to the instructions in Table 8. The command bits (Cx) control the operation of the digital potentiometer. The address bits (Ax) determine which register is activated. The data bits (Dx) are the values that are loaded into the decoded register. Table 9 provides an address map of the EEMEM locations. The last command instruction executed prior to a period of no programming activity should be the no operation (NOP) command instruction (Command Instruction 0). This instruction places the internal logic circuitry in a minimum power dissipation state.
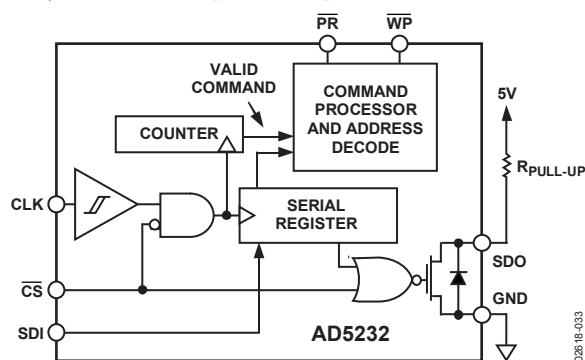
Figure 33. Equivalent Digital Input/Output Logic

The AD5232 has an internal counter that counts a multiple of 16 bits (per frame) for proper operation. For example, the AD5232 works with a 16-bit or 32-bit word, but it cannot work properly with a 15-bit or 17-bit word. To prevent data from mislocking (due to noise, for example), the counter resets if the count is not a multiple of 4 when $\overline{CS}$ goes high, but the data remains in the register if the count is a multiple of 4. In addition, the AD5232 has a subtle feature whereby, if $\overline{CS}$ is pulsed without CLK and SDI, the part repeats the previous command (except during power-up). As a result, care must be taken to ensure that no excessive noise exists in the CLK or $\overline{CS}$ line that may alter the effective number of bits pattern.

The equivalent serial data input and output logic is shown in Figure 33. The open-drain SDO is disabled whenever $\overline{CS}$ is logic high. The SPI interface can be used in two slave modes: CPHA = 1, CPOL = 1; and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits that dictate SPI timing in the following microprocessors and MicroConverter® devices: the ADuC812 and the ADuC824, the M68HC11, and the MC68HC16R1/916R1. ESD protection of the digital inputs is shown in Figure 34 and Figure 35.
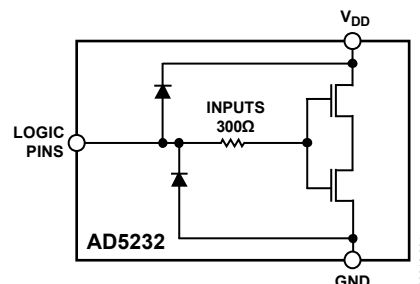
Figure 34. Equivalent ESD Digital Input Protection
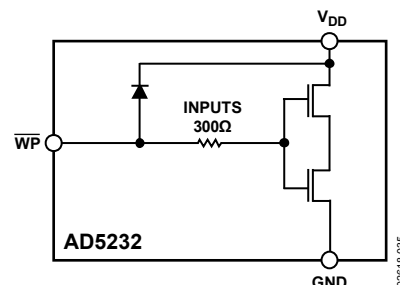
Figure 35. Equivalent $\overline{WP}$ Input Protection

DAISY-CHAINING OPERATION

The SDO pin serves two purposes: it can be used to read back the contents of the wiper setting and the EEMEM using Command Instruction 9 and Command Instruction 10 (see Table 8), or it can be used for daisy-chaining multiple devices. The remaining command instructions are valid for daisy-chaining multiple devices in simultaneous operations. Daisy chaining minimizes the number of port pins required from the controlling IC (see Figure 36). The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor if this function is used. As shown in Figure 36, users must tie the SDO pin of one package to the SDI pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-to-SDI interface may require additional time delay between subsequent packages. If two AD5232s are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits with the same format go to U1. The 16 bits are formatted to contain the 4-bit instruction, followed by the 4-bit address, followed by the eight bits of data. The $\overline{CS}$ pin should be kept low until all 32 bits are locked into their respective serial registers. The $\overline{CS}$ pin is then pulled high to complete the operation.
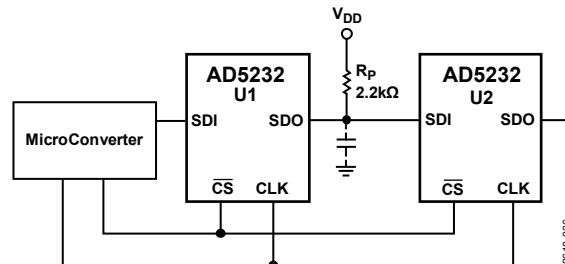
Figure 36. Daisy-Chain Configuration Using the SDO

Command bits are identified as Cx, address bits are Ax, and data bits are Dx. The command instruction codes are defined in Table 8. The SDO output shifts out the last eight bits of data clocked into the serial register for daisy-chain operation, with the following exception: after Command Instruction 9 or Command Instruction 10, the selected internal register data is present in Data Byte 0. The command instructions following Command Instruction 9 and Command Instruction 10 must be full 16-bit data-words to completely clock out the contents of the serial register. The RDACx register is a volatile scratch pad register that is refreshed at power-on from the corresponding nonvolatile EEMEMx register. The increment, decrement, and shift command instructions ignore the contents of Data Byte 0 in the shift register. Execution of the operation noted in Table 8 occurs when the $\overline{CS}$ strobe returns to logic high. Execution of an NOP instruction minimizes power dissipation.

Table 7. 16-Bit Serial Data Word

MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 8. Instruction/Operation Truth Table

| Comm. Inst. No.	Instruction Byte 1 B15 C3	C2	C1	C0	A3	A2	A1	B8 A0	Data Byte 0 B7 D7	D6	D5	D4	D3	D2	D1	B0 D0	Operation
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	No operation (NOP). Do nothing.
1	0	0	0	1	0	0	0	A0	X	X	X	X	X	X	X	X	Write contents of EEMEM (A0) to the RDAC (A0) register. This command leaves the device in the read program power state. To return the part to the idle state, perform Command Instruction 0 (NOP).
2	0	0	1	0	0	0	0	A0	X	X	X	X	X	X	X	X	Save wiper setting. Write contents of RDAC (ADDR) to EEMEM (A0).
3	0	0	1	1		ADDR			D7	D6	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data Byte 0 to EEMEM (ADDR).
4	0	1	0	0	0	0	0	A0	X	X	X	X	X	X	X	X	Decrement 6 dB right shift contents of RDAC (A0). Stops at all 0s.
5	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement all 6 dB right shift contents of all RDAC registers. Stops at all 0s.
6	0	1	1	0	0	0	0	A0	X	X	X	X	X	X	X	X	Decrement contents of RDAC (A0) by 1. Stops at all 0s.
7	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement contents of all RDAC registers by 1. Stops at all 0s.
8	1	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	Reset. Load all RDACs with their corresponding, previously saved EEMEM values.
9	1	0	0	1		ADDR			X	X	X	X	X	X	X	X	Write contents of EEMEM(ADDR) to Serial Register Data Byte 0.
10	1	0	1	0	0	0	0	A0	X	X	X	X	X	X	X	X	Write contents of RDAC (A0) to Serial Register Data Byte 0.
11	1	0	1	1	0	0	0	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data Byte 0 to RDAC (A0).
12	1	1	0	0	0	0	0	A0	X	X	X	X	X	X	X	X	Increment 6 dB left shift contents of RDAC (A0). Stops at all 1s.
13	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment all 6 dB left shift contents of all RDAC registers. Stops at all 1s.
14	1	1	1	0	0	0	0	A0	X	X	X	X	X	X	X	X	Increment contents of RDAC (A0) by 1. Stops at all 1s.
15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment contents of all RDAC registers by 1. Stops at all 1s.

ADVANCED CONTROL MODES

The AD5232 digital potentiometer contains a set of user programming features to address the wide variety of applications available to these universal adjustment devices. Key programming features include the following:

- Independently programmable read and write to all registers
- Simultaneous refresh of all RDAC wiper registers from corresponding internal EEMEM registers
- Increment and decrement command instructions for each RDAC wiper register
- Left and right bit shift of all RDAC wiper registers to achieve 6 dB level changes
- Nonvolatile storage of the present scratch pad RDACx register values into the corresponding EEMEMx register
- Fourteen extra bytes of user-addressable, electrical erasable memory

Increment and Decrement Commands

The increment and decrement command instructions (Command Instruction 14, Command Instruction 15, Command Instruction 6, and Command Instruction 7) are useful for the basic servo adjustment application. These commands simplify microcontroller software coding by eliminating the need to perform a readback of the current wiper position and then add a 1 to the register contents using the microcontroller adder. The microcontroller sends an increment command instruction (Command Instruction 14) to the digital potentiometer, which automatically moves the wiper to the next resistance segment position. The master increment command instruction (Command Instruction 15) moves all potentiometer wipers by one position from their present position to the next resistor segment position. The direction of movement is referenced to Terminal B. Thus, each Command Instruction 15 moves the wiper tap position farther from Terminal B.

Logarithmic Taper Mode Adjustment

Programming instructions allow decrement and increment wiper position control by an individual potentiometer or in a ganged potentiometer arrangement, where both wiper positions are changed at the same time. These settings are activated by the 6 dB decrement and 6 dB increment command instructions (Command Instruction 4 and Command Instruction 5, and Command Instruction 12 and Command Instruction 13, respectively). For example, starting with the wiper connected to Terminal B, executing nine increment instructions (Command Instruction 12) moves the wiper in 6 dB steps from the 0% of the R_{BA} (Terminal B) position to the 100% of the R_{BA} position of the AD5232 8-bit potentiometer. The 6 dB increment instruction doubles the value of the RDACx register contents each time the command is executed. When the wiper position is greater than midscale, the last 6 dB increment command instruction causes the wiper to go to the full-scale 255 code position. Any addi-

tional 6 dB instruction does not change the wiper position from full scale (RDACx register code = 255).

Figure 37 illustrates the operation of the 6 dB shifting function on the individual RDACx register data bits for the 8-bit AD5232 example. Each line going down the table represents a successive shift operation. Note that the Left Shift 12 and Left Shift 13 command instructions were modified so that if the data in the RDACx register is equal to 0 and is left shifted, it is then set to Code 1.

In addition, the left shift commands were modified so that if the data in the RDAC register is greater than or equal to midscale and is left shifted, the data is then set to full scale. This makes the left shift function as close to ideally logarithmic as possible.

The Right Shift 4 and Right Shift 5 command instructions are ideal only if the LSB is 0 (that is, ideal logarithmic, with no error). If the LSB is a 1, the right shift function generates a linear half-LSB error that translates to a code-dependent logarithmic error for odd codes only, as shown in Figure 38. The plot shows the errors of the odd codes.

LEFT SHIFT	RIGHT SHIFT
0000 0000	1111 1111
0000 0001	0111 1111
0000 0010	0011 1111
0000 0100	0001 1111
0000 1000	0000 1111
0001 0000	0000 0111
0010 0000	0000 0011
0100 0000	0000 0001
1000 0000	0000 0000
1111 1111	0000 0000
1111 1111	0000 0000

LEFT SHIFT (+6dB)   RIGHT SHIFT (–6dB)

Figure 37. Detail Left and Right Shift Function

Actual conformance to a logarithmic curve between the data contents in the RDACx register and the wiper position for each Right Shift 4 and Right Shift 5 command execution contains an error only for the odd codes. The even codes are ideal, with the exception of zero right shift or greater than half-scale left shift. Figure 38 shows plots of Log_Error, that is, $20 \times \log10$ (error/code). For example, Code 3 Log_Error = $20 \times \log10$ (0.5/3) = −15.56 dB, which is the worst case. The plot of Log_Error is more signifi-cant at the lower codes.
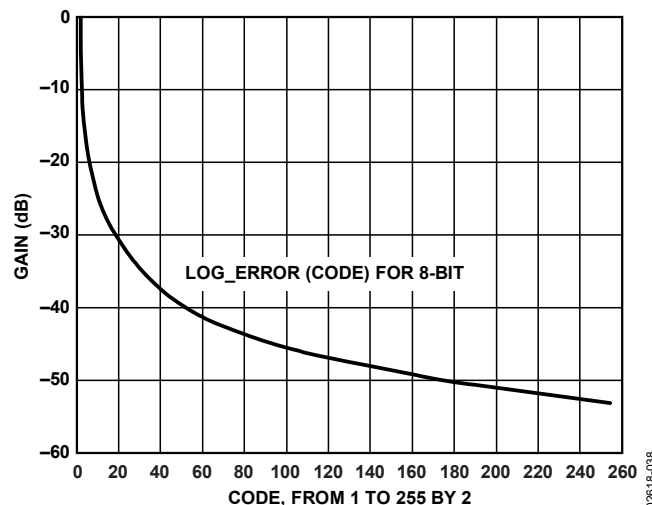

Figure 38. Plot of Log_Error Conformance for Odd Codes Only (Even Codes Are Ideal)

USING ADDITIONAL INTERNAL, NONVOLATILE EEMEM

The AD5232 contains additional internal user storage registers (EEMEM) for saving constants and other 8-bit data. Table 9 provides an address map of the internal nonvolatile storage registers, which are shown in the functional block diagram as EEMEM1, EEMEM2, and bytes of USER EEMEM.

Note the following about EEMEM function:

- RDAC data stored in EEMEM locations are transferred to their corresponding RDACx register at power-on or when Command Instruction 1 and Command Instruction 8 are executed.
- USERx refers to internal nonvolatile EEMEM registers that are available to store and retrieve constants by using Command Instruction 3 and Command Instruction 9, respectively.
- The EEMEM locations are one byte each (eight bits).
- Execution of Command Instruction 1 leaves the device in the read mode power consumption state. When the final Command Instruction 1 is executed, the user should perform an NOP (Command Instruction 0) to return the device to the low power idle state.

Table 9. EEMEM Address Map

EEMEM Address (ADDR)	EEMEM Contents of Each Device EEMEM (ADDR)
0000	RDAC1
0001	RDAC2
0010	USER 1
0011	USER 2
0100	USER 3
0101	USER 4
***	***
1111	USER 14

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supply of the digital potentiometer defines the boundary conditions for proper 3-terminal programmable resistance operations. Signals present on Terminal A, Terminal B, and Wiper Terminal W that exceed V_{DD} or V_{SS} are clamped by a forward biased diode (see Figure 39).

The ground pin of the AD5232 device is used primarily as a digital ground reference that needs to be tied to the common ground of the PCB. The digital input logic signals to the AD5232 must be referenced to the ground (GND) pin of the device and satisfy the minimum input logic high level and the maximum input logic low level that are defined in the Specifications section.

An internal level shift circuit between the digital interface and the wiper switch control ensures that the common-mode voltage range of the three terminals, Terminal A, Terminal B, and Wiper Terminal W, extends from V_{SS} to V_{DD}.
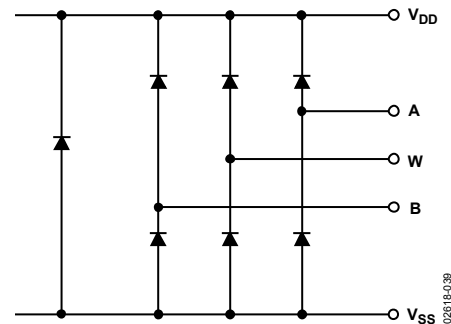
Figure 39. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

Table 10. RDAC and Digital Register Address Map

Register Address (ADDR)	Name of Register[1]
0000	RDAC1
0001	RDAC2

[1] The RDACx registers contain data that determines the position of the variable resistor wiper.

DETAILED POTENTIOMETER OPERATION

The actual structure of the RDACx is designed to emulate the performance of a mechanical potentiometer. The RDACx contains multiple strings of connected resistor segments, with an array of analog switches that act as the wiper connection to several points along the resistor array. The number of points is equal to the resolution of the device. For example, the AD5232 has 256 connection points, allowing it to provide better than 0.5% setability resolution. Figure 40 provides an equivalent diagram of the connections between the three terminals that make up one channel of the RDACx. The SW_A and SW_B switches are always on, whereas only one of the SW(0) to SW(2^N–1) switches is on at a time, depending on the resistance step decoded from the data bits. The resistance contributed by R_W must be accounted for in the output resistance.

NOTES
1. DIGITAL CIRCUITRY OMITTED FOR CLARITY

Figure 40. Equivalent RDAC Structure

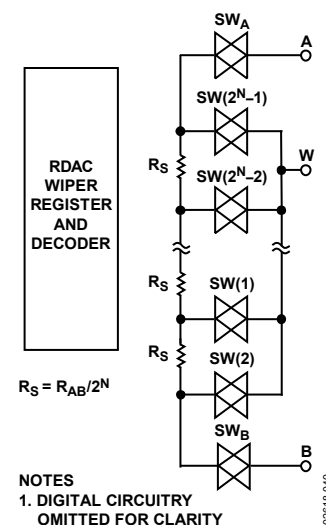**Table 11. Nominal Individual Segment Resistor Values (Ω)**

| Device Resolution | Segmented Resistor Size for R_{AB} End-to-End Values | | |
	10 kΩ Version	50 kΩ Version	100 kΩ Version
8-Bit	78.10	390.5	781.0

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistances of the RDACx between Terminal A and Terminal B are available with values of 10 kΩ, 50 kΩ, and 100 kΩ. The final digits of the part number determine the nominal resistance value; for example, 10 kΩ = 10; 100 kΩ = 100. The nominal resistance (R_{AB}) of the AD5232 VR has 256 contact points accessed by Wiper Terminal W, plus the Terminal B contact. The 8-bit data-word in the RDACx latch is decoded to select one of the 256 possible settings.

The general transfer equation, which determines the digitally programmed output resistance between Wx and Bx, is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \qquad (1)$$

where:
D is the decimal equivalent of the data contained in the RDACx register.
R_{AB} is the nominal resistance between Terminal A and Terminal B.
R_W is the wiper resistance.

Table 12 lists the output resistance values that are set for the RDACx latch codes shown for 8-bit, 10 kΩ potentiometers.

Table 12. Nominal Resistance Value at Selected Codes for R_{AB} = 10 kΩ

D (Dec)	R_{WB} (D) (Ω)	Output State
255	10011	Full scale
128	5050	Midscale
1	89	1 LSB
0	50	Zero scale[1] (wiper contact resistance)

[1] Note that in the zero-scale condition, a finite wiper resistance of 50 Ω is present. Care should be taken to limit the current flow between Wx and Bx in this state to a maximum continuous value of 2 mA to avoid degradation or possible destruction of the internal switch metallization. Intermittent current operation to 20 mA is allowed.

Like the mechanical potentiometer that the RDACx replaces, the AD5232 parts are totally symmetrical. The resistance between the Wiper Terminal W and Terminal A also produces a digitally controlled resistance, R_{WA}. Figure 41 shows the symmetrical programmability of the various terminal connections.
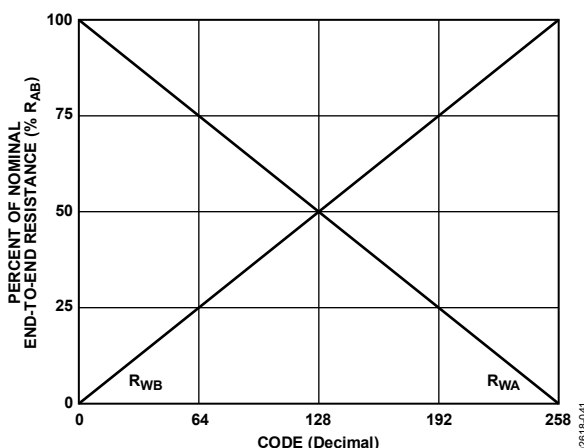

Figure 41. Symmetrical RDAC Operation

When these terminals are used, Terminal B should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \qquad (2)$$

where:
D is the decimal equivalent of the data contained in the RDAC register.
R_{AB} is the nominal resistance between Terminal A and Terminal B.
R_W is the wiper resistance.

Table 13 lists the output resistance values that are set for the RDACx latch codes shown for 8-bit, 10 kΩ potentiometers.

Table 13. Nominal Resistance Value at Selected Codes for R_{AB} = 10 kΩ

D (Dec)	R_{WA} (D) (Ω)	Output State
255	89	Full scale
128	5050	Midscale
1	10011	1 LSB
0	10050	Zero scale

The multichannel AD5232 has a ±0.2% typical distribution of internal channel-to-channel R_{BA} match. Device-to-device matching is dependent on process lot and exhibits a −40% to +20% variation. The change in R_{BA} with temperature has a 600 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example, connecting Terminal A to 5 V and Terminal B to GND produces an output voltage at the wiper that can be any value from 0 V to 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A to Terminal B, divided by the 2^N position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to Terminal A to Terminal B is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{WA}(D)}{R_{AB}} \times V_B \qquad (3)$$

where $R_{WB}(D)$ can be obtained from Equation 1 and $R_{WA}(D)$ can be obtained from Equation 2.

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors, not the absolute value; therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction between Terminal A, Terminal B, and Wiper Terminal W as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

OPERATION FROM DUAL SUPPLIES

The AD5232 can be operated from dual supplies, enabling control of ground-referenced ac signals (see Figure 42 for a typical circuit connection).
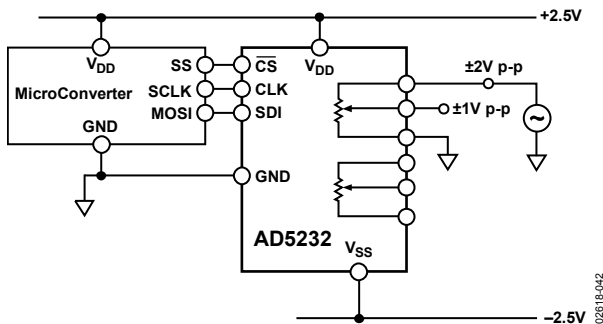

Figure 42. Operation from Dual Supplies

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. When configured as a potentiometer divider, the −3 dB bandwidth of the AD5232BRU10 (10 kΩ resistor) measures 500 kHz at half scale. Figure 14 provides the large signal BODE plot characteristics of the three resistor versions: 10 kΩ, 50 kΩ, and 100 kΩ (see Figure 43 for a parasitic simulation model of the RDAC circuit).
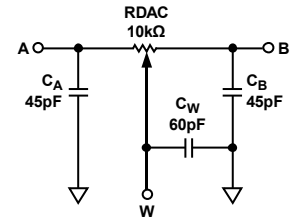

Figure 43. RDAC Circuit Simulation Model for RDACx = 10 kΩ

The following code provides a macro model net list for the 10 kΩ RDAC:

```
.PARAM DW=255, RDAC=10E3
*
.SUBCKT DPOT (A,W,B)
*
CA A 0 {45E-12}
RAW A W {(1-DW/256)*RDAC+50}
CW W 0 60E-12
RBW W B {DW/256*RDAC+50}
CB B 0 {45E-12}
*
.ENDS DPOT
```

APPLICATION PROGRAMMING EXAMPLES

The command sequence examples shown in Table 14 to Table 18 have been developed to illustrate a typical sequence of events for the various features of the AD5232 nonvolatile digital potentiometer. Table 14 illustrates setting two digital potentiometers to independent data values.

Table 14.

SDI	SDO	Action
0xB140	0xXXXX	Loads 0x40 data into the RDAC2 register; Wiper W2 moves to 1/4 full-scale position.
0xB080	0xB140	Loads 0x80 data into the RDAC1 register; Wiper W1 moves to 1/2 full-scale position.

Table 15 illustrates the active trimming of one potentiometer, followed by a save to nonvolatile memory (PCB calibrate).

Table 15.

SDI	SDO	Action
0xB040	0xXXXX	Loads 0x40 data into the RDAC1 register; Wiper W1 moves to 1/4 full-scale position.
0xE0XX	0xB040	Increments the RDAC1 register by 1, to 0x41; Wiper W1 moves one resistor segment away from Terminal B.
0xE0XX	0xE0XX	Increments the RDAC1 register by 1, to 0x42; Wiper W1 moves one more resistor segment away from Terminal B. Continue until desired the wiper position is reached.
0x20XX	0xE0XX	Saves the RDAC1 register data into the corresponding nonvolatile EEMEM1 memory: ADDR = 0x0.

Table 16 illustrates using the left shift-by-one to change circuit gain in 6 dB steps.

Table 16.

SDI	SDO	Action
0xC1XX	0xXXXX	Moves Wiper W2 to double the present data value contained in the RDAC2 register in the direction of Terminal A.
0xC1XX	0xXXXX	Moves Wiper W2 to double the present data value contained in the RDAC2 register in the direction of Terminal A.

Table 17 illustrates storing additional data in nonvolatile memory.

Table 17.

SDI	SDO	Action
0x3280	0xXXXX	Stores 0x80 data in spare EEMEM location, USER1.
0x3340	0xXXXX	Stores 0x40 data in spare EEMEM location, USER2.

Table 18 illustrates reading back data from various memory locations.

Table 18.

SDI	SDO	Action
0x94XX	0xXXXX	Prepares data read from USER3 location. (USER3 is already loaded with 0x80.)
0x00XX	0xXX80	Instruction 0 (NOP) sends 16-bit word out of SDO where the last eight bits contain the contents of USER3 location. The NOP command ensures that the device returns to the idle power dissipation state.

EQUIPMENT CUSTOMER START-UP SEQUENCE FOR A PCB CALIBRATED UNIT WITH PROTECTED SETTINGS

1. For the PCB setting, tie $\overline{WP}$ to GND to prevent changes in the PCB wiper set position.
2. Set power V_{DD} and V_{SS} with respect to GND.
3. As an optional step, strobe the $\overline{PR}$ pin to ensure full power-on preset of the wiper register with EEMEM contents in unpredictable supply sequencing environments.

FLASH/EEMEM RELIABILITY

The Flash/EE memory array on the AD5232 is fully qualified for two key Flash/EE memory characteristics: namely, Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events. These events are defined as follows:

1. Initial page erase sequence
2. Read/verify sequence
3. Byte program sequence
4. Second read/verify sequence

During reliability qualification, Flash/EE memory is cycled from 0x00 to 0xFF until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications section, the AD5232 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Std. 22, Method A117 over the industrial temperature range of −40°C to +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the AD5232 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature of $T_J = 55°C$. As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, as described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J, as shown in Figure 44.
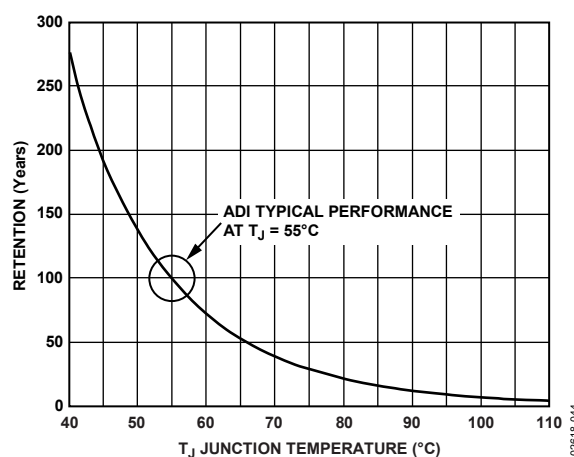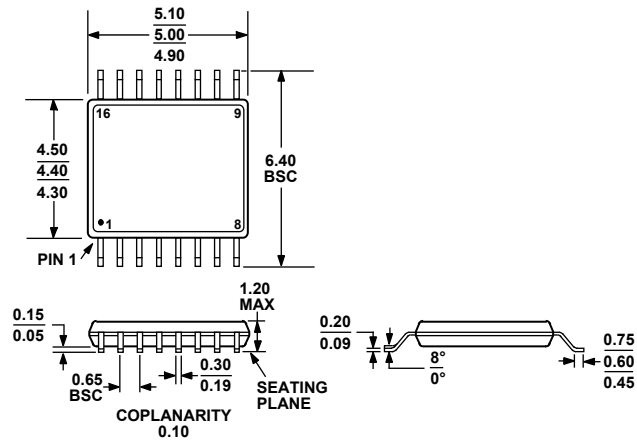

Figure 44. Flash/EE Memory Data Retention

EVALUATION BOARD

Analog Devices, Inc., offers a user-friendly EVAL-AD5232-10EBZ evaluation kit that can be controlled by a personal computer through a printer port. The driving program is self-contained; no programming languages or skills are needed.

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 45. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Number of Channels	End-to-End R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding[2]
AD5232BRU10	2	10	−40°C to +85°C	16-Lead TSSOP	RU-16	96	5232B10
AD5232BRU10-REEL7	2	10	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000	5232B10
AD5232BRUZ10	2	10	−40°C to +85°C	16-Lead TSSOP	RU-16	96	5232B10
AD5232BRUZ10-REEL7	2	10	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000	5232B10
AD5232BRU50	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96	5232B50
AD5232BRU50-REEL7	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000	5232B50
AD5232BRUZ50	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	96	5232B50
AD5232BRUZ50-REEL7	2	50	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000	5232B50
AD5232BRU100	2	100	−40°C to +85°C	16-Lead TSSOP	RU-16	96	5232BC
AD5232BRU100-REEL7	2	100	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000	5232BC
AD5232BRUZ100	2	100	−40°C to +85°C	16-Lead TSSOP	RU-16	96	5232BC
AD5232BRUZ100-RL7	2	100	−40°C to +85°C	16-Lead TSSOP	RU-16	1,000	5232BC
EVAL-AD5232-10EBZ		10		Evaluation Board		1	

[1] Z = RoHS Compliant Part.

[2] Line 1 contains the Analog Devices logo, followed by the date code: YYWW. Line 2 contains the model number, followed by the end-to-end resistance value. (Note that C = 100 kΩ).
OR
Line 1 contains the model number. Line 2 contains the Analog Devices logo, followed by the end-to-end resistance value. Line 3 contains the date code: YYWW.

NOTES

NOTES

www.analog.com