Virtex-6 CXT Family Data Sheet

DS153 (v1.6) February 11, 2011 **Product Specification**

General Description

Virtex®-6 CXT FPGAs provide designers needing power-optimized 3.75 Gb/s transceiver performance with an optimized ratio of built-in system-level blocks. These include 36 Kb block RAM/FIFOs, up to 15 Mb of block RAM, up to 768 DSP48E1 slices, enhanced mixed-mode clock management blocks, PCI Express® (GEN 1) compatible integrated blocks, a tri-mode Ethernet media access controller (MAC), up to 241K logic cells, and strong IP support. Using the third generation ASMBL™ (Advanced Silicon Modular Block) column-based architecture, the Virtex-6 CXT family also contains SelectIO™ technology with built-in digitally controlled impedance, ChipSync™ source-synchronous interface blocks, enhanced mixed-mode clock management blocks, and advanced configuration options. Customers needing higher transceiver speeds, greater I/O performance, additional Ethernet MACs, or greater capacity should instead use the Virtex-6 LXT or SXT families. Built on a 40 nm state-of-the-art copper process technology, Virtex-6 CXT FPGAs are a programmable alternative to custom ASIC technology. Virtex-6 CXT FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins.

Summary of Virtex-6 CXT FPGA Features

- Advanced, high-performance, FPGA Logic
  - Real 6-input look-up table (LUT) technology
  - Dual LUT5 (5-input LUT) option
  - LUT/dual flip-flop pair for applications requiring rich register mix
  - Improved routing efficiency
  - 64-bit (or 32 x 2-bit) distributed LUT RAM option
  - SRL32/dual SRL16 with registered outputs option
- Powerful mixed-mode clock managers (MMCM)
  - MMCM blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input-jitter filtering, and phase-matched clock division
- 36-Kb block RAM/FIFOs
  - Dual-port RAM blocks
  - Programmable
    - Dual-port widths up to 36 bits
    - Simple dual-port widths up to 72 bits
  - Enhanced programmable FIFO logic
  - Built-in optional error-correction circuitry
  - Optionally use each block as two independent 18 Kb blocks
- High-performance parallel SelectIO technology
  - 1.2 to 2.5V I/O operation
  - Source-synchronous interfacing using ChipSync™ technology
  - Digitally controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support with integrated write-leveling capability
- Advanced DSP48E1 slices
  - 25 x 18, two's complement multiplier/accumulator
  - Optional pipelining
  - New optional pre-adder to assist filtering applications
  - Optional bitwise logic functionality
  - Dedicated cascade connections
- Flexible configuration options
  - SPI and Parallel Flash interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Automatic bus width detection
- Integrated interface blocks for PCI Express designs
  - Compliant to the PCI Express Base Specification 2.0
  - Gen1 Endpoint (2.5 Gb/s) support with GTX transceivers
  - x1, x2, x4, or x8 lane support per block
  - One virtual channel, eight traffic classes
- GTX transceivers: 150 Mb/s to 3.75 Gb/s
- Integrated 10/100/1000 Mb/s Ethernet MAC block
  - Supports 1000BASE-X PCS/PMA and SGMII using GTX transceivers
  - Supports MII, GMII, and RGMII using SelectIO technology resources
- 40 nm copper CMOS process technology
- 1.0V core voltage
- Two speed grades (-1 and -2)
- Two temperature grades (commercial and industrial)
- High signal-integrity flip-chip packaging available in standard or Pb-free package options
- Compatibility across sub-families: CXT, LXT, and SXT devices are footprint compatible in the same package

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Virtex-6 CXT FPGA Feature Summary

Table 1: **Virtex-6 CXT FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices(2)	Block RAM Blocks			MMCMs(4)	Interface Blocks for PCI Express	Ethernet MACs(5)	Maximum GTX Transceivers	Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb(3)	36 Kb	Max (Kb)						
XC6VCX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	1	12	9	360
XC6VCX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	1	16	15	600
XC6VCX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	1	16	15	600
XC6VCX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	1	16	18	600

Notes:

1. Each Virtex-6 CXT FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two mixed-mode clock managers (MMCM).
5. This table lists individual Ethernet MACs per device.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Virtex-6 CXT FPGA Device-Package Combinations and Maximum I/Os

Virtex-6 CXT FPGA package combinations with the maximum available I/Os per package are shown in Table 2.

Table 2: **Virtex-6 CXT FPGA Device-Package Combinations and Maximum Available I/Os**

Package	FF484 FFG484		FF784 FFG784		FF1156 FFG1156	
Size (mm)	23 x 23		29 x 29		35 x 35	
Device	GTs	I/O	GTs	I/O	GTs	I/O
XC6VCX75T	8 GTXs	240	12 GTXs	360		
XC6VCX130T	8 GTXs	240	12 GTXs	400	16 GTXs	600
XC6VCX195T			12 GTXs	400	16 GTXs	600
XC6VCX240T			12 GTXs	400	16 GTXs	600

Notes:

1. Flip-chip packages are also available in Pb-Free versions (FFG).

Virtex-6 CXT FPGA Ordering Information

The Virtex-6 CXT FPGA ordering information shown in Figure 1 applies to all packages including Pb-Free.

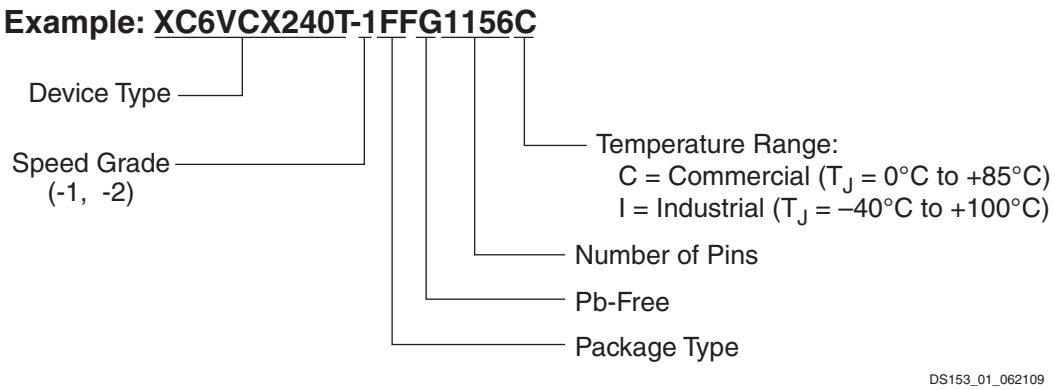

Figure 1: **Virtex-6 CXT FPGA Ordering Information**

Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

Virtex-6 FPGA Configuration Guide **(UG360)**

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-6 FPGA SelectIO Resources User Guide **(UG361)**

This guide describes the SelectIO™ resources available in all the Virtex-6 CXT devices.

Virtex-6 FPGA Clocking Resources User Guide **(UG362)**

This guide describes the clocking resources available in all the Virtex-6 CXT devices, including the MMCM and clock buffers.

Virtex-6 FPGA Memory Resources User Guide **(UG363)**

This guide describes the Virtex-6 CXT device block RAM and FIFO capabilities.

Virtex-6 FPGA CLB User Guide **(UG364)**

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 CXT devices.

Virtex-6 FPGA DSP48E1 Slice User Guide **(UG369)**

This guide describes the architecture of the DSP48E1 slice in Virtex-6 CXT FPGAs and provides configuration examples.

Virtex-6 FPGA GTX Transceivers User Guide **(UG366)**

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide **(UG368)**

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Data Sheet: DC and Switching Characteristics **(DS152)**

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

Virtex-6 FPGA Packaging and Pinout Specifications **(UG365)**

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 CXT FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

Table 3: **Virtex-6 CXT FPGA Bitstream Length**

Device	Total Number of Configuration Bits
XC6VCX75T	26,239,328
XC6VCX130T	43,719,776
XC6VCX195T	61,552,736
XC6VCX240T	73,859,552

Table 4: **Virtex-6 CXT FPGA Device ID Codes**

Device	ID Code (Hex)
XC6VCX75T	0x042C4093
XC6VCX130T	0x042CA093
XC6VCX195T	0x042CC093
XC6VCX240T	0x042D0093

CLB Overview for CXT Devices

Table 5, updated specifically for the CXT family from a similar table in the *Virtex-6 FPGA CLB User Guide*, shows the available resources in all Virtex-6 CXT FPGA CLBs.

Table 5: **Virtex-6 CXT FPGA Logic Resources Available in All CLBs**

Device	Total Slices	SLICELs	SLICEMs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Register (Kb)	Number of Flip-Flops
XC6VCX75T	11,640	7,460	4,180	46,560	1045	522.5	93,120
XC6VCX130T	20,000	13,040	6,960	80,000	1740	870	160,000
XC6VCX195T	31,200	19,040	12,160	124,800	3140	1570	249,600
XC6VCX240T	37,680	23,080	14,600	150,720	3770	1885	301,440

Regional Clock Management for CXT Devices

Table 6, updated from the *Virtex-6 FPGA Clocking Resources User Guide* specifically for the CXT family, shows the number of clock regions in all Virtex-6 CXT FPGA CLBs.

Table 6: **Virtex-6 CXT FPGA Clock Regions**

Device	Number of Clock Regions
XC6VCX75T	6
XC6VCX130T	10
XC6VCX195T	10
XC6VCX240T	12

CXT Packaging Specifications

Table 7, updated from the *Virtex-6 FPGA Packaging and Pinout Specifications* specifically for the CXT family, shows the number of GTX transceiver I/O channels. Table 8 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination.

Table 7: **Number of Serial Transceivers (GTs) I/O Channels/Device**

I/O Channels	Device			
	CX75T(1)	CX130T(2)	CX195T(3)	CX240T(4)
MGTRXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTRXN	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXN	8 or 12	8, 12, or 16	12 or 16	12 or 16

Notes:

1. The XC6VCX75T has 8 GTX I/O channels in the FF484/FFG484 package and 12 GTX I/O channels in the FF784/FFG784 package.
2. The XC6VCX130T has 8 GTX I/O channels in the FF484/FFG484 package, 12 GTX I/O channels in the FF784/FFG784 package, and 16 GTX I/O channels in the FF1156/FFG1156 package.
3. The XC6VCX195T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.
4. The XC6VCX240T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.

Table 8: **Available I/O Pin/Device/Package Combinations**

Virtex-6 CXT Device	User I/O Pins	Virtex-6 CXT FPGA Package		
		FF484	FF784	FF1156
XC6VCX75T	Available User I/Os	240	360	–
	Differential I/O Pairs	120	180	–
XC6VCX130T	Available User I/Os	240	400	600
	Differential I/O Pairs	120	200	300
XC6VCX195T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300
XC6VCX240T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300

GTX Transceivers in CXT Devices

CXT devices have between 8 to 16 gigabit transceiver circuits. Each GTX transceiver is a combined transmitter and receiver capable of operating at a data rate between 480 Mb/s and 3.75 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The transmitter and receiver are independent circuits that use separate PLLs to multiply the reference frequency input by certain programmable numbers between 2 and 25, to become the bit-serial data clock. Each GTX transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

Note: Unbonded locations in the FF484 package are:

- CX75T: X0Y8, X0Y9, X0Y10, X0Y11
- CX130T: X0Y0, X0Y1, X0Y2, X0Y3, and X0Y12, X0Y13, X0Y14, X0Y15

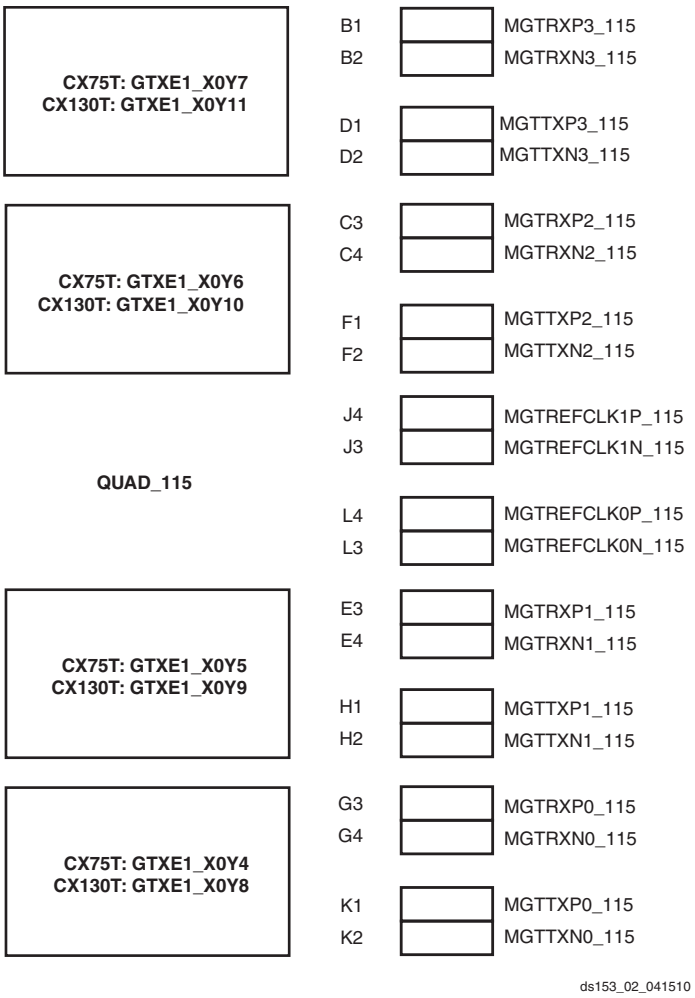

Figure 2: **Placement Diagram for the FF484 Package (1 of 2)**

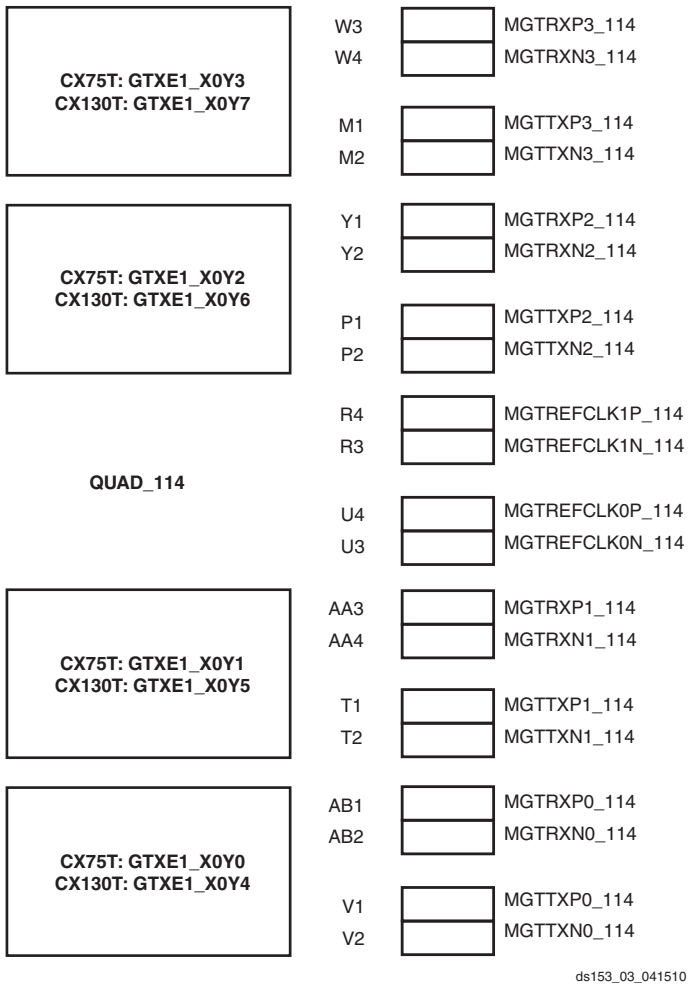

Figure 3: **Placement Diagram for the FF484 Package (2 of 2)**

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

Note: Unbonded locations in the FF784 package are:

- CX130T: X0Y0, X0Y1, X0Y2, X0Y3
- CX195T: X0Y0, X0Y1, X0Y2, X0Y3
- CX240T: X0Y0, X0Y1, X0Y2, X0Y3

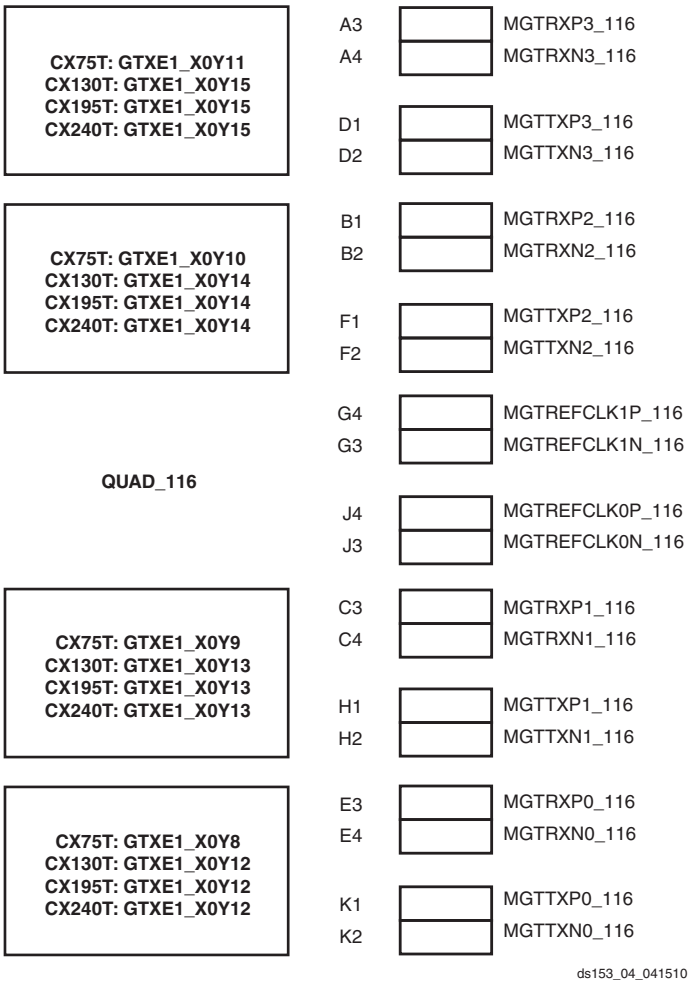

Figure 4: **Placement Diagram for the FF784 Package (1 of 3)**

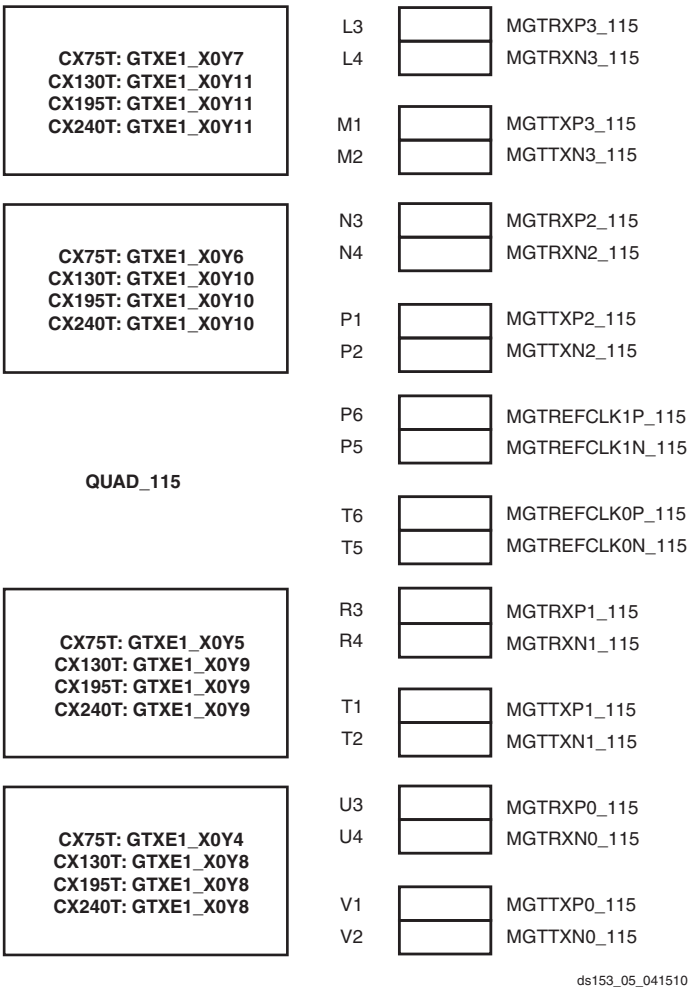

Figure 5: **Placement Diagram for the FF784 Package (2 of 3)**

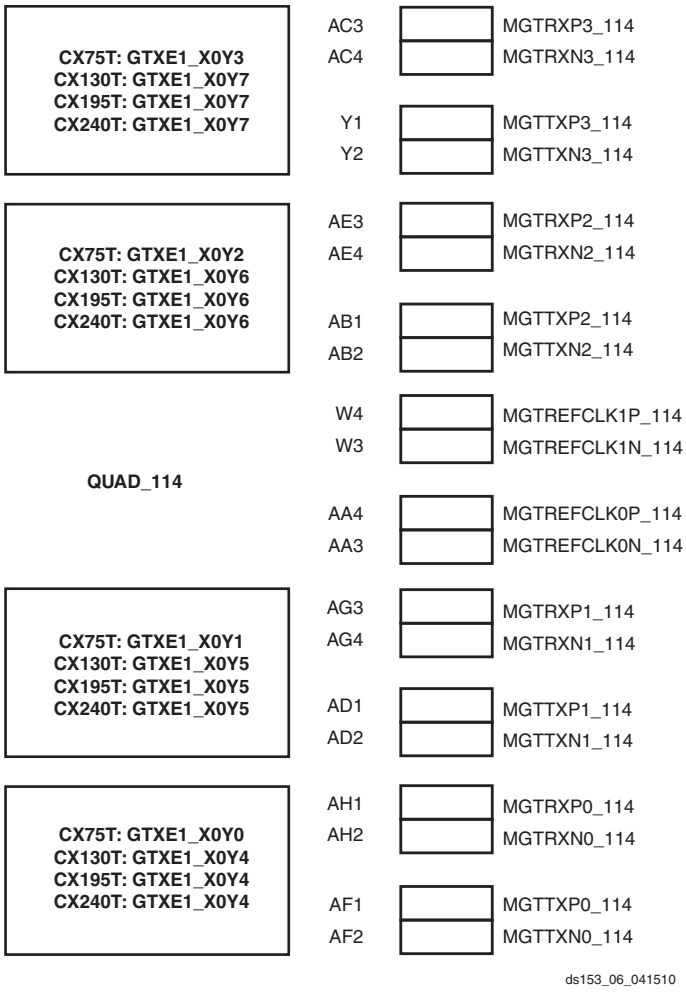

Figure 6: **Placement Diagram for the FF784 Package (3 of 3)**

FF1156 Package Placement Diagrams

Figure 7 through Figure 10 show the placement diagrams for the GTX transceivers in the FF1156 package.

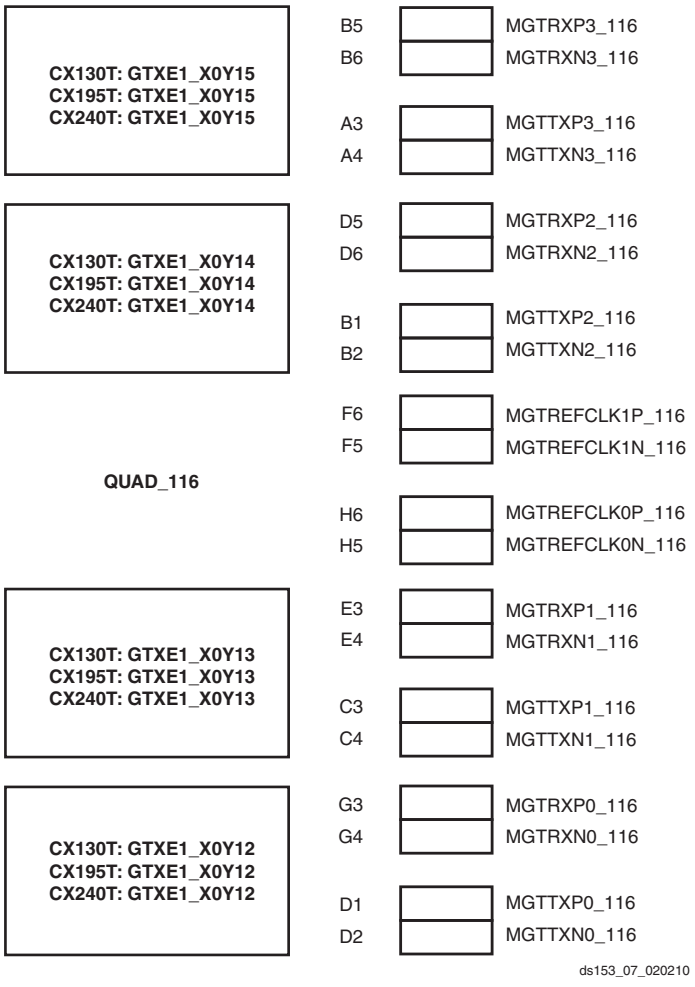

Figure 7: **Placement Diagram for the FF1156 Package (1 of 4)**

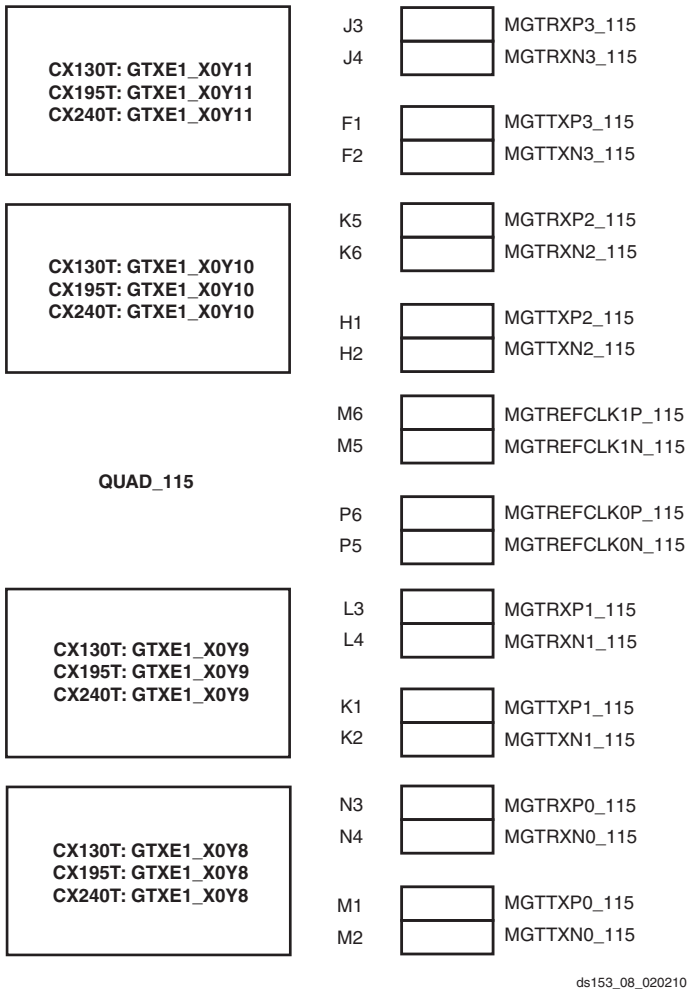

Figure 8: **Placement Diagram for the FF1156 Package (2 of 4)**

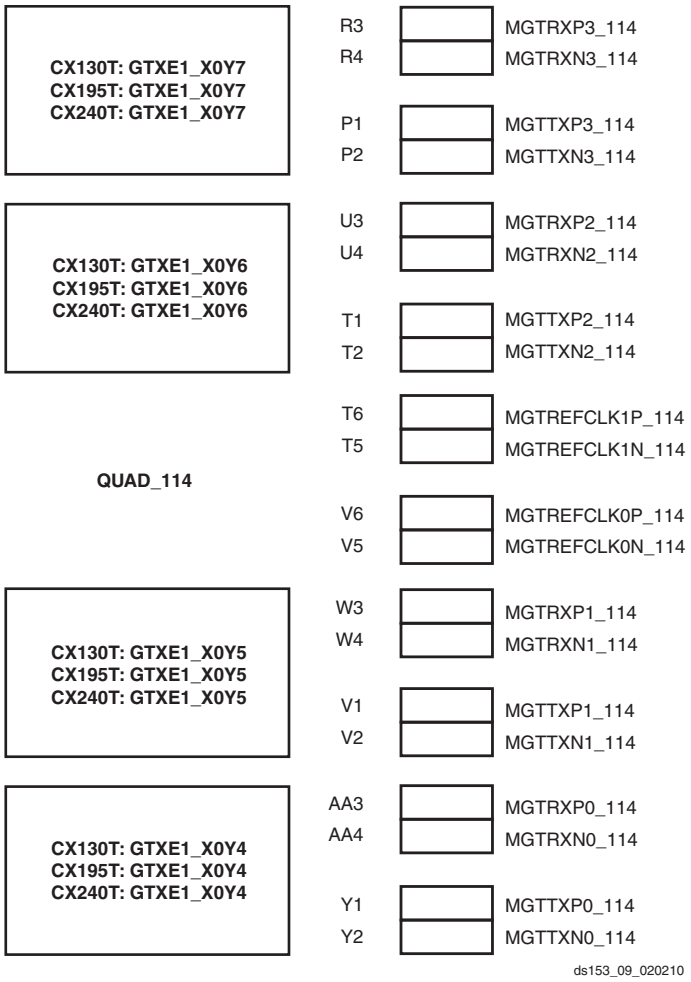

Figure 9: **Placement Diagram for the FF1156 Package (3 of 4)**

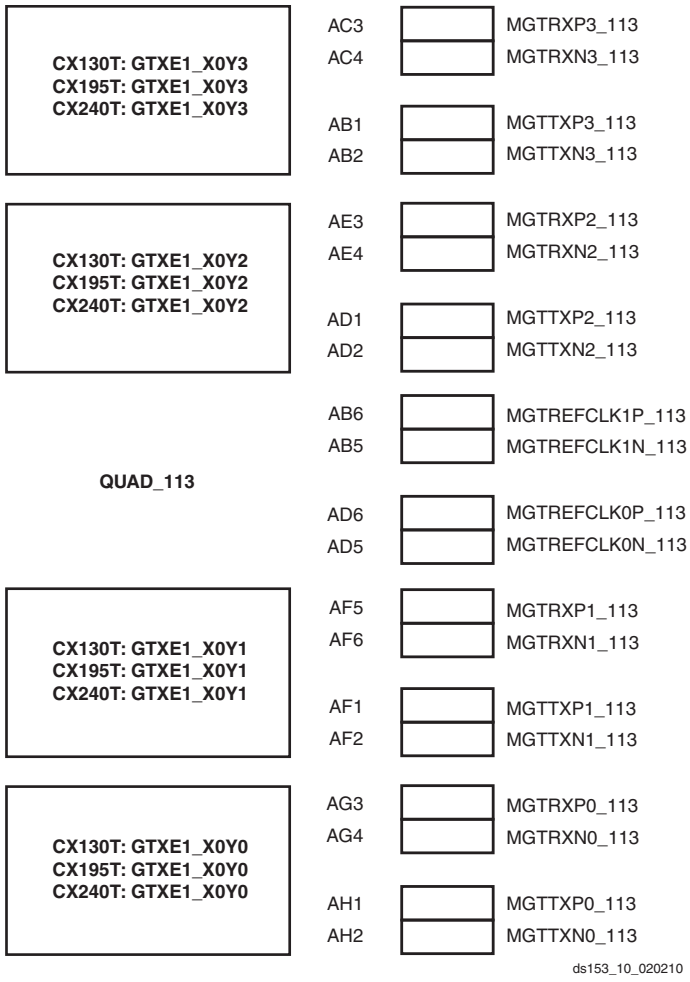

Figure 10: **Placement Diagram for the FF1156 Package (4 of 4)**

Virtex-6 CXT FPGA Electrical Characteristics Introduction

Virtex-6 CXT FPGAs are available in -2 and -1 speed grades, with -2 having the highest performance. Virtex-6 CXT FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

All specifications are subject to change without notice.

Virtex-6 CXT FPGA DC Characteristics

Table 9: **Absolute Maximum Ratings(1)**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{FS}	External voltage supply for eFUSE programming(2)	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.5 to 3.0	V
V_{IN}(3)	2.5V or below I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 2.5V or below output(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(5)	+220	°C
T_j	Maximum junction temperature(5)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When not programming eFUSE, connect V_{FS} to GND.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to the *Virtex-6 FPGA SelectIO Resources User Guide*.
5. For soldering guidelines and thermal considerations, see *Virtex-6 FPGA Packaging and Pinout Specification*.

Table 10: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	0.95	1.05	V
	Internal supply voltage relative to GND, T_j = –40°C to +100°C	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_j = 0°C to +85°C	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_j = –40°C to +100°C	2.375	2.625	V
V_{CCO}(1)(2)(3)	Supply voltage relative to GND, T_j = 0°C to +85°C	1.14	2.625	V
	Supply voltage relative to GND, T_j = –40°C to +100°C	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	2.625	V
	2.5V supply voltage relative to GND, T_j = –40°C to +100°C	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_j = –40°C to +100°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(4)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}(5)	Battery voltage relative to GND, T_j = 0°C to +85°C	1.0	2.5	V
	Battery voltage relative to GND, T_j = –40°C to +100°C	1.0	2.5	V
V_{FS}(6)	External voltage supply for eFUSE programming	2.375	2.625	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
4. A total of 100 mA per bank should not be exceeded.
5. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
6. When not programming eFUSE, connect V_{FS} to GND.
7. All voltages are relative to ground.

Table 11: **DC Characteristics Over Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	µA
C_{IN}(3)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	20	–	80	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	8	–	40	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	5	–	30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	1	–	20	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V	3	–	80	µA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Quiescent Supply Current: Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 CXT devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 12.

Table 12: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade		Units
			-2 (C & I)	-1 (C & I)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VCX75T	927	927	mA
		XC6VCX130T	1563	1563	mA
		XC6VCX195T	2059	2059	mA
		XC6VCX240T	2478	2478	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VCX75T	1	1	mA
		XC6VCX130T	1	1	mA
		XC6VCX195T	1	1	mA
		XC6VCX240T	2	2	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VCX75T	45	45	mA
		XC6VCX130T	75	75	mA
		XC6VCX195T	113	113	mA
		XC6VCX240T	135	135	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (Tj). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 CXT devices require a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO}. V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX} or if powered by the same supply, V_{CCAUX} and V_{CCO} power-down simultaneously.

Table 13 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 CXT devices for proper power-on and configuration. If the current minimums shown in Table 12 and Table 13 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 13: **Power-On Current for Virtex-6 CXT Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VCX75T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VCX130T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VCX195T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VCX240T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 14: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

HT DC Specifications (HT_25)

Table 16: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 17: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 18: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 22: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 23: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: **GTX Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 25 summarizes the DC output specifications of the GTX transceivers in Virtex-6 CXT FPGAs. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 25: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	125	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

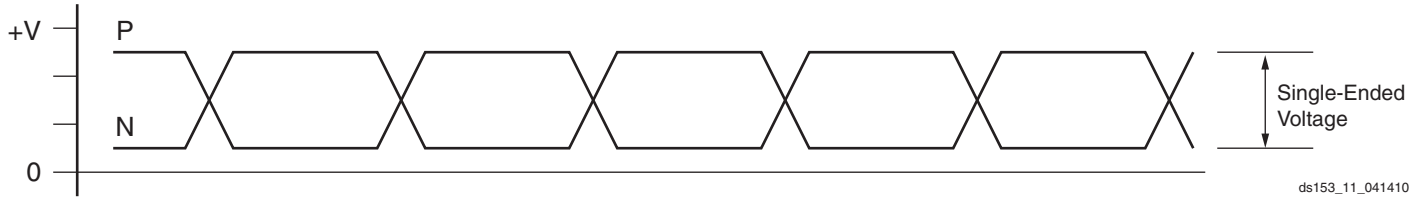

Figure 11: **Single-Ended Peak-to-Peak Voltage**

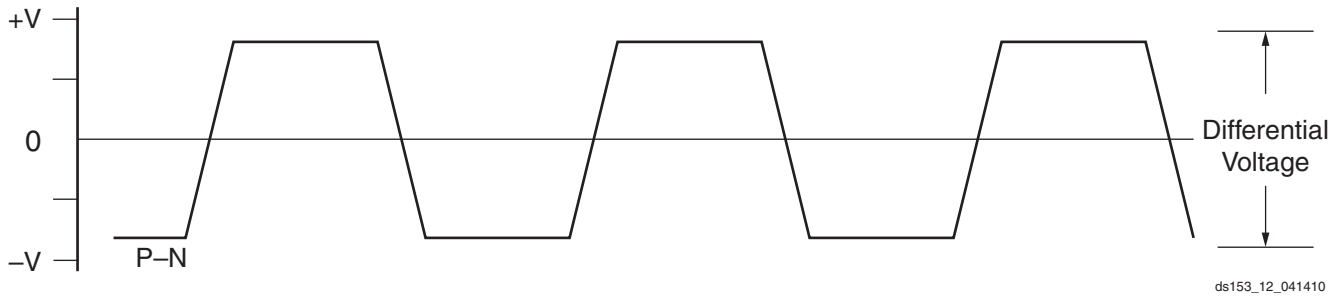

Figure 12: **Differential Peak-to-Peak Voltage**

Table 26 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 26: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 27: **GTX Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.75	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.5	2.5	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	GHz

Table 28: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 29: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5	–	375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

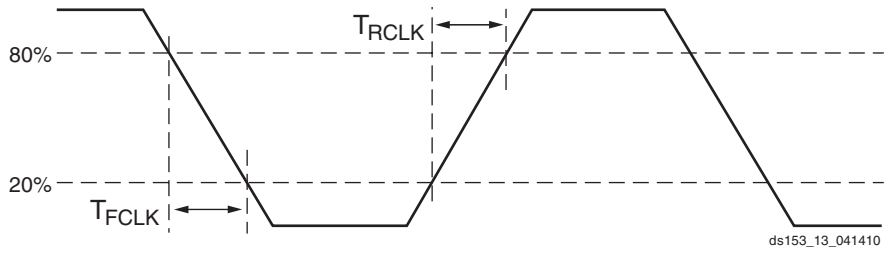

Figure 13: **Reference Clock Timing Parameters**

Table 30: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T_{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T_{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$D_{J3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$T_{J3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$D_{J3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
T_{J600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
D_{J600}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Table 31: **GTX Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
T_{J480}	Total Jitter(2)(3)	480 Mb/s	–	–	0.1	UI
D_{J480}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTX transceiver sites.
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 32: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
$T_{RXELECIDLE}$	TIme for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled	–200	–	200	ppm
		CDR 2nd-order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance(2)						
$JT_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s	0.45	–	–	UI
$JT_SJ_{3.125L}$	Sinusoidal Jitter(3)	3.125 Gb/s(4)	0.45	–	–	UI
$JT_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(5)	0.5	–	–	UI
$JT_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(6)	0.5	–	–	UI
JT_SJ_{675}	Sinusoidal Jitter(3)	675 Mb/s	0.4	–	–	UI
JT_SJ_{480}	Sinusoidal Jitter(3)	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT_TJSE_{3.125}$	Total Jitter with Stressed Eye(7)	3.125 Gb/s	0.70	–	–	UI
$JT_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye(7)	3.125 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a bit-error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.
7. Composite jitter with RX equalizer enabled. DFE disabled.

Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 33: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 34: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	125	125	MHz
$F_{USERCLK}$	User clock maximum frequency	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	MHz

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 CXT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 25.

Table 35: **Interface Performances**

Description	Speed Grade	
	-2	-1
Networking Applications		
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	650 Mb/s	625 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.25 Gb/s	1.0 Gb/s
SDR LVDS receiver (SFI-4.1)(1)	650 Mb/s	625 Mb/s
DDR LVDS receiver (SFI-4.2)(1)	1.0 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces(2)(3)		
DDR2	666 Mb/s	666 Mb/s
DDR3	800 Mb/s	666 Mb/s
QDR II + SRAM	250 MHz	250 MHz

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Based on Xilinx memory characterization platforms designed according to the guidelines in the *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult the *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).

Switching Characteristics

All values represented in this data sheet are based on the speed specification (version 1.08). Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 36 correlates the current status of each Virtex-6 CXT device on a per speed grade basis.

Table 36: **Virtex-6 CXT Device/Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VCX75T			-2, -1
XC6VCX130T			-2, -1
XC6VCX195T			-2, -1
XC6VCX240T			-2, -1

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 CXT devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 37 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 37: **Virtex-6 CXT Device/Production Software and Speed Specification Release**

Device	Speed Grade Designations	
	-2	-1
XC6VCX75T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX130T	ISE 12.1 v1.04	
XC6VCX195T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX240T	ISE 12.1 v1.04	

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 38 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 39 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 38: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVDS_25	1.09	1.09	1.68	1.68	1.68	1.68	ns
LVDSEXT_25	1.09	1.09	1.84	1.84	1.84	1.84	ns
HT_25	1.09	1.09	1.78	1.78	1.78	1.78	ns
BLVDS_25	1.09	1.09	1.67	1.67	1.67	1.67	ns
RSDS_25 (point to point)	1.09	1.09	1.68	1.68	1.68	1.68	ns
HSTL_I	1.06	1.06	1.73	1.73	1.73	1.73	ns
HSTL_II	1.06	1.06	1.74	1.74	1.74	1.74	ns
HSTL_III	1.06	1.06	1.71	1.71	1.71	1.71	ns
HSTL_I_18	1.06	1.06	1.75	1.75	1.75	1.75	ns
HSTL_II_18	1.06	1.06	1.81	1.81	1.81	1.81	ns
HSTL_III_18	1.06	1.06	1.71	1.71	1.71	1.71	ns
SSTL2_I	1.06	1.06	1.77	1.77	1.77	1.77	ns
SSTL2_II	1.06	1.06	1.72	1.72	1.72	1.72	ns
SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
LVCMOS25, Slow, 2 mA	0.66	0.66	6.01	6.01	6.01	6.01	ns
LVCMOS25, Slow, 4 mA	0.66	0.66	3.79	3.79	3.79	3.79	ns
LVCMOS25, Slow, 6 mA	0.66	0.66	3.08	3.08	3.08	3.08	ns
LVCMOS25, Slow, 8 mA	0.66	0.66	2.72	2.72	2.72	2.72	ns
LVCMOS25, Slow, 12 mA	0.66	0.66	2.17	2.17	2.17	2.17	ns
LVCMOS25, Slow, 16 mA	0.66	0.66	2.29	2.29	2.29	2.29	ns
LVCMOS25, Slow, 24 mA	0.66	0.66	2.02	2.02	2.02	2.02	ns
LVCMOS25, Fast, 2 mA	0.66	0.66	6.04	6.04	6.04	6.04	ns
LVCMOS25, Fast, 4 mA	0.66	0.66	3.82	3.82	3.82	3.82	ns
LVCMOS25, Fast, 6 mA	0.66	0.66	2.99	2.99	2.99	2.99	ns
LVCMOS25, Fast, 8 mA	0.66	0.66	2.65	2.65	2.65	2.65	ns
LVCMOS25, Fast, 12 mA	0.66	0.66	2.08	2.08	2.08	2.08	ns
LVCMOS25, Fast, 16 mA	0.66	0.66	2.13	2.13	2.13	2.13	ns
LVCMOS25, Fast, 24 mA	0.66	0.66	1.99	1.99	1.99	1.99	ns

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVCMOS18, Slow, 2 mA	0.71	0.71	4.87	4.87	4.87	4.87	ns
LVCMOS18, Slow, 4 mA	0.71	0.71	3.21	3.21	3.21	3.21	ns
LVCMOS18, Slow, 6 mA	0.71	0.71	2.64	2.64	2.64	2.64	ns
LVCMOS18, Slow, 8 mA	0.71	0.71	2.27	2.27	2.27	2.27	ns
LVCMOS18, Slow, 12 mA	0.71	0.71	2.15	2.15	2.15	2.15	ns
LVCMOS18, Slow, 16 mA	0.71	0.71	2.11	2.11	2.11	2.11	ns
LVCMOS18, Fast, 2 mA	0.71	0.71	4.57	4.57	4.57	4.57	ns
LVCMOS18, Fast, 4 mA	0.71	0.71	2.97	2.97	2.97	2.97	ns
LVCMOS18, Fast, 6 mA	0.71	0.71	2.46	2.46	2.46	2.46	ns
LVCMOS18, Fast, 8 mA	0.71	0.71	2.13	2.13	2.13	2.13	ns
LVCMOS18, Fast, 12 mA	0.71	0.71	1.97	1.97	1.97	1.97	ns
LVCMOS18, Fast, 16 mA	0.71	0.71	1.91	1.91	1.91	1.91	ns
LVCMOS15, Slow, 2 mA	0.85	0.85	4.29	4.29	4.29	4.29	ns
LVCMOS15, Slow, 4 mA	0.85	0.85	3.10	3.10	3.10	3.10	ns
LVCMOS15, Slow, 6 mA	0.85	0.85	2.68	2.68	2.68	2.68	ns
LVCMOS15, Slow, 8 mA	0.85	0.85	2.23	2.23	2.23	2.23	ns
LVCMOS15, Slow, 12 mA	0.85	0.85	2.13	2.13	2.13	2.13	ns
LVCMOS15, Slow, 16 mA	0.85	0.85	2.04	2.04	2.04	2.04	ns
LVCMOS15, Fast, 2 mA	0.85	0.85	4.28	4.28	4.28	4.28	ns
LVCMOS15, Fast, 4 mA	0.85	0.85	2.78	2.78	2.78	2.78	ns
LVCMOS15, Fast, 6 mA	0.85	0.85	2.42	2.42	2.42	2.42	ns
LVCMOS15, Fast, 8 mA	0.85	0.85	2.11	2.11	2.11	2.11	ns
LVCMOS15, Fast, 12 mA	0.85	0.85	1.97	1.97	1.97	1.97	ns
LVCMOS15, Fast, 16 mA	0.85	0.85	1.96	1.96	1.96	1.96	ns
LVCMOS12, Slow, 2 mA	0.93	0.93	3.75	3.75	3.75	3.75	ns
LVCMOS12, Slow, 4 mA	0.93	0.93	2.93	2.93	2.93	2.93	ns
LVCMOS12, Slow, 6 mA	0.93	0.93	2.41	2.41	2.41	2.41	ns
LVCMOS12, Slow, 8 mA	0.93	0.93	2.25	2.25	2.25	2.25	ns
LVCMOS12, Fast, 2 mA	0.93	0.93	3.39	3.39	3.39	3.39	ns
LVCMOS12, Fast, 4 mA	0.93	0.93	2.51	2.51	2.51	2.51	ns
LVCMOS12, Fast, 6 mA	0.93	0.93	2.11	2.11	2.11	2.11	ns
LVCMOS12, Fast, 8 mA	0.93	0.93	2.02	2.02	2.02	2.02	ns
LVDCI_25	0.66	0.66	2.26	2.26	2.26	2.26	ns
LVDCI_18	0.71	0.71	2.47	2.47	2.47	2.47	ns
LVDCI_15	0.85	0.85	2.24	2.24	2.24	2.24	ns
LVDCI_DV2_25	0.66	0.66	2.01	2.01	2.01	2.01	ns
LVDCI_DV2_18	0.71	0.71	2.00	2.00	2.00	2.00	ns
LVDCI_DV2_15	0.85	0.85	1.91	1.91	1.91	1.91	ns

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVPECL_25	1.09	1.09	1.65	1.65	1.65	1.65	ns
HSTL_I_12	1.06	1.06	1.78	1.78	1.78	1.78	ns
HSTL_I_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_II_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_T_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_III_DCI	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_I_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_DCI_18	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_II _T_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_III_DCI_18	1.06	1.06	1.69	1.69	1.69	1.69	ns
DIFF_HSTL_I_18	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_HSTL_I_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_I	1.09	1.09	1.73	1.73	1.73	1.73	ns
DIFF_HSTL_I_DCI	1.09	1.09	1.66	1.66	1.66	1.66	ns
DIFF_HSTL_II_18	1.09	1.09	1.81	1.81	1.81	1.81	ns
DIFF_HSTL_II_DCI_18	1.09	1.09	1.62	1.62	1.62	1.62	ns
DIFF_HSTL_II _T_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_II	1.09	1.09	1.74	1.74	1.74	1.74	ns
DIFF_HSTL_II_DCI	1.09	1.09	1.68	1.68	1.68	1.68	ns
SSTL2_I_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL2_II_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL2_II_T_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL18_I	1.06	1.06	1.75	1.75	1.75	1.75	ns
SSTL18_II	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_I_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_II_DCI	1.06	1.06	1.63	1.63	1.63	1.63	ns
SSTL18_II_T_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL2_I	1.09	1.09	1.77	1.77	1.77	1.77	ns
DIFF_SSTL2_I_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL2_II	1.09	1.09	1.72	1.72	1.72	1.72	ns
DIFF_SSTL2_II_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL2_II_T_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL18_I	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_SSTL18_I_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II_DCI	1.09	1.09	1.63	1.63	1.63	1.63	ns

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
DIFF_SSTL18_II_T_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
DIFF_SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns

Table 39: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{IOTPHZ}	T input to Pad high-impedance	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 40 shows the test setup parameters used for measuring input delay.

Table 40: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 14.
6. The value given is the differential output voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 14 and Figure 15.

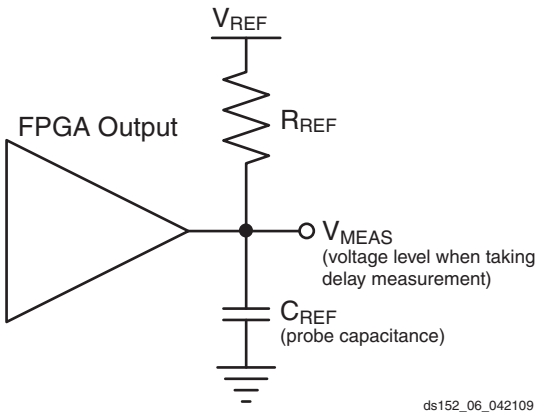

Figure 14: **Single Ended Test Setup**

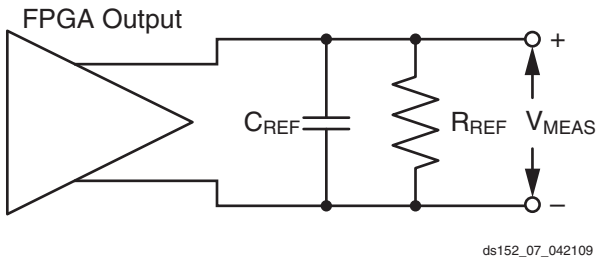

Figure 15: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 41.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 41: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[2]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[2]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0

Table 41: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 42: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.27/0.04	0.27/0.04	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.96/–0.10	0.96/–0.10	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.10/0.54	0.10/0.54	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.14/0.42	0.14/0.40	ns
Combinatorial				
T_{IDI}	D pin to O pin propagation delay, no Delay	0.20	0.20	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.25	0.25	ns
Sequential Delays				
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.64	0.64	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.68	0.68	ns
T_{ICKQ}	CLK to Q outputs	0.71	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	1.15	1.15	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Table 43: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.54/–0.11	0.54/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.71/–0.29	0.71/–0.29	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.56/–0.10	0.56/–0.10	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Combinatorial				
T_{DOQ}	D1 to OQ out or T1 to TQ out	1.01	1.01	ns
Sequential Delays				
T_{OCKQ}	CLK to OQ/TQ out	0.71	0.71	ns
T_{RQ}	SR pin to OQ/TQ out	1.05	1.05	ns
T_{GSRQ}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 44: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold for Control Lines				
$T_{ISCCK_BITSLIP}/T_{ISCKC_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.09/0.17	0.09/0.17	ns
$T_{ISCCK_CE}/T_{ISCKC_CE}$ (2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.27/0.04	0.27/0.04	ns
$T_{ISCCK_CE2}/T_{ISCKC_CE2}$ (2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.06/0.31	–0.06/0.31	ns
Setup/Hold for Data Lines				
T_{ISDCK_D}/T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.09/0.11	0.09/0.11	ns
$T_{ISDCK_DDLY}/T_{ISCKD_DDLY}$	DDLY pin Setup/Hold with respect to CLK (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
$T_{ISDCK_D_DDR}/T_{ISCKD_D_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.09/0.11	0.09/0.11	ns
$T_{ISDCK_DDLY_DDR}$ $T_{ISCKD_DDLY_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
Sequential Delays				
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.75	0.75	ns
Propagation Delays				
T_{ISDO_DO}	D input to DO output pin	0.25	0.25	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCCK_CE}/T_{ISCKC_CE}$ in a TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 45: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.31/–0.12	0.31/–0.12	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.56/–0.08	0.56/–0.08	ns
$T_{OSDCK_T2}/T_{OSCKD_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.31/–0.08	0.31/–0.08	ns
$T_{OSCCK_OCE}/T_{OSCKC_OCE}$	OCE input Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	ns
$T_{OSCCK_TCE}/T_{OSCKC_TCE}$	TCE input Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Sequential Delays				
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.82	0.82	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.82	0.82	ns
Combinatorial				
T_{OSDO_TTQ}	T input to TQ Out	0.97	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the TRACE report.

Input/Output Delay Switching Characteristics

Table 46: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
IDELAYCTRL				
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3	3	µs
$F_{IDELAYCTRL_REF}$	REFCLK frequency	200	200	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	MHz
$T_{IDELAYCTRL_RPW}$	Minimum Reset pulse width	50	50	ns
IODELAY				
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	1/(32 x 2 x F_{REF})		ps
$T_{IDELAYPAT_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(1)	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern.(2)	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern.(3)	±9	±9	ps per tap
$T_{IODELAY_CLK_MAX}$	Maximum frequency of CLK input to IODELAY	300	300	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.65/–0.09	0.65/–0.09	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.31/–0.00	0.31/–0.00	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.69/–0.08	0.69/–0.08	ns
T_{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 4	Note 4	ps
$T_{IODDO_IDATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps
$T_{IODDO_ODATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps

Notes:

1. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
2. When HIGH_PERFORMANCE mode is set to TRUE
3. When HIGH_PERFORMANCE mode is set to FALSE.
4. Delay depends on IODELAY tap setting. See the TRACE report for actual values.

CLB Switching Characteristics

Table 47: **CLB Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays				
T_{ILO}	An – Dn LUT address to A	0.08	0.08	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.23	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.37	0.41	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.79	0.91	ns, Max
T_{AXA}	AX inputs to AMUX output	0.42	0.48	ns, Max
T_{AXB}	AX inputs to BMUX output	0.47	0.53	ns, Max
T_{AXC}	AX inputs to CMUX output	0.52	0.60	ns, Max
T_{AXD}	AX inputs to DMUX output	0.55	0.63	ns, Max

Table 47: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BXB}	BX inputs to BMUX output	0.39	0.45	ns, Max
T_{BXD}	BX inputs to DMUX output	0.50	0.58	ns, Max
T_{CXB}	CX inputs to CMUX output	0.34	0.38	ns, Max
T_{CXD}	CX inputs to DMUX output	0.40	0.45	ns, Max
T_{DXD}	DX inputs to DMUX output	0.38	0.44	ns, Max
T_{OPCYA}	An input to COUT output	0.42	0.47	ns, Max
T_{OPCYB}	Bn input to COUT output	0.42	0.47	ns, Max
T_{OPCYC}	Cn input to COUT output	0.35	0.39	ns, Max
T_{OPCYD}	Dn input to COUT output	0.33	0.37	ns, Max
T_{AXCY}	AX input to COUT output	0.33	0.38	ns, Max
T_{BXCY}	BX input to COUT output	0.28	0.32	ns, Max
T_{CXCY}	CX input to COUT output	0.20	0.23	ns, Max
T_{DXCY}	DX input to COUT output	0.19	0.22	ns, Max
T_{BYP}	CIN input to COUT output	0.08	0.09	ns, Max
T_{CINA}	CIN input to AMUX output	0.28	0.32	ns, Max
T_{CINB}	CIN input to BMUX output	0.29	0.34	ns, Max
T_{CINC}	CIN input to CMUX output	0.30	0.34	ns, Max
T_{CIND}	CIN input to DMUX output	0.33	0.38	ns, Max
Sequential Delays				
T_{CKO}	Clock to AQ – DQ outputs	0.39	0.44	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.54	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK				
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.43/0.20	0.50/0.23	ns, Min
$T_{CECK_CLB}/T_{CKCE_CLB}$	CE input to CLK on A – D Flip Flops	0.32/–0.01	0.37/–0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.52/–0.08	0.60/–0.08	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.24/0.17	0.27/0.19	ns, Min
Set/Reset				
T_{SRMIN}	SR input minimum pulse width	0.97	0.97	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.68	0.78	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.59	0.67	ns, Max
F_{TOG}	Toggle frequency (for export control)	1098.00	1098.00	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 48: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{SHCKO}	Clock to A – B outputs	1.36	1.56	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.71	1.96	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{DS}/T_{DH}	A – D inputs to CLK	0.88/0.22	1.01/0.26	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.27/0.70	0.31/0.80	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.40/–0.01	0.46/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.41/–0.02	0.48/–0.01	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	1.00	1.15	ns, Min
T_{MCP}	Minimum clock period	2.00	2.30	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to the TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 49: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{REG}	Clock to A – D outputs	1.58	1.82	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.93	2.22	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.55	1.78	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{WS}/T_{WH}	WE input	0.09/–0.01	0.10/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.10/–0.02	0.11/–0.01	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.94/0.24	1.08/0.28	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	0.85	0.98	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 50: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Block RAM and FIFO Clock-to-Out Delays				
T_{RCKO_DO} and $T_{RCKO_DO_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	2.08	2.39	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.75	0.86	ns, Max
$T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	3.30	3.79	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.86	0.98	ns, Max
T_{RCKO_CASC} and $T_{RCKO_CASC_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	3.18	3.65	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.58	1.81	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.91	1.05	ns, Max
$T_{RCKO_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	1.09	1.25	ns, Max
$T_{RCKO_RDCOUNT}$	Clock CLK to FIFO Read Counter	1.09	1.25	ns, Max
$T_{RCKO_WRCOUNT}$	Clock CLK to FIFO Write Counter	1.09	1.25	ns, Max
$T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$	Clock CLK to BITERR (with output register)	0.76	0.87	ns, Max
	Clock CLK to BITERR (without output register)	2.84	3.26	ns, Max
$T_{RCKO_PARITY_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	1.06	1.21	ns, Max
$T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.90	1.03	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.92	1.06	ns, Max
Setup and Hold Times Before/After Clock CLK				
$T_{RCCK_ADDR}/T_{RCKC_ADDR}$	ADDR inputs[8]	0.62/0.32	0.72/0.37	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	1.11/0.34	1.28/0.39	ns, Min
$T_{RDCK_DI_ECC}/T_{RCKD_DI_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.59/0.34	0.68/0.39	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.85/0.34	0.97/0.39	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.02/0.34	1.17/0.39	ns, Min
$T_{RCCK_CLK}/T_{RCKC_CLK}$	Inject single/double bit error in ECC mode	1.20/0.29	1.38/0.33	ns, Min
$T_{RCCK_RDEN}/T_{RCKC_RDEN}$	Block RAM Enable (EN) input	0.41/0.30	0.47/0.34	ns, Min
$T_{RCCK_REGCE}/T_{RCKC_REGCE}$	CE input of output register	0.22/0.31	0.25/0.35	ns, Min
$T_{RCCK_RSTREG}/T_{RCKC_RSTREG}$	Synchronous RSTREG input	0.28/0.26	0.32/0.29	ns, Min
$T_{RCCK_RSTRAM}/T_{RCKC_RSTRAM}$	Synchronous RSTRAM input	0.41/0.27	0.47/0.31	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (block RAM only)	0.52/0.35	0.60/0.40	ns, Min
$T_{RCCK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.55/0.30	0.64/0.34	ns, Min
$T_{RCCK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.55/0.30	0.63/0.34	ns, Min
Reset Delays				
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers[10]	1.10	1.27	ns, Max
$T_{RCCK_RSTREG}/T_{RCKC_RSTREG}$	FIFO reset timing[11]	0.28/0.26	0.32/0.29	ns, Min

Table 50: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Maximum Frequency				
F_{MAX}	Block RAM (Write First and No Change modes)	400	350	MHz
	Block RAM (Read First mode)	400	347	MHz
	Block RAM (SDP mode)(12)	400	347	MHz
$F_{MAX_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	400	347	MHz
	Block RAM Cascade (Read First mode)	350	304	MHz
F_{MAX_FIFO}	FIFO in all modes	400	350	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	325	282	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDARRDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

DSP48E1 Switching Characteristics

Table 51: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock				
$T_{DSPDCK_\{A, ACIN; B, BCIN\}_\{AREG; BREG\}}$/ $T_{DSPCKD_\{A, ACIN; B, BCIN\}_\{AREG; BREG\}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.35/0.34	0.41/0.39	ns
$T_{DSPDCK_C_CREG}$/$T_{DSPCKD_C_CREG}$	C input to C register CLK	0.22/0.24	0.26/0.27	ns
$T_{DSPDCK_D_DREG}$/$T_{DSPCKD_D_DREG}$	D input to D register CLK	0.15/0.39	0.17/0.44	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock				
$T_{DSPDCK_\{A, ACIN, B, BCIN\}_PREG_MULT}$/ $T_{DSPCKD_\{A, ACIN, B, BCIN\}_PREG_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	3.21/0.02	3.69/0.02	ns
$T_{DSPDCK_\{A, D\}_ADREG}$/ $T_{DSPCKD–\{A, D\}_ADREG}$	{A, D} input to AD register CLK	1.69/0.13	1.94/0.15	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock				
$T_{DSPDCK_\{A, ACIN, B, BCIN\}_PREG_MULT}$/ $T_{DSPCKD_\{A, ACIN, B, BCIN\}_PREG_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	5.20/–0.19	5.97/–0.22	ns
$T_{DSPDCK_D_DREG_MULT}$/ $T_{DSPCKD_D_DREG_MULT}$	D input to P register CLK	4.90/–0.65	5.63/–0.75	ns
$T_{DSPDCK_\{A, ACIN, B, BCIN\}_PREG}$/ $T_{DSPCKD_\{A, ACIN, B, BCIN\}_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	2.15/–0.19	2.47/–0.22	ns
$T_{DSPDCK_C_PREG}$/ $T_{DSPCKD_C_PREG}$	C input to P register CLK	1.91/–0.14	2.19/–0.17	ns
$T_{DSPDCK_\{PCIN, CARRYCASCIN, MULTSIGNIN\}_PREG}$/ $T_{DSPCKD_\{PCIN, CARRYCASCIN, MULTSIGNIN\}_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.67/–0.04	1.92/–0.05	ns
Setup and Hold Times of the CE Pins				
$T_{DSPDCK_\{CEA; CEB\}_\{AREG; BREG\}}$/ $T_{DSPCKD_\{CEA; CEB\}_\{AREG; BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.22/0.25	0.25/0.29	ns
$T_{DSPDCK_CEC_CREG}$/ $T_{DSPCKD_CEC_CREG}$	CEC input to C register CLK	0.24/0.23	0.28/0.27	ns
$T_{DSPDCK_CED_DREG}$/ $T_{DSPCKD_CED_DREG}$	CED input to D register CLK	0.31/0.14	0.35/0.16	ns
$T_{DSPDCK_CEM_MREG}$/ $T_{DSPCKD_CEM_MREG}$	CEM input to M register CLK	0.26/0.25	0.30/0.28	ns
$T_{DSPDCK_CEP_PREG}$/ $T_{DSPCKD_CEP_PREG}$	CEP input to P register CLK	0.46/0.03	0.53/0.03	ns
Setup and Hold Times of the RST Pins				
$T_{DSPDCK_\{RSTA; RSTB\}_\{AREG; BREG\}}$/ $T_{DSPCKD_\{RSTA; RSTB\}_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.38/0.22	0.43/0.25	ns
$T_{DSPDCK_RSTC_CREG}$/ $T_{DSPCKD_RSTC_CREG}$	RSTC input to C register CLK	0.23/0.09	0.27/0.11	ns
$T_{DSPDCK_RSTD_DREG}$/ $T_{DSPCKD_RSTD_DREG}$	RSTD input to D register CLK	0.38/0.19	0.44/0.21	ns
$T_{DSPDCK_RSTM_MREG}$/ $T_{DSPCKD_RSTM_MREG}$	RSTM input to M register CLK	0.26/0.30	0.30/0.35	ns
$T_{DSPDCK_RSTP_PREG}$/ $T_{DSPCKD_RSTP_PREG}$	RSTP input to P register CLK	0.33/0.05	0.41/0.06	ns
Combinatorial Delays from Input Pins to Output Pins				
$T_{DSPDO_\{A, B\}_\{P, CARRYOUT\}_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	5.08	5.84	ns
$T_{DSPDO_D_\{P, CARRYOUT\}_MULT}$	D input to {P, CARRYOUT} output using multiplier	4.82	5.54	ns
$T_{DSPDO_\{A, B\}_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	2.07	2.38	ns
$T_{DSPDO_\{C, CARRYIN\}_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.83	2.10	ns

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays from Input Pins to Cascading Output Pins				
$T_{DSPDO_\{A; B\}_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.65	0.75	ns
$T_{DSPDO_\{A, B\}_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.24	6.03	ns
$T_{DSPDO_D_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.94	5.68	ns
$T_{DSPDO_\{A, B\}_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.19	2.52	ns
$T_{DSPDO__\{C, CARRYIN\}_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.95	2.25	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins				
$T_{DSPDO_\{ACIN, BCIN\}_\{P, CARRYOUT\}_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	4.97	5.72	ns
$T_{DSPDO_\{ACIN, BCIN\}_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.92	2.21	ns
$T_{DSPDO_\{ACIN; BCIN\}_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.49	0.57	ns
$T_{DSPDO_\{ACIN, BCIN\}_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.10	5.86	ns
$T_{DSPDO_\{ACIN, BCIN\}_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.05	2.35	ns
$T_{DSPDO_\{PCIN, CARRYCASCIN, MULTSIGNIN\}_ \{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.60	1.83	ns
$T_{DSPDO_\{PCIN, CARRYCASCIN, MULTSIGNIN\}_ \{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.72	1.98	ns
Clock to Outs from Output Register Clock to Output Pins				
$T_{DSPCKO_\{P, CARRYOUT\}_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.50	0.57	ns
$T_{DSPCKO_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.66	ns
Clock to Outs from Pipeline Register Clock to Output Pins				
$T_{DSPCKO_\{P, CARRYOUT\}_MREG}$	CLK (MREG) to {P, CARRYOUT} output	2.30	2.65	ns
$T_{DSPCKO_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.43	2.79	ns
$T_{DSPCKO_\{P, CARRYOUT\}_ADREG_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	3.72	4.72	ns
$T_{DSPCKO_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}_ADREG_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	3.84	4.42	ns
Clock to Outs from Input Register Clock to Output Pins				
$T_{DSPCKO_\{P, CARRYOUT\}_\{AREG, BREG\}_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	5.36	6.16	ns
$T_{DSPCKO_\{P, CARRYOUT\}_\{AREG, BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.27	2.61	ns
$T_{DSPCKO_\{P, CARRYOUT\}_CREG}$	CLK (CREG) to {P, CARRYOUT} output	2.27	2.61	ns
$T_{DSPCKO_\{P, CARRYOUT\}_DREG_MULT}$	CLK (DREG) to {P, CARRYOUT} output	5.25	6.04	ns

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins				
$T_{DSPCKO_\{ACOUT;\ BCOUT\}_\{AREG;\ BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.89	1.02	ns
$T_{DSPCKO_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}_\{AREG,\ BREG\}_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.49	6.31	ns
$T_{DSPCKO_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}_\{AREG,\ BREG\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.40	2.76	ns
$T_{DSPCKO_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}_DREG_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.38	6.18	ns
$T_{DSPCKO_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.40	2.76	ns
Maximum Frequency				
F_{MAX}	With all registers used	350	275	MHz
F_{MAX_PATDET}	With pattern detector	350	275	MHz
$F_{MAX_MULT_NOMREG}$	Two register multiply without MREG	262	227	MHz
$F_{MAX_MULT_NOMREG_PATDET}$	Two register multiply without MREG with pattern detect	241	209	MHz
$F_{MAX_PREADD_MULT_NOADREG}$	Without ADREG	292	253	MHz
$F_{MAX_PREADD_MULT_NOADREG_PATDET}$	Without ADREG with pattern detect	292	253	MHz
$F_{MAX_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	196	170	MHz
$F_{MAX_NOPIPELINEREG_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	184	160	MHz

Configuration Switching Characteristics

Table 52: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Power-up Timing Characteristics				
T_{PL} (1)	Program Latency	3	3	ms, Max
T_{POR} (1)	Power-on-Reset	15/55	15/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	ns, Min
Master/Slave Serial Mode Programming Switching (1)				
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	ns, Max
	DOUT at 1.8V	6	6	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK	55	55	%
F_{MSCCK}	Slave mode external CCLK	100	100	MHz
SelectMAP Mode Programming Switching				
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7	7	ns, Min
T_{SMCO}	CCLK to DATA out in readback at 2.5V	8	8	ns, Max
	CCLK to DATA out in readback at 1.8V	8	8	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK	55	55	%
Boundary-Scan Port Timing Specifications				
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	MHz, Max

Table 52: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
BPI Master Flash Mode Programming Switching				
T_{BPICCO}(2)	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching				
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	ns
T_{SPICCM}	MOSI clock to out at 2.5V	6	6	ns
	MOSI clock to out at 1.8V	6	6	ns
$T_{SPICCFC}$	FCS_B clock to out at 2.5V	6	6	ns
	FCS_B clock to out at 1.8V	6	6	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	µs
CCLK Output (Master Modes)				
T_{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	%, Min/Max
CCLK Input (Slave Modes)				
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK				
F_{DCK}	Maximum frequency for DCLK	200	200	MHz
$T_{MMCMDCK_DADDR}/T_{MMCMCKD_DADDR}$	DADDR Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK_DI}/T_{MMCMCKD_DI}$	DI Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK_DEN}/T_{MMCMCKD_DEN}$	DEN Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK_DWE}/T_{MMCMCKD_DWE}$	DWE Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMCKO_DO}$	CLK to out of DO(3)	3.64	3.64	ns
$T_{MMCMCKO_DRDY}$	CLK to out of DRDY	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in *Virtex-6 FPGA Configuration Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 53: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{BCCCK_CE}/T_{BCCKC_CE}$(1)	CE pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.10	0.10	ns
Maximum Frequency				
F_{MAX}	Global clock tree (BUFG)	700	700	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 54: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	0.18	0.18	ns
Maximum Frequency				
F_{MAX}	I/O clock tree (BUFIO)	710	710	MHz

Table 55: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.83	0.83	ns
Maximum Frequency				
F_{MAX}	Regional clock tree (BUFR)	300	300	MHz

Table 56: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.13	0.13	ns
$T_{BHCCK_CE}/T_{BHCKC_CE}$	CE pin Setup and Hold	0.05/0.05	0.05/0.05	ns
Maximum Frequency				
F_{MAX}	Horizontal clock buffer (BUFH)	700	700	MHz

MMCM Switching Characteristics

Table 57: **MMCM Specification**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{INMAX}	Maximum Input Clock Frequency(1)	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max		
F_{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25/75		%
	Allowable Input Duty Cycle: 50—199 MHz	30/70		%
	Allowable Input Duty Cycle: 200—399 MHz	35/65		%
	Allowable Input Duty Cycle: 400—499 MHz	40/60		%
	Allowable Input Duty Cycle: >500 MHz	45/55		%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(2)	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(2)	4.00	4.00	MHz

Table 57: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(3)	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter(4)	Note 1		
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(5)	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	µs
F_{OUTMAX}	MMCM Maximum Output Frequency	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency(6)(7)	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max		
$RST_{MINPULSE}$	Minimum Reset Pulse Width	1.5	1.5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized(8)	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10.00	10.00	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle		
$T_{MMCMDCK_PSEN}$/ $T_{MMCMCKD_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK_PSINCDEC}$/ $T_{MMCMCKD_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
3. The static offset is measured between any MMCM outputs with identical phase.
4. Values for this parameter are available in the Architecture Wizard.
5. Includes global clock buffer.
6. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
7. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
8. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Virtex-6 CXT Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 58. Values are expressed in nanoseconds unless otherwise noted.

Table 58: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.					
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VCX75T	5.88	5.88	ns
		XC6VCX130T	6.00	6.00	ns
		XC6VCX195T	6.13	6.13	ns
		XC6VCX240T	6.13	6.13	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 59: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VCX75T	2.77	2.77	ns
		XC6VCX130T	2.78	2.78	ns
		XC6VCX195T	2.78	2.78	ns
		XC6VCX240T	2.79	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 60: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VCX75T	2.63	2.63	ns
		XC6VCX130T	2.65	2.65	ns
		XC6VCX195T	2.65	2.65	ns
		XC6VCX240T	2.65	2.65	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 CXT Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

Table 61: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VCX75T	1.75/–0.01	1.75/–0.01	ns
		XC6VCX130T	1.88/–0.11	1.88/–0.11	ns
		XC6VCX195T	1.97/–0.14	1.97/–0.14	ns
		XC6VCX240T	1.97/–0.14	1.97/–0.14	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 62: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VCX75T	1.72/–0.22	1.72/–0.22	ns
		XC6VCX130T	1.81/–0.21	1.81/–0.21	ns
		XC6VCX195T	1.82/–0.20	1.82/–0.20	ns
		XC6VCX240T	1.82/–0.20	1.82/–0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VCX75T	1.86/–0.28	1.86/–0.28	ns
		XC6VCX130T	1.93/–0.28	1.93/–0.28	ns
		XC6VCX195T	1.96/–0.27	1.96/–0.27	ns
		XC6VCX240T	1.96/–0.27	1.96/–0.27	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 CXT FPGA clock transmitter and receiver data-valid windows.

Table 64: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC6VCX75T	0.18	0.18	ns
		XC6VCX130T	0.29	0.29	ns
		XC6VCX195T	0.31	0.31	ns
		XC6VCX240T	0.31	0.31	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All	0.22	0.22	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 65: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VCX75T	FF484		ps
			FF784		ps
		XC6VCX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VCX195T	FF784		ps
			FF1156		ps
		XC6VCX240T	FF784	146	ps
			FF1156	182	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: **Sample Window**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	610	610	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	400	400	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 67: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade		Units
		-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO				
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.33/1.31	–0.33/1.31	ns
Pin-to-Pin Clock-to-Out Using BUFIO				
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	5.19	5.19	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/09	1.0	Initial Xilinx release.
02/05/10	1.1	Removed Figure 11: Placement Diagram for the FF1156 Package (5 of 5) from page 11 as there are only 16 GTX transceivers in the FF1156 package. Corrected the placement diagrams in Figure 2 through Figure 10.

Date	Version	Description of Revisions
06/08/10	1.2	Revised GTX Transceivers in CXT Devices, page 5. Added V_{FS} and revised the V_{IN} and V_{TS} values in Table 9, page 11. Added V_{FS} and note 6 to Table 10. Revised description of C_{IN} in Table 11, including adding note 3. Updated Table 13 including adding note 2. Removed DIFF SSTL15 and added values to SSTL15 in Table 15. Updated Table 16 through Table 19. Added eFUSE Read Endurance section. Updated entire GTX Transceivers in CXT Devices section. Changed specifications of PCI Express in Table 34. In Table 35, removed RLDRAM II and revised and added values to other interface performance specifications. Updated speed specification to v1.04 with appropriate changes to Table 36. Revised the IOB switching characteristics in Table 38. Updated values in Table 39 and note 4 in Table 41. ILOGIC (Table 42), OLOGIC (Table 43), ISERDES (Table 44), and OSERDES (Table 45) switching characteristics changes. Revised $T_{IODELAY_CLK_MAX}$ and $T_{IDELAYPAT_JIT}$ in Table 46. Revised CLB switching characteristics and added T_{SHCKO} to Table 47and revised CLB switching characteristics in Table 48 and Table 49. In Table 50, removed $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$, removed $T_{RCKO_PARITY_ECC}$: Clock CLK to ECCPARITY in standard ECC mode, revised $T_{RDCK_DI_ECC}$/$T_{RCKD_DI_ECC}$, $T_{RCKO_POINTERS}$, and revised F_{MAX} and $F_{MAX_CASCADE}$ switching characteristics. Multiple changes to configuration specifications in Table 52. Revised switching characteristics and global clock tree (BUFG) F_{MAX} in Table 53. Revised switching characteristics and I/O clock tree (BUFIO) F_{MAX} in Table 54. Added note 1 to Table 55. Revised the F_{MAX} horizontal clock tree (BUFH) in Table 56. Multiple changes to MMCM specifications in Table 57 including F_{INMAX} and F_{OUTMAX}. Updated switching characteristics in Table 58 through Table 63. Removed T_{DCD_BUFH} and $T_{BUFHSKEW}$ from Table 64.
06/30/10	1.3	Production release of XC6VCX130T and XC6VCX240T in Table 36 and Table 37. Updated -1 speed grade SDR values in Table 35. Updated BUFIO F_{MAX} specification in Table 54. Added Note 6 to Table 57.
07/28/10	1.4	Production release of XC6VCX75T and XC6VCX195T in Table 36 and Table 37 using ISE 12.2 software with speed file v1.06 using the *Speed File Patch*. Updated PCI compliance on page 1. Added values to Table 13. In Table 25, update $V_{CMOUTDC}$ equation to MGTAVTT – DV_{PPOUT}/4. Updated F_{MAX} in Table 53, Table 54, and Table 56. Updated F_{INMAX} and F_{OUTMAX} in Table 57. Updated values in Table 61, Table 62, and Table 63.
10/14/10	1.5	Moved data sheet to Production status on the first page. Updated speed file with ISE 12.3 software with speed file v1.08 using the *Speed File Patch.* In Table 51, updated values for $T_{DSPCKO_\{PCOUT,}$ CARRYCASCOUT, MULTSIGNOUT}_PREG.
02/11/11	1.6	Updated Table 10 to include the industrial range specifications. Added Note 12 to Table 50. Revised T_{BPICCO} values in Table 52. Updated range description for F_{INDUTY} in Table 57 and added note 8. The following revisions are due to specification changes as described in XCN11009, *Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates*. In Table 52, updated the values for T_{SMCCKW}, T_{SPIDCC}, T_{SPICCM}, and $T_{SPICCFC}$. In Table 57: MMCM Specification, added bandwidth settings to F_{PFDMIN} and added note 1.

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