

IR2105

HALF BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Internally set deadtime
- High side output in phase with input
- Match propagation delay for both channels

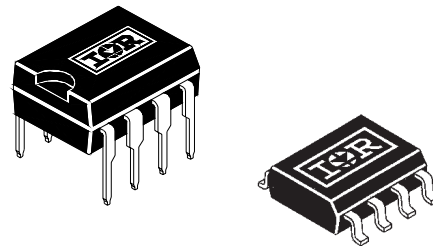
Description

The IR2105 is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

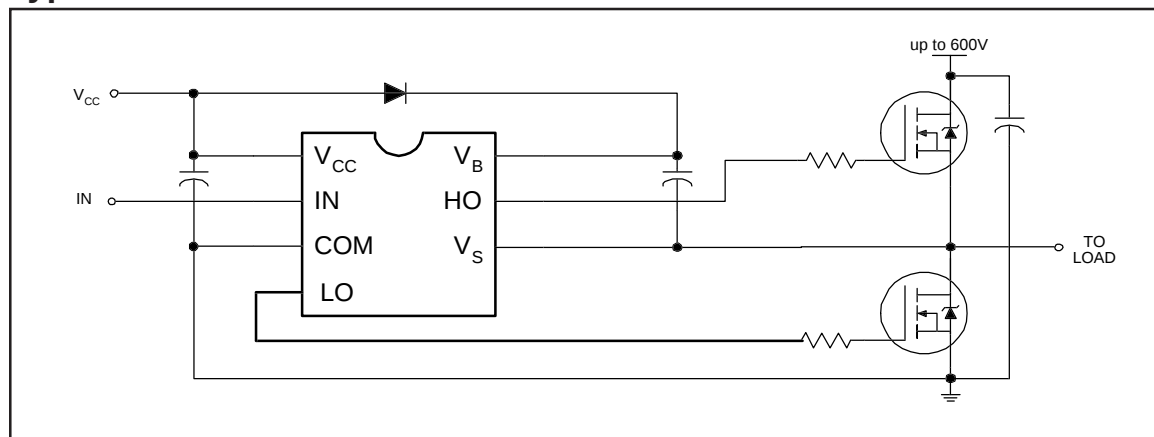
Product Summary

V_{OFFSET}	600V max.
$I_{\text{O+/-}}$	100 mA / 210 mA
V_{OUT}	10 - 20V
$t_{\text{on/off (typ.)}}$	600 & 90 ns
Deadtime (typ.)	500 ns

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V_B	High Side Floating Absolute Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High Side Floating Output Voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage (IN & $\overline{SD}$)	-0.3	$V_{CC} + 0.3$	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R_{thJA}	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	$^\circ\text{C/W}$
	(8 Lead SOIC)	—	200	
T_J	Junction Temperature	—	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V_B	High Side Floating Supply Absolute Voltage	$V_S + 10$	$V_S + 20$	V
V_S	High Side Floating Supply Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage (IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
t_{on}	Turn-On Propagation Delay	—	600	720	ns	$V_S = 0V$
t_{off}	Turn-Off Propagation Delay	—	90	200		$V_S = 600V$
t_r	Turn-On Rise Time	—	100	150		
t_f	Turn-Off Fall Time	—	50	80		
DT	Deadtime, LS Turn-Off to HS Turn-On & HS Turn-On to LS Turn-Off	—	500	750		
MT	Delay Matching, HS & LS Turn-On/Off	—	30	—		

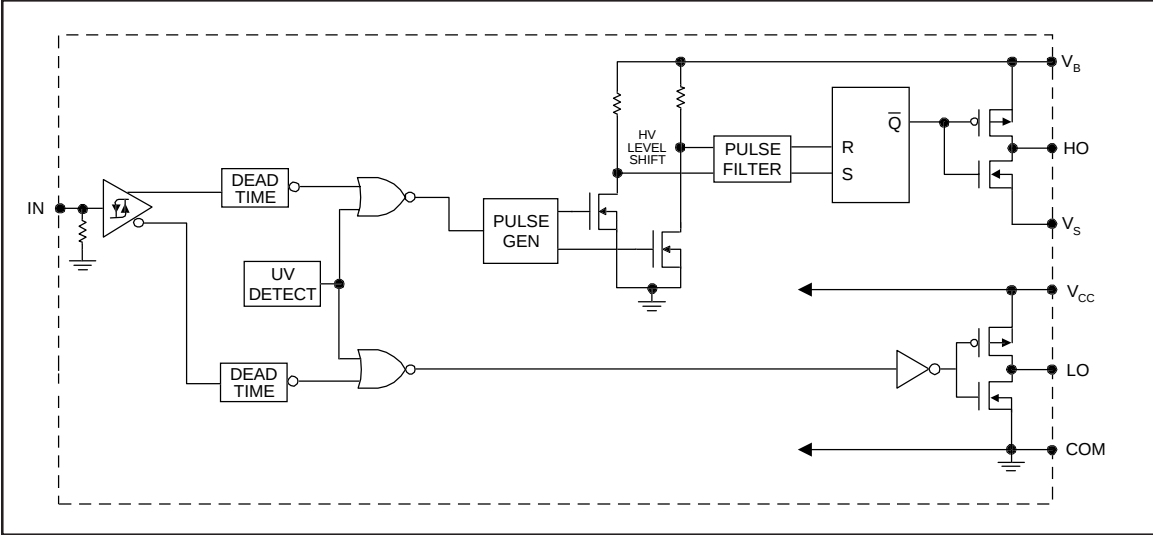
Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
V_{IH}	Logic "1" Input Voltage for HO & Logic "0" for LO	2.7	—	—	V	$V_{CC} = 10V$ to $20V$
V_{IL}	Logic "0" Input Voltage for HO & Logic "1" for LO	—	—	0.8		$V_{CC} = 10V$ to $20V$
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	—	—	100		$I_O = 0A$
I_{LK}	Offset Supply Leakage Current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} Supply Current	—	20	50		$V_{IN} = 0V$ or $5V$
I_{QCC}	Quiescent V_{CC} Supply Current	—	140	240		$V_{IN} = 0V$ or $5V$
I_{IN+}	Logic "1" Input Bias Current	—	25	—		$V_{IN} = 5V$
I_{IN-}	Logic "0" Input Bias Current	—	—	1.0		$V_{IN} = 0V$
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.3	8.9	9.5	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.5	8.2	8.6		
I_{O+}	Output High Short Circuit Pulsed Current	100	125	—	mA	$V_O = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	210	250	—		$V_O = 15V$ $PW \leq 10 \mu s$

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Functional Block Diagram



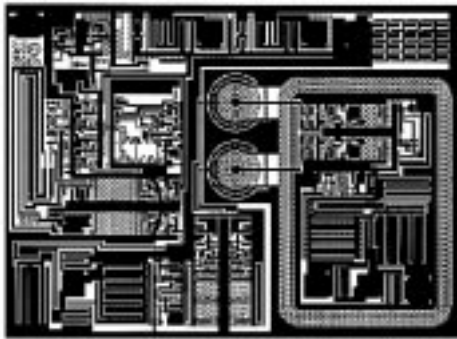
Lead Definitions

Lead	
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

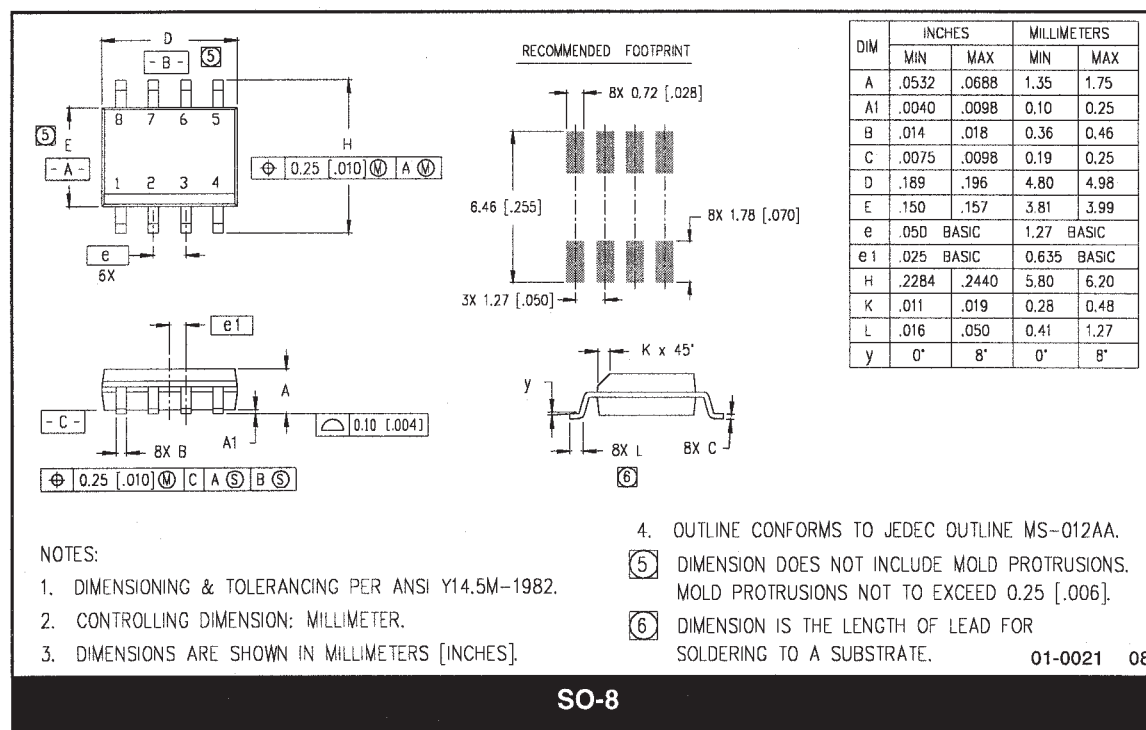
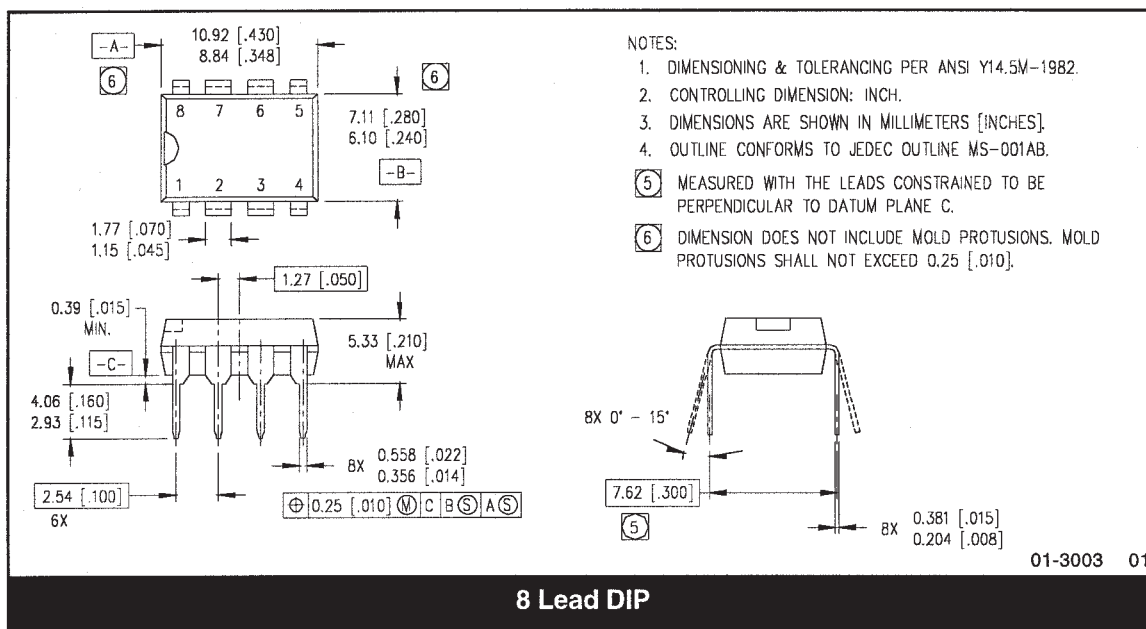
8 Lead DIP IR2105	SO-8 IR2106S
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Device Information

Process & Design Rule		HVDCMOS 4.0 μm	
Transistor Count		168	
Die Size		67 X 91 X 26 (mil)	
Die Outline			
Thickness of Gate Oxide		800Å	
Connections	First Layer	Material	Poly Silicon
		Width	4 μm
		Spacing	6 μm
		Thickness	5000Å
	Second Layer	Material	Al - Si (Si: 1.0% ±0.1%)
		Width	6 μm
		Spacing	9 μm
		Thickness	20,000Å
Contact Hole Dimension		5 μm X 5 μm	
Insulation Layer	Material	PSG (SiO ₂)	
	Thickness	1.5 μm	
Passivation	Material	PSG (SiO ₂)	
	Thickness	1.5 μm	
Method of Saw		Full Cut	
Method of Die Bond		Ablebond 84 - 1	
Wire Bond	Method	Thermo Sonic	
	Material	Au (1.0 mil / 1.3 mil)	
Leadframe	Material	Cu	
	Die Area	Ag	
	Lead Plating	Pb : Sn (37 : 63)	
Package	Types	8 Lead PDIP / SO-8	
	Materials	EME6300 / MP150 / MP190	
Remarks:			

IR2105

International
IOR Rectifier



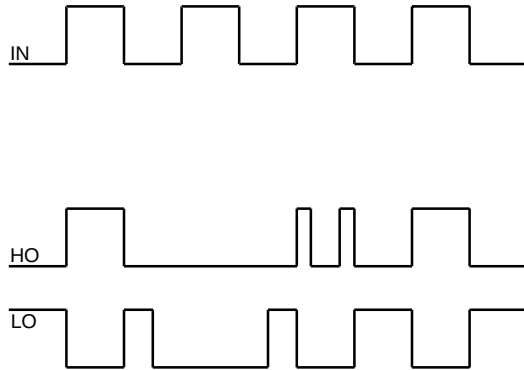


Figure 1. Input/Output Timing Diagram

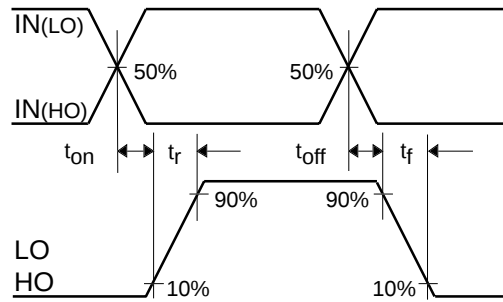


Figure 2. Switching Time Waveform Definitions

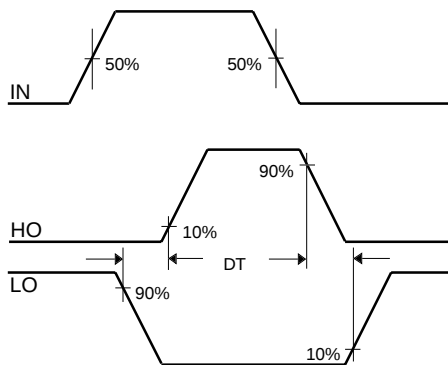


Figure 3. Deadtime Waveform Definitions

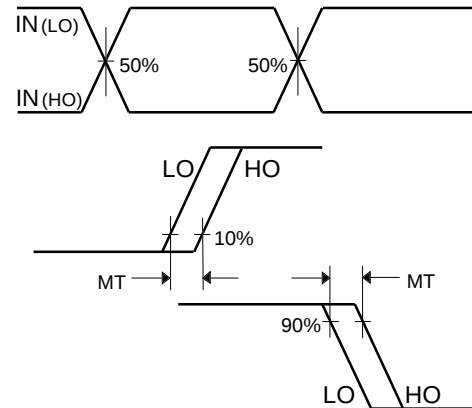


Figure 4. Delay Matching Waveform Definitions