



High-Speed CMOS 10 Bits Bus Switch with Flow-Thru Pinout

QS3861

2

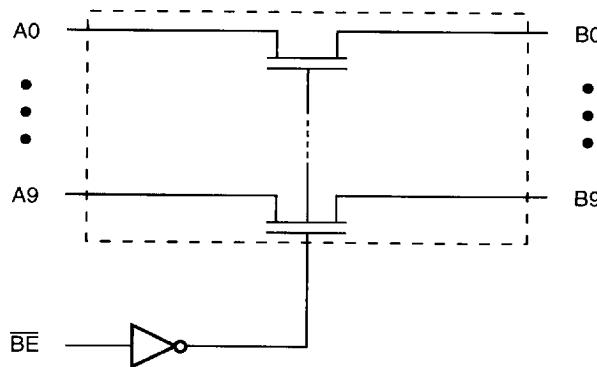
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay
- Undershoot clamp diodes on all inputs
- Low power QCMOS™ technology
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels
- Available in 24-pin QSOP and
and in 24-pin SOIC (SO) packages

DESCRIPTION

The QS3861 provides two ports of ten bits. The low ON resistance (5Ω) of the QS3861 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable (\overline{BE}) signal turns the switches on.

FUNCTIONAL BLOCK DIAGRAM

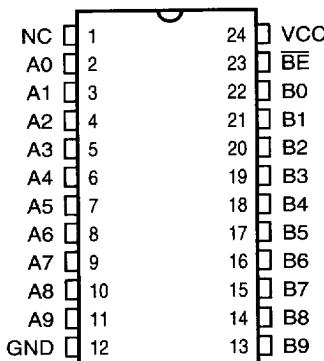


PIN DESCRIPTION

Name	Function
BE	Bus Enable
A9-A0	Bus A
B9-B0	Bus B
GND	Ground
Vcc	Power

PIN CONFIGURATION
(All Pins Top View)

QSOP, SOIC (SO)



FUNCTION TABLE

BE	A9-A0	Function
H	Hi-Z	Disconnect
L	B9-B0	Connect

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground (Inputs and VCC Only)	-0.5V to +7.0V
Supply Voltage to Ground (Outputs and D/O Only).....	-0.5V to Vcc
DC Input Voltage VIN	-0.5V to +7.0V
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
Tstg Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

TA = 25°C, f = 1 MHz, VIN = 0V

Pins	QSOP		SOIC		Unit
	Typ	Max	Typ	Max	
Input capacitance	—	6	—	6	pF
A/B Switch Off	—	6	—	6	pF
A/B Switch On	—	8	—	8	pF

Note: Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

2

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$ I_{IN} $	Input Leakage Current ⁽²⁾	$0 \leq V_{IN} \leq V_{CC}$	—	—	1	μA
$ I_{IOZ} $	Off-State Current (Hi-Z)	$0 \leq A, B \leq V_{CC}$	—	—	1	μA
R_{ON}	Switch ON Resistance ^(3,4)	$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}$ $I_{ON} = 30\text{ mA}$	—	5	7	Ω
R_{ON}	Switch ON Resistance ^(3,4)	$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}$ $I_{ON} = 15\text{ mA}$	—	10	15	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the \overline{BE} control is HIGH.
3. Measured by voltage drop between A and B pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A, B) pins.
4. Max. value R_{ON} guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽²⁾	Max	Unit
I _{CCA}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0	0.2	3.0	µA
ΔI _{CC}	Power Supply Current per Input HIGH	V _{CC} = Max., V _{IN} = 3.4V ⁽³⁾ , f = 0 per Control Input	—	2.5	mA
Q _{CCD}	Dynamic Power Supply Current per MHz ⁽⁴⁾	V _{CC} = Max., A and B Pins Open, \overline{BE} = GND, Control Inputs Toggling @ 50% Duty Cycle	—	0.25	mA/MHz
I _C	Total Power Supply Current ^(6,7)	V _{CC} = Max., A and B Pins at 0.0V, \overline{BE} = GND, Control Inputs Toggling @ 50% Duty Cycle V _{IH} = 3.4V, V _{IN} = GND, f Clock = MHz	—	9.0 ⁽⁵⁾	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Typical Values are at V_{CC} = 5.0V, +25°C Ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to I_{CC}.
4. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. I_C = I Quiescent + I Inputs + I Dynamic.
 $I_C = I_{CC} + \Delta I_{CC} D_{HT} N_T + Q_{CCD} (f/2 + f_i N_i)$
I_{CC} = Power Supply Current for each TTL HIGH input (V_{IN} = 3.4V, control inputs only).
D_{HT} = Duty Cycle for each TTL input that is HIGH (control inputs only).
N_T = Number of TTL inputs that are at D_{HT} (control inputs only).
I_{CCD} = Dynamic Current caused by an Input Transition Pair (HHL or LHL).
f = Clock Frequency for Register Devices (Zero for Non-Register Devices).
f_i = frequency that the inputs are toggled (control inputs only).
N_i = Number of inputs at f_i.
All currents are in millamps and all frequencies are in megahertz.
7. Note that activity on A and/or B inputs do not contribute to I_C if A and B inputs are between GND and V_{CC}. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, I_C will be equal to I_{CC} only regardless of activity on the A and B pins.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$ $C_{LOAD} = 50\text{ pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

2

Symbol	Description ⁽¹⁾	QS3861			Unit
		Min	Typ	Max	
t_{PLH}	Data Propagation Delay ^(2,3) A to B or B to A	—	0.25	—	ns
t_{PZL}	Switch Turn-on Delay \overline{BE} to A or B	1.5	—	6.5	ns
t_{PLZ}	Switch Turn-off Delay \overline{BE} to A or B	1.5	—	5.5	ns
$ Q_{CI} $	Charge Injection	—	1.5	—	pC

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.