IRFF9130, IRFF9131
IRFF9132, IRFF9133

File Number **2216**

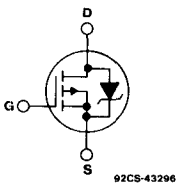
Avalanche-Energy-Rated P-Channel Power MOSFETs

-5.5A and -6.5A, -60V and -100V
r_{DS} (on) = 0.30Ω and 0.40Ω

Features:

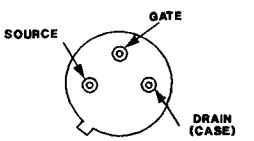
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF9130, IRFF9131, IRFF9132 and IRFF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

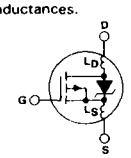
Absolute Maximum Ratings

	Parameter	IRFF9130	IRFF9131	IRFF9132	IRFF9133	Units
V_{DS}	Drain – Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-6.5	-6.5	-5.5	-5.5	A
I_{DM}	Pulsed Drain Current ③	-26	-26	-22	-22	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{AS}	Single Pulse Avalanche Energy ④	500				mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF9130 IRFF9132	-100	–	–	V	V_{GS} = 0V
		IRFF9131 IRFF9133	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	-100	nA	V_{GS} = -20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF9130 IRFF9131	-6.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRFF9132 IRFF9133	-5.5	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF9130 IRFF9131	–	0.25	0.30	Ω	V_{GS} = -10V, I_D = -3.0A
		IRFF9132 IRFF9133	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -3.0A
C_{iss}	Input Capacitance	ALL	–	500	–	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	70	140	ns	
t_f	Fall Time	ALL	–	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	12	22	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

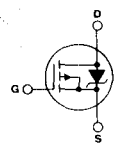


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	ALL	–	–	5.0	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	ALL	–	–	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF9130 IRFF9131	–	–	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF9132 IRFF9133	–	–	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF9130 IRFF9131	–	–	-26	A	
		IRFF9132 IRFF9133	–	–	-22	A	
V_{SD}	Diode Forward Voltage ②	IRFF9130 IRFF9131	–	–	-1.5	V	T_C = 25°C, I_S = -6.5A, V_{GS} = 0V
		IRFF9132 IRFF9133	–	–	-1.5	V	T_C = 25°C, I_S = -5.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.8	–	μC	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 25V, starting T_J = 25°C, L = 17.75 mH, R_G = 25Ω, Peak I_L = 6.5A. (See Fig. 15 and 16)

IRFF9130, IRFF9131, IRFF9132, IRFF9133

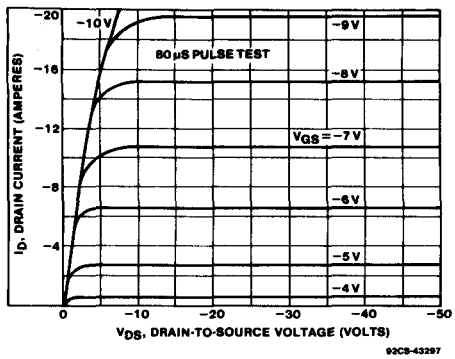


Fig. 1 - Typical Output Characteristics

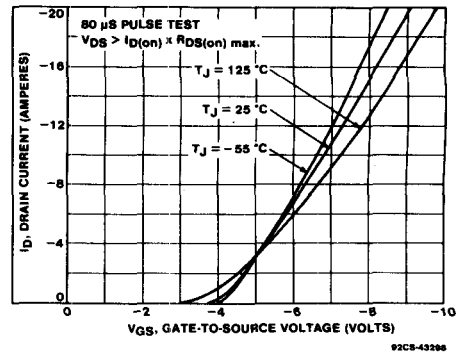


Fig. 2 - Typical Transfer Characteristics

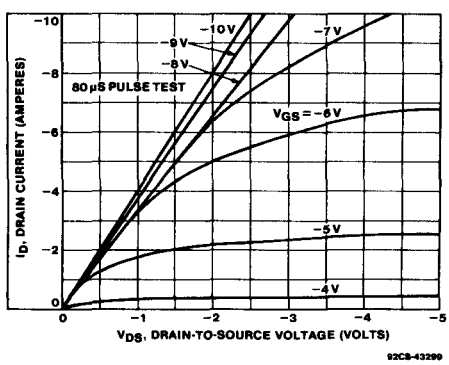


Fig. 3 - Typical Saturation Characteristics

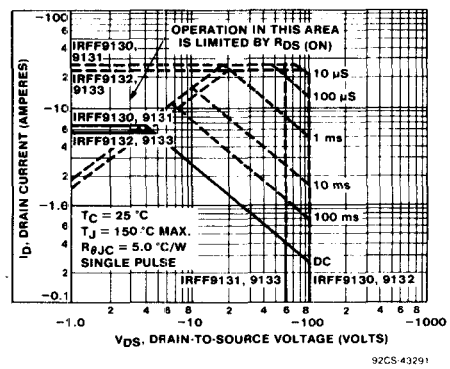


Fig. 4 - Maximum Safe Operating Area

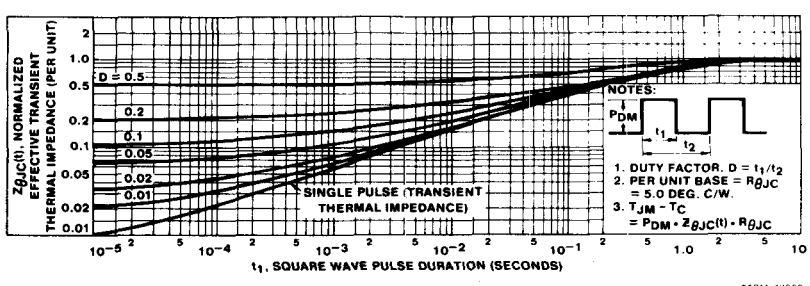


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

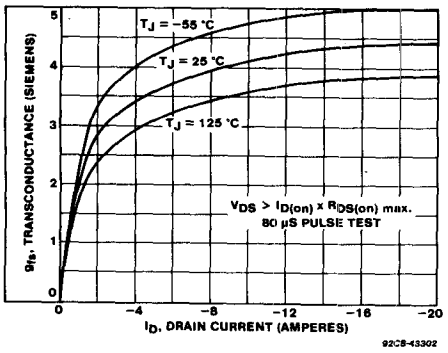


Fig. 6 - Typical Transconductance Vs. Drain Current

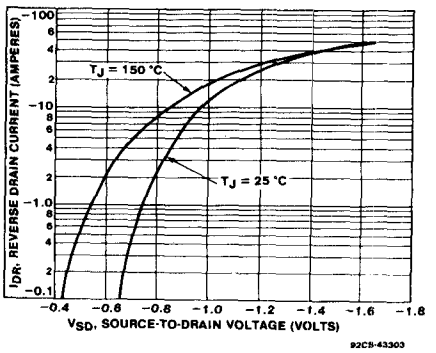


Fig. 7 - Typical Source-Drain Diode Forward Voltage

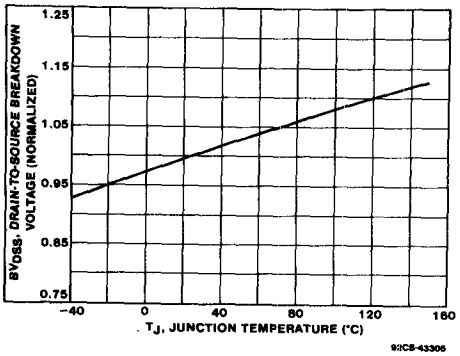


Fig. 8 - Breakdown Voltage Vs. Temperature

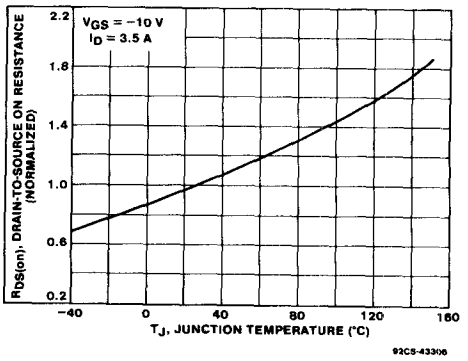


Fig. 9 - Normalized On-Resistance Vs. Temperature

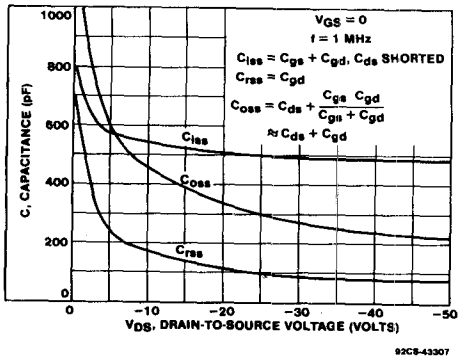


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

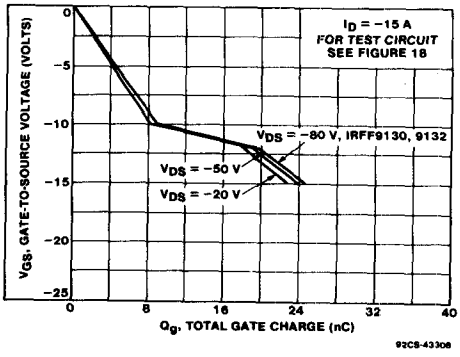


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

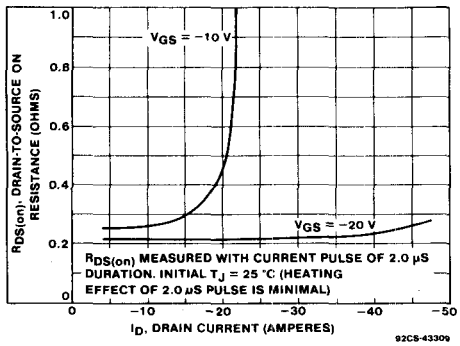


Fig. 12 - Typical On-Resistance Vs. Drain Current

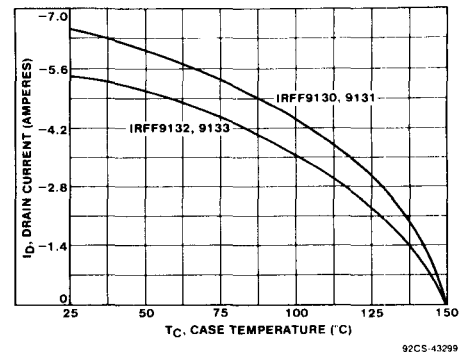


Fig. 13 - Maximum Drain Current Vs. Case Temperature

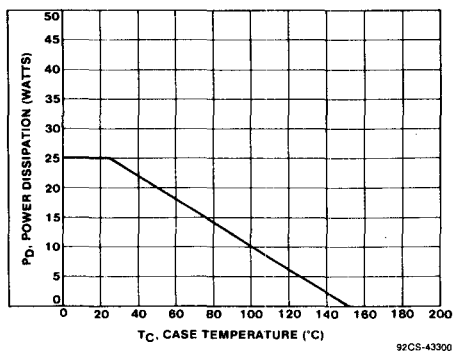


Fig. 14 - Power Vs. Temperature Derating Curve

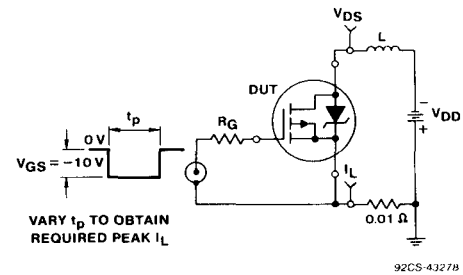


Fig. 15 - Unclamped Inductive Test Circuit

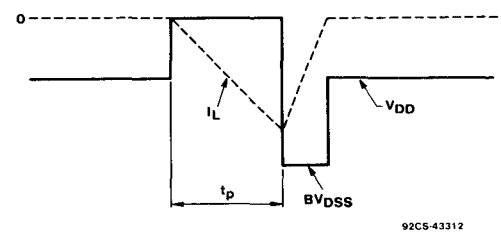


Fig. 16 - Unclamped Inductive Waveforms

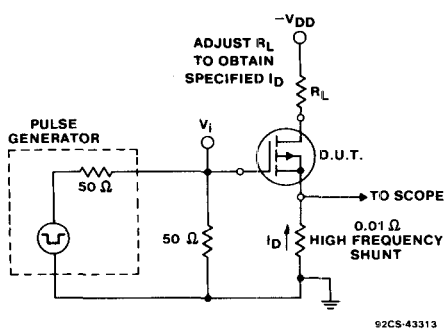


Fig. 17 - Switching Time Test Circuit

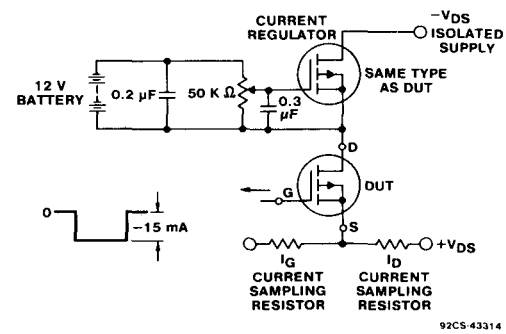


Fig. 18 - Gate Charge Test Circuit