CY25402/CY25422/CY25482

Two PLL Programmable Clock Generator with Spread Spectrum

Features

- Two fully integrated phase locked loops (PLLs)
- Input frequency range
  - External crystal: 8 to 48 MHz
  - External reference: 8 to 166 MHz clock
- Reference Clock input voltage range
  - 2.5V, 3.0V, and 3.3V for CY25482
  - 1.8V for CY25402 and CY25422
- Wide operating output frequency range
  - 3 to 166 MHz
- Programmable Spread Spectrum with Center and Down Spread option and Lexmark and Linear modulation profiles
- VDD supply voltage options:
  - 2.5V, 3.0V, and 3.3V for CY25402 and CY25482
  - 1.8V for CY25422
- Selectable output clock voltages independent of VDD:
  - 2.5V, 3.0V, and 3.3V for CY25402 and CY25482
  - 1.8V for CY25422
- Frequency Select feature with option to select four different frequencies
- Power Down, Output Enable, and SS ON/OFF controls
- Low jitter, high accuracy outputs
- Ability to synthesize nonstandard frequencies with Fractional-N capability
- Three clock outputs with Programmable drive strength
- Glitch-free outputs while frequency switching
- 8-pin SOIC package
- Commercial and Industrial temperature ranges

Benefits

- Multiple high performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific Programmable EMI reduction using Spread Spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of Zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low power systems

Block Diagram

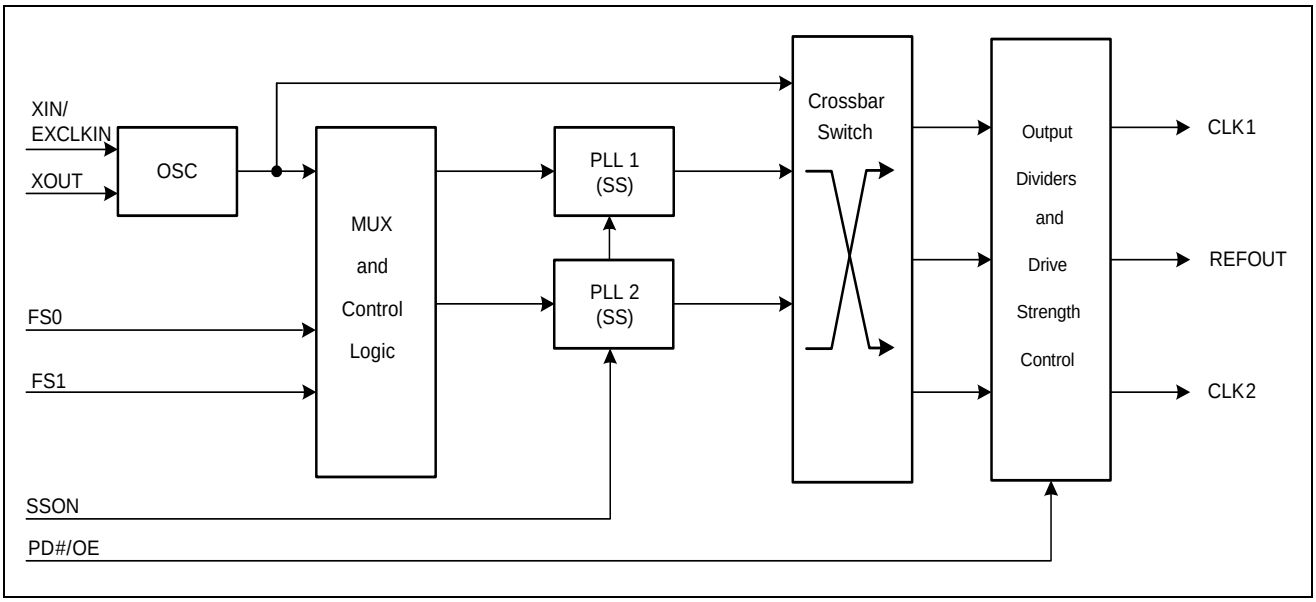


Table 1. Device Selector Guide

Device	Crystal Input	EXCKLKIN Input	VDD
CY25402	Yes	1.8V LVCMOS	2.5V, 3.0V, 3.3V
CY25482	No	2.5V, 3.0V, 3.3V LVCMOS	2.5V, 3.0V, 3.3V
CY25422	Yes	1.8V LVCMOS	1.8V

Figure 1. Pin Diagram - CY25402 8-LD SOIC

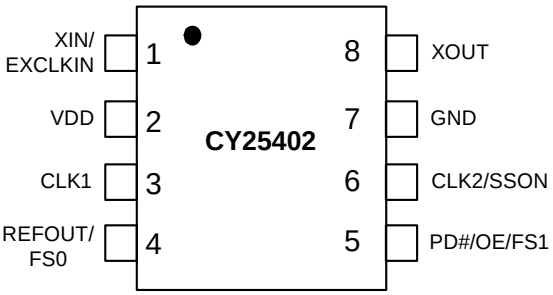


Table 1. Pin Definition - CY25402 (2.5V, 3.0V or 3.3V Supply)

Pin Number	Name	IO	Description
1	XIN/EXCLKIN	Input	Crystal Input or 1.8V External Clock Input
2	VDD	Power	Power Supply: 2.5V, 3.0V or 3.3V
3	CLK1	Output	Programmable Clock Output with Spread Spectrum
4	REFOUT/FS0	Output/Input	Multifunction Programmable pin: Reference Clock Output or Frequency Select pin
5	PD#/OE/FS1	Input	Multifunction Programmable pin: Power Down, Output Enable or Frequency Select pin
6	CLK2/SSON	Output/Input	Multifunction Programmable pin: Programmable Clock Output with Spread Spectrum or Spread Spectrum ON/OFF control pin
7	GND	Power	Power Supply Ground
8	XOUT	Output	Crystal Output

Figure 2. Pin Diagram - CY25482 8-LD SOIC

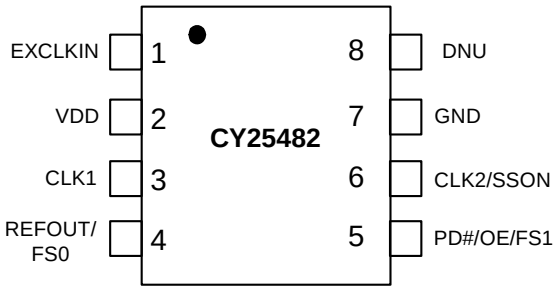


Table 2. Pin Definition - CY25482 (2.5V, 3.0V or 3.3V Supply)

Pin Number	Name	IO	Description
1	EXCLKIN	Input	2.5V, 3.0V or 3.3V External Clock Input
2	VDD	Power	Power Supply: 2.5V, 3.0V or 3.3V
3	CLK1	Output	Programmable Clock Output with Spread Spectrum
4	REFOUT/FS0	Output/Input	Multifunction Programmable pin: Reference Clock Output or Frequency Select pin
5	PD#/OE/FS1	Input	Multifunction Programmable pin: Power Down, Output Enable or Frequency Select pin
6	CLK2/SSON	Output/Input	Multifunction Programmable pin: Programmable Clock Output with Spread Spectrum or Spread Spectrum ON/OFF control pin
7	GND	Power	Power Supply Ground
8	DNU	Output	Do not use this pin

Figure 3. Pin Diagram - CY25422 8-LD SOIC

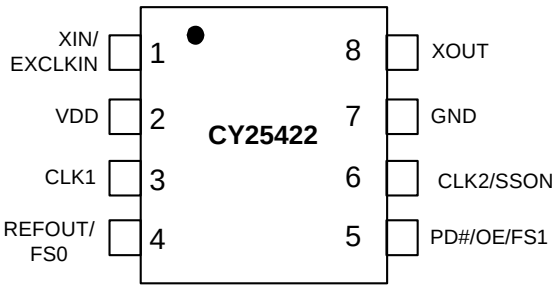


Table 3. Pin Definition - CY25422 (1.8V Supply)

Pin Number	Name	IO	Description
1	XIN/EXCLKIN	Input	Crystal Input or 1.8V External Clock Input
2	VDD	Power	Power Supply: 1.8V
3	CLK1	Output	Programmable Clock Output with Spread Spectrum
4	REFOUT/FS0	Output/Input	Multifunction Programmable pin: Reference Clock Output or Frequency Select pin
5	PD#/OE/FS1	Input	Multifunction Programmable pin: Power Down, Output Enable or Frequency Select pin
6	CLK2/SSON	Output/Input	Multifunction Programmable pin: Programmable Clock Output with Spread Spectrum or Spread Spectrum ON/OFF control pin
7	GND	Power	Power Supply Ground
8	XOUT	Output	Crystal Output

General Description

2 Configurable PLLs

The CY25402, CY25482 and CY25422 have two programmable PLLs that can be used to generate output frequencies ranging from 3 to 166 MHz. The advantage of having two PLLs is that a single device generates two independent frequencies from a single crystal.

Input Reference Clocks

The input reference clock can be either a crystal or a clock signal, for CY25402 and CY25422 while just a clock signal for CY25482. The input frequency range for crystal (XIN) is 8 MHz to 48 MHz and that for external reference clock (EXCLKIN) is 8 MHz to 166 MHz. The voltage range of the reference clock input for CY25482 is 2.5V/3.0V/3.3V while that for CY25402 and CY25422 is 1.8V. This gives user an option for this device to be compatible for different input clock voltage levels in the system.

VDD Power Supply Options

These devices have programmable power supply options. The CY25402/CY25482 is a high voltage part that can be programmed to operate at any voltage 2.5V, 3.0V, or 3.3V while CY25422 is a low voltage part that can operate at 1.8V.

Output Source Selection

These devices have programmable input sources for each of its clock outputs. There are three available clock sources and these clock sources are: XIN/EXCLKIN, PLL1, and PLL2. Output clock source selection is done by using three out of three crossbar switch. Thus, any one of these three available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have two independent clock outputs.

Spread Spectrum Control

Both PLLs (PLL1 and PLL2) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK2/SSON). It can be programmed to either center spread range from ±0.125% to ±2.50% or down spread range from –0.25% to –5.0% with Lexmark or Linear profile.

Frequency Select

Each PLL can be programmed for up to four different frequencies. There are two multifunction programmable pins, REFOUT/FS0 and PD#/OE/FS1 which if programmed as frequency select inputs, can be used to select among these arbitrarily programmed frequency settings. Each output has programmable output divider options.

Glitch-Free Frequency Switch

When the frequency select pin, FS(1:0) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

PD#/OE Mode

Multifunction pin PD#/OE/FS1 (Pin 5) can be programmed to operate as either frequency select (FS1), power down (PD#) or output enable (OE) mode. PD# is a low-true input. If activated it shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings.

When this pin is programmed as Output Enable (OE), clock outputs can be enabled or disabled using OE (pin 5). Individual clock outputs can be programmed to be sensitive to this OE pin.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 4 shows the typical rise and fall times for different drive strength settings.

Table 4. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	6.8
Mid Low	3.4
Mid High	2.0
High	1.0

Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The devices, CY25402, CY25482 and CY25422 can be custom programmed to any desired frequencies and listed features. For customer specific programming, please contact local Cypress Field Application Engineer (FAE) or sales representative.

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage for CY25402/CY25482		–0.5	4.5	V
V_{DD}	Supply Voltage for CY25422		–0.5	2.6	V
V_{IN}	Input Voltage for CY25402/CY25482	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
V_{IN}	Input Voltage for CY25422	Relative to V_{SS}	–0.5	2.2	V
T_S	Temperature, Storage	Non Functional	–65	+150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC EIA/JESD22-A114-E	2000		Volts
UL-94	Flammability Rating	V-0 @1/8 in.		10	ppm
MSL	Moisture Sensitivity Level	SOIC package	3		

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	VDD Operating Voltage for CY25402/CY25482	2.25	–	3.60	V
V_{DD}	VDD Operating Voltage for CY25422	1.65	1.8	1.95	V
T_{AC}	Commercial Ambient Temperature	0	–	+70	°C
T_{AI}	Industrial Ambient Temperature	–40	--	+85	°C
C_{LOAD}	Maximum Load Capacitance	–	–	15	pF
t_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, drive strength = [00]	–	–	0.4	V
		I_{OL} = 3 mA, drive strength = [01]				
		I_{OL} = 7 mA, drive strength = [10]				
		I_{OL} = 12 mA, drive strength = [11]				
V_{OH}	Output High Voltage	I_{OH} = –2 mA, drive strength = [00]	V_{DD} – 0.4	–	–	V
		I_{OH} = –3 mA, drive strength = [01]				
		I_{OH} = –7 mA, drive strength = [10]				
		I_{OH} = –12 mA, drive strength = [11]				
V_{IL1}	Input Low Voltage of PD#/OE, FS0, FS1 and SSON		–	–	0.2*V_{DD}	V
V_{IL2}	Input Low Voltage of EXCLKIN		–	–	0.18	V
V_{IH1}	Input High Voltage of PD#/OE, FS0, FS1 and SSON		0.8*V_{DD}	–	–	V
V_{IH2}	Input High Voltage of EXCLKIN for CY25402/CY25422		1.62	–	2.2	V
V_{IH3}	Input High Voltage of EXCLKIN for CY25482		0.8*V_{DD}	–	–	V
I_{IL}	Input Low Current, PD#/OE/FS1	V_{IN} = 0V	–	–	10	µA
I_{IH}	Input High Current, PD#/OE/FS1	V_{IN} = V_{DD}	–	–	10	µA
I_{ILDN}	Input Low Current, SSON and FS0 pins	V_{IN} = 0V (Internal pull down resistor = 160k typ.)	–	–	10	µA
I_{IHDN}	Input High Current, SSON and FS0 pins	V_{IN} = V_{DD} (Internal pull down resistor = 160k typ.)	14	–	36	µA
R_{DN}	Pull Down Resistor of CLK1, REFOUT/FS0 and CLK2/SSON pins	Output clocks in off state by setting PD# = Low	100	160	250	kΩ
I_{DD}[1,2]	Supply Current for CY25422	PD# = High, No load	–	12	–	mA
	Supply Current for CY25402/CY25482	PD# = High, No load	–	14	–	mA
I_{DDS}[1]	Standby Current	PD# = Low	–	3	–	µA
C_{IN}[1]	Input Capacitance	SSON, PD#/OE/FS1 and FS0 pins	–	–	7	pF

Notes
1. Guaranteed by design but not 100% tested
2. Configuration dependent

AC Electrical Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{IN} (crystal)	Crystal Frequency, XIN		8	–	48	MHz
F_{IN} (clock)	Input Clock Frequency (EXCLKIN)		8	–	166	MHz
F_{CLK}	Output Clock Frequency		3	–	166	MHz
DC	Output Duty Cycle, All Clocks except Ref Out	Duty Cycle is defined in Figure 5 on page 8; t_1/t_2, measured at 50% of V_{DD}	45	50	55	%
DC	Ref Out Duty Cycle	Ref In Min 45%, Max 55%	40	–	60	%
T_{RF1}[1]	Output Rise/Fall Time	Measured from 20% to 80% of $V_{DD,}$ as shown in Figure 6 on page 8, C_{LOAD} = 15 pF, drive strength [00]	–	6.8	–	ns
T_{RF2}[1]	Output Rise/Fall Time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 8, C_{LOAD} = 15 pF, drive strength [01]	–	3.4	–	ns
T_{RF3}[1]	Output Rise/Fall Time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 8, C_{LOAD} = 15 pF, drive strength [10]	–	2.0	–	ns
T_{RF4}[1]	Output Rise/Fall Time	Measured from 20% to 80% of V_{DD}, as shown in Figure 6 on page 8, C_{LOAD} = 15 pF, drive strength [11]	–	1.0	–	ns
T_{CCJ}[1,2]	Cycle-to-cycle Jitter (peak)	Configuration dependent. See Table 5	–	100	–	ps
T_{LOCK}[1]	PLL Lock Time	Measured from 90% of the applied power supply level	–	1	3	ms

Table 5. Configuration Example for C-C Jitter

Ref. Frequency (MHz)	CLK1 Output		CLK2 Output	
	Freq. (MHz)	C-C Jitter Typ (ps)	Freq. (MHz)	C-C Jitter Typ (ps)
14.3181	8.0	134	48	92
19.2	74.25	99	8	91
27	48	67	166	103
48	48	93	166	137

Recommended Crystal Specification for SMD Package

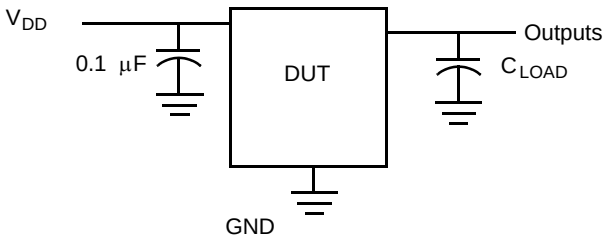
Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum Frequency	8	14	28	MHz
Fmax	Maximum Frequency	14	28	48	MHz
R1	Motional Resistance (ESR)	135	50	30	Ω
C0	Shunt Capacitance	4	4	2	pF
CL	Parallel Load Capacitance	18	14	12	pF
DL(max)	Maximum Crystal Drive Level	300	300	300	µW

Recommended Crystal Specification for Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum Frequency	8	14	24	MHz
Fmax	Maximum Frequency	14	24	32	MHz
R1	Motional Resistance (ESR)	90	50	30	Ω
C0	Shunt Capacitance	7	7	7	pF
CL	Parallel Load Capacitance	18	12	12	pF
DL(max)	Maximum Crystal Drive Level	1000	1000	1000	µW

Test and Measurement Setup

Figure 4. Test and Measurement Setup



Voltage and Timing Definitions

Figure 5. Duty Cycle Definition

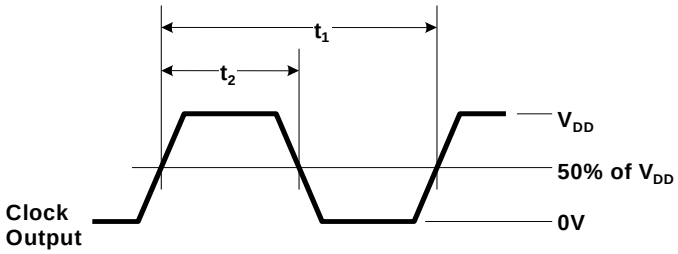
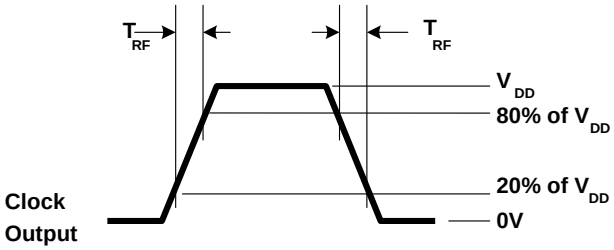


Figure 6. Rise Time = T_{RF}, Fall Time = T_{RF}

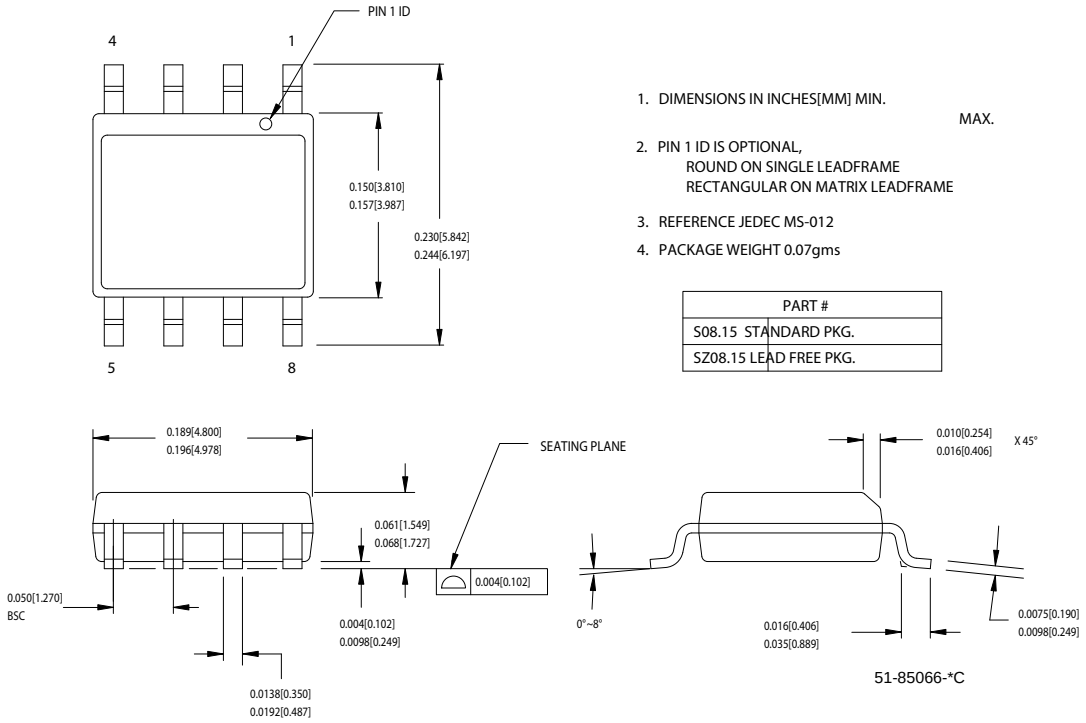


Ordering Information

Part Number[3]	Type	VDD(V)	Production Flow
Pb-free			
CY25402SXC-xxx	8-pin SOIC	Supply Voltage: 2.5V, 3.0V or 3.3V	Commercial, 0°C to 70°C
CY25402SXC-xxxT	8-pin SOIC -Tape & Reel	Supply Voltage: 2.5V, 3.0V or 3.3V	Commercial, 0°C to 70°C
CY25482SXC-xxx	8-pin SOIC	Supply Voltage: 2.5V, 3.0V or 3.3V	Commercial, 0°C to 70°C
CY25482SXC-xxxT	8-pin SOIC -Tape & Reel	Supply Voltage: 2.5V, 3.0V or 3.3V	Commercial, 0°C to 70°C
CY25422SXC-xxx	8-pin SOIC	Supply Voltage: 1.8V	Commercial, 0°C to 70°C
CY25422SXC-xxxT	8-pin SOIC -Tape & Reel	Supply Voltage: 1.8V	Commercial, 0°C to 70°C
CY25402SXI-xxx	8-pin SOIC	Supply Voltage: 2.5V, 3.0V or 3.3V	Industrial, -40°C to +85°C
CY25402SXI-xxxT	8-pin SOIC -Tape & Reel	Supply Voltage: 2.5V, 3.0V or 3.3V	Industrial, -40°C to +85°C
CY25482SXI-xxx	8-pin SOIC	Supply Voltage: 2.5V, 3.0V or 3.3V	Industrial, -40°C to +85°C
CY25482SXI-xxxT	8-pin SOIC -Tape & Reel	Supply Voltage: 2.5V, 3.0V or 3.3V	Industrial, -40°C to +85°C
CY25422SXI-xxx	8-pin SOIC	Supply Voltage: 1.8V	Industrial, -40°C to +85°C
CY25422SXI-xxxT	8-pin SOIC -Tape & Reel	Supply Voltage: 1.8V	Industrial, -40°C to +85°C

Package Drawing and Dimensions

Figure 7. 8-lead (150-Mil) SOIC S8



Note
3. xxx indicates Factory Programmable and are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Document History Page

Document Title: CY25402/CY25422/CY25482 Two PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12565				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	690296	See ECN	RGL	New Data Sheet
*A	815788	See ECN	RGL	Minor Change: To post on web
*B	1428744	See ECN	RGL/AESA	Changed data sheet format to match generic part, CY2544/46 Added new device and specification for high ref. input voltage part, CY25482 Removed Preliminary from Title page Replaced CLK2 with REFOUT
*C	2748211	08/10/09	TSAI	Posting to external web.