

Not Recommended for New Designs

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MAXIM

Low Offset Voltage Operational Amplifier

OP07

General Description

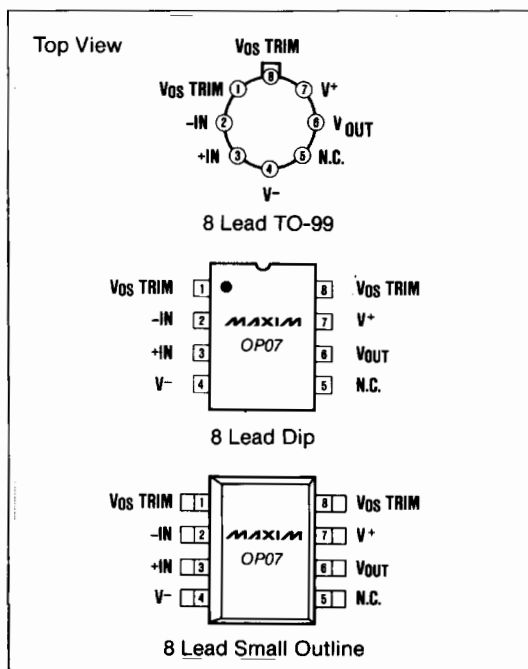
The OP07 is a precision operational amplifier with very low input offset voltage ($10\mu\text{V}$ typ., $25\mu\text{V}$ max. for the OP07A), input offset drift of $0.2\mu\text{V}/^\circ\text{C}$ and low input bias current of 0.7nA . The wide input common mode range of $\pm 14\text{V}$ combined with high CMRR of 110dB minimum (OP07A), plus high input impedance and high open-loop gain make these devices particularly useful for high-gain instrumentation applications.

The excellent linearity and gain accuracy are maintained at high open-loop gains, over both time and temperature. The OP07 has become an industry standard and Maxim's reliability and quality are added advantages.

Applications

Precision Amplifiers
Thermocouple Amplifiers
Low Level Signal Processing
Medical Instrumentation
Strain Gauge Amplifiers
High Accuracy Data Acquisition

Pin Configuration



Features

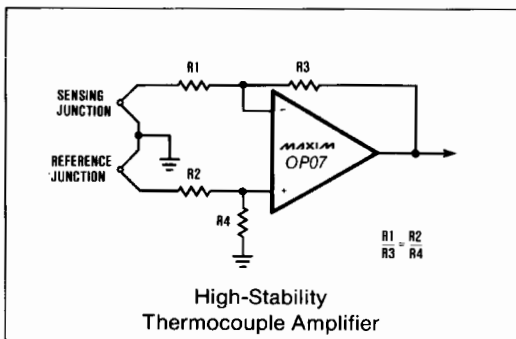
- ◆ Ultra Low Offset Voltage: $10\mu\text{V}$
- ◆ Ultra Low Offset Voltage Drift: $0.2\mu\text{V}/^\circ\text{C}$
- ◆ Ultra Stable vs. Time: $0.2\mu\text{V}/\text{Month}$
- ◆ Ultra Low Noise: $0.35\mu\text{V}_{\text{p-p}}$
- ◆ Wide Supply Voltage: $\pm 3\text{V}$ to $\pm 18\text{V}$
- ◆ High Common Mode Input: $\pm 14\text{V}$
- ◆ No External Components Required
- ◆ Fits AD510, 725, 108A/308A, 741 Sockets

Ordering Information

PART	TEMP. RANGE	PACKAGE
OP07AJ	-55°C to $+125^\circ\text{C}$	TO-99
OP07J	-55°C to $+125^\circ\text{C}$	TO-99
OP07EJ	0°C to $+70^\circ\text{C}$	TO-99
OP07CJ	0°C to $+70^\circ\text{C}$	TO-99
OP07DJ	0°C to $+70^\circ\text{C}$	TO-99
OP07EP	0°C to $+70^\circ\text{C}$	8 Lead Plastic Dip
OP07CP	0°C to $+70^\circ\text{C}$	8 Lead Plastic Dip
OP07DP	0°C to $+70^\circ\text{C}$	8 Lead Plastic Dip
OP07AZ	-55°C to $+125^\circ\text{C}$	8 Lead Hermetic Dip
OP07Z	-55°C to $+125^\circ\text{C}$	8 Lead Hermetic Dip
OP07EZ	0°C to $+70^\circ\text{C}$	8 Lead Hermetic Dip
OP07CZ	0°C to $+70^\circ\text{C}$	8 Lead Hermetic Dip
OP07ECSA	0°C to $+70^\circ\text{C}$	8 Lead Small Outline
OP07CCSA	0°C to $+70^\circ\text{C}$	8 Lead Small Outline
OP07DCSA	0°C to $+70^\circ\text{C}$	8 Lead Small Outline
OP07D/D	0°C to $+70^\circ\text{C}$	Dice

* Contact factory for dice specifications.

Typical Operating Circuit



MAXIM

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Call toll free 1-800-998-8800 for free samples or literature.

Low Offset Voltage Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) $\pm 22V$
 Internal Power Dissipation 500mW
 TO-99(J) — derate at 7.1mW/°C above +80°C
 Hermetic Dip(Z) — derate at 6.7mW/°C above +75°C
 Plastic Dip(P) — derate at 5.6mW/°C above +36°C
 Small Outline — derate at 5mW/°C above +55°C
 Differential Input Voltage $\pm 30V$
 Input Voltage (Note 1) $\pm 22V$

Storage Temperature Range -65°C to +150°C
 Operating Temperature Range
 OP07AJ, OP07AZ, OP07J and OP07Z -55°C to +125°C
 All Other Parts 0°C to +70°C
 Lead Temperature (Soldering, 10 sec) +300°C
 Duration of Output Short Circuit Indefinite
 Junction Temperature (T_J) -65°C to +160°C

Note 1: For supply voltages less than $\pm 22V$, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2)		10	25		30	75	μV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 3)		0.2	1.0		0.2	1.0	$\mu V/\text{Month}$
Input Offset Current	I_{OS}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_B			± 0.7	± 2.0		± 1.0	± 3.0	nA
Input Noise Voltage	$e_{N\text{P-P}}$	0.1Hz to 10Hz (Note 4)		0.35	0.6		0.35	0.6	μV_{P-P}
Input Noise Voltage Density	e_N	$f_O = 10\text{Hz}$ (Note 4)		10.3	18.0		10.3	18.0	$nV/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 4)		10.0	13.0		10.0	13.0	
		$f_O = 1000\text{Hz}$ (Note 4)		9.6	11.0		9.6	11.0	
Input Noise Current	$I_{N\text{P-P}}$	0.1Hz to 10Hz (Note 4)		14	30		14	30	pA_{P-P}
Input Noise Current Density	I_N	$f_O = 10\text{Hz}$ (Note 4)		0.32	0.80		0.32	0.80	$pA/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 4)		0.14	0.23		0.14	0.23	
		$f_O = 1000\text{Hz}$ (Note 4)		0.12	0.17		0.12	0.17	
Input Resistance Differential-Mode	R_{IN}	(Note 5)	30	80		20	60		M Ω
Input Resistance Common-Mode	R_{INCM}			200			200		G Ω
Input Voltage Range	IVR		± 13	± 14		± 13	± 14		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126		110	126		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$		4	10		4	10	$\mu V/V$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500		200	500		V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 5)	150	400		150	400		
Output Voltage Swing	$-V_O$	$R_L \geq 10k\Omega$	± 12.5	± 13.0		± 12.5	± 13.0		V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8		± 12.0	± 12.8		
		$R_L \geq 1k\Omega$	± 10.5	± 12.0		± 10.5	± 12.0		

Note 2: OP07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.

Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV . Parameter is sample tested.

Note 4: Sample tested.

Note 5: Guaranteed by design.

Low Offset Voltage Operational Amplifier

OP07

ELECTRICAL CHARACTERISTICS (continued)

($V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 6)	0.1	0.3		0.1	0.3		V/ μ S
Closed-Loop Bandwidth	BW	$A_{VCL} = +1V$ (Note 6)	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	$V_O = 0V$, $I_O = 0$		60			60		Ω
Power Consumption	P_D	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		75 4	120 6		75 4	120 6	mW
Offset Adjustment Range		$R_P = 20k\Omega$		± 4			± 4		mV

Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS

($V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 7)		25	60		60	200	μ V
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 8)		0.2	0.6		0.3	1.3	μ V/ $^\circ C$
Input Offset Current	I_{OS}			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 8)		5	25		8	50	pA/ $^\circ C$
Input Bias Current	I_B			± 1.0	± 4.0		± 2.0	± 6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 8)		8	25		13	50	pA/ $^\circ C$
Input Voltage Range	IVR		± 13	± 13.5		± 13	± 13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123		106	123		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$		5	20		5	20	μ V/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400		150	400		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6		± 12.0	± 12.6		V

Note 7: OP07A grade Offset Voltage is measured one minute after application of power. For all other grades V_{OS} is measured 0.5 seconds after power on.

Note 8: Sample tested.

Low Offset Voltage Operational Amplifier

ELECTRICAL CHARACTERISTICS

($V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07E			OP07C			OP07D			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 1)	30	75		60	150		60	150		μV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 2)	0.3	1.5		0.4	2.0		0.5	3.0		$\mu V/\text{Month}$
Input Offset Current	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0		nA
Input Bias Current	I_B		± 1.2	± 4.0		± 1.8	± 7.0		± 2.0	± 12.0		nA
Input Noise Voltage	$e_{N\text{P-P}}$	0.1Hz to 10Hz (Note 3)	0.35	0.6		0.38	0.65		0.38	0.65		μV_{P-P}
Input Noise Voltage Density	e_N	$f_O = 10\text{Hz}$ (Note 3)	10.3	18.0		10.5	20.0		10.5	20.0		$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 3)	10.0	13.0		10.2	13.5		10.3	13.5		
		$f_O = 1000\text{Hz}$ (Note 3)	9.6	11.0		9.8	11.5		9.8	11.5		
Input Noise Current	$I_{N\text{P-P}}$	0.1Hz to 10Hz (Note 3)	14	30		15	35		15	35		pA_{P-P}
Input Noise Current Density	I_N	$f_O = 10\text{Hz}$ (Note 3)	0.32	0.80		0.35	0.90		0.35	0.90		$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 3)	0.14	0.23		0.15	0.27		0.15	0.27		
		$f_O = 1000\text{Hz}$ (Note 3)	0.12	0.17		0.13	0.18		0.13	0.18		
Input Resistance Differential-Mode	R_{IN}	(Note 4)	15	50		8	33		7	31		M Ω
Input Resistance Common-Mode	R_{INCM}		160			120			120			G Ω
Input Voltage Range	I_{VR}		± 13	± 14		± 13	± 14		± 13	± 14		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	5	20		7	32		7	32		$\mu V/V$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500		120	400		120	400		V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 5)	150	400		100	400			400		
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0		± 12.0	± 13.0		± 12.0	± 13.0		V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8		± 11.5	± 12.8		± 11.5	± 12.8		
		$R_L \geq 1k\Omega$	± 10.5	± 12.0			± 12.0			± 12.0		
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3		0.1	0.3		0.1	0.3		V/ μS
Closed-Loop Bandwidth	BW	$A_{VCL} = +1V$ (Note 3)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	$V_O = 0V$, $I_O = 0$	60			60			60			Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	75	120		80	150		80	150		mW
		$V_S = \pm 3V$, No Load	4	6		4	8		4	8		
Offset Adjustment Range		$R_P = 20k\Omega$	± 4			± 4			± 4			mV

Note 1: Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Note 2: Long-Term Input Offset Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation.

Note 3: Sample tested.

Note 4: Guaranteed by design.

Low Offset Voltage Operational Amplifier

OP07

ELECTRICAL CHARACTERISTICS

($V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07E			OP07C			OP07D			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 5)	45	130		85	250		85	250		μV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 6)	0.3	1.3		0.4	1.8		0.7	2.5		$\mu V/^\circ C$
Input Offset Current	I_{OS}		0.9	5.3		1.6	8.0		1.6	8.0		nA
Average Input Offset Current Drift	TCI_{OS}	(Note 6)	8	35		12	50		12	50		$pA/^\circ C$
Input Bias Current	I_B		± 1.5	± 5.5		± 2.2	± 9.0		± 3.0	± 14		nA
Average Input Bias Current Drift	TCI_B	(Note 6)	13	35		18	50		18	50		$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5		± 13.0	± 13.5		± 13.0	± 13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	7	32		10	51		10	51		$\mu V/V$
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	400		100	400		100	400		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6		± 11.0	± 12.6		± 11.0	± 12.6		V

Note 5: Input Offset Voltage is measured 0.5 seconds after application of power.

Note 6: Sample tested.

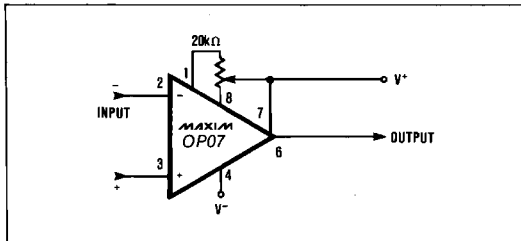


Figure 1. Optional Offset Nulling Circuit.

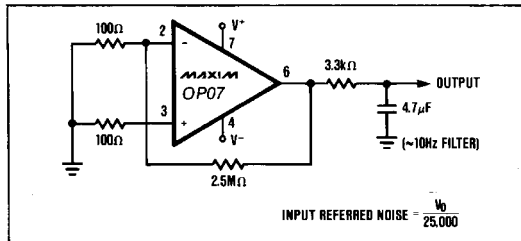
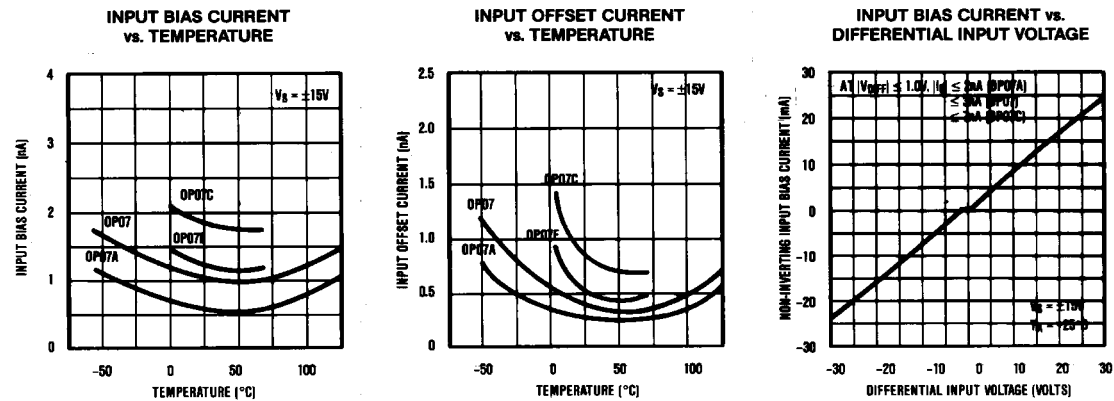
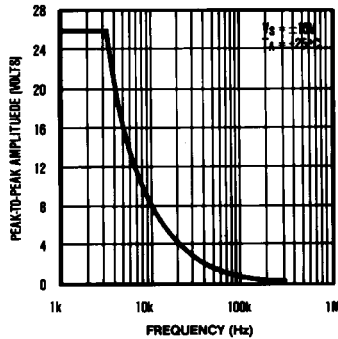


Figure 2. Low Frequency Noise Test Circuit.

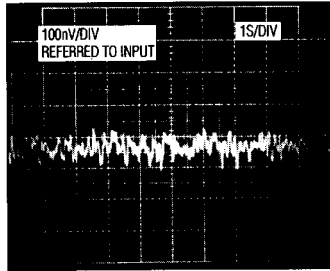


Low Offset Voltage Operational Amplifier

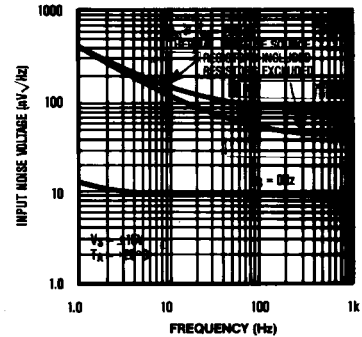
**MAXIMUM OUTPUT SWING
vs. FREQUENCY**



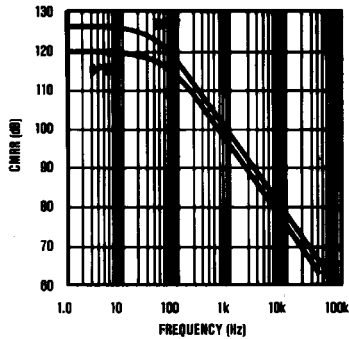
LOW FREQUENCY NOISE



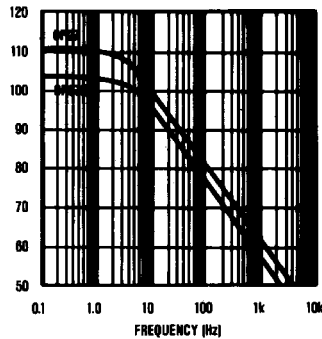
**TOTAL INPUT NOISE
VOLTAGE vs. FREQUENCY**



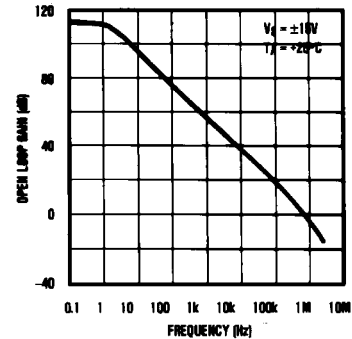
CMRR vs. FREQUENCY



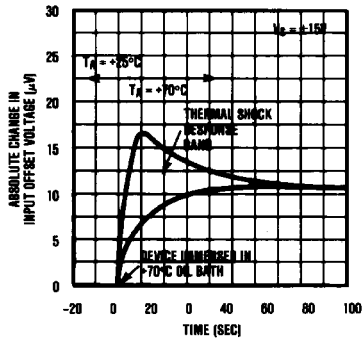
PSRR vs. FREQUENCY



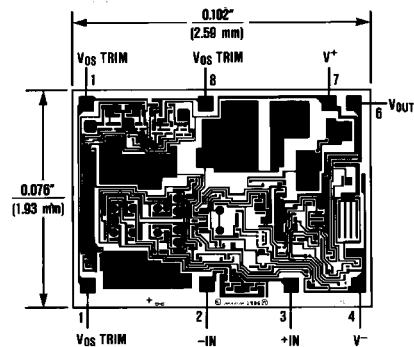
**OPEN LOOP
FREQUENCY RESPONSE**



**OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK**



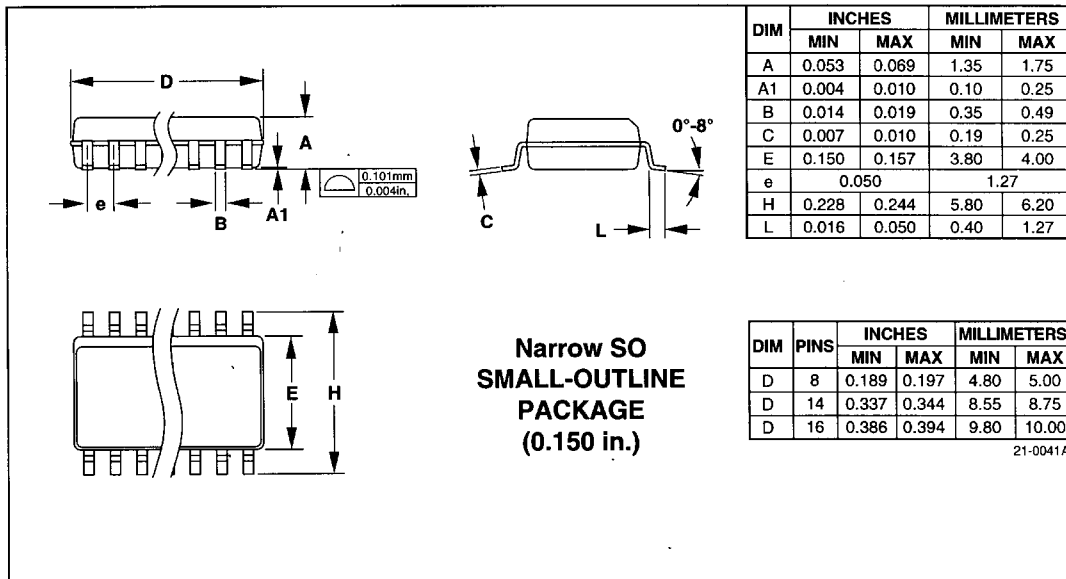
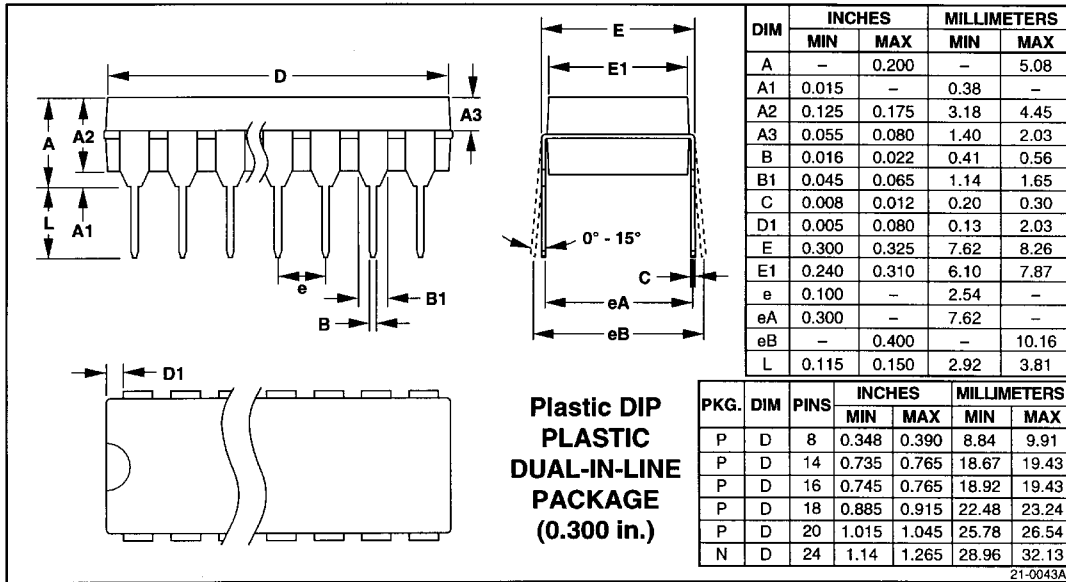
Chip Topography



Low Offset Voltage Operational Amplifier

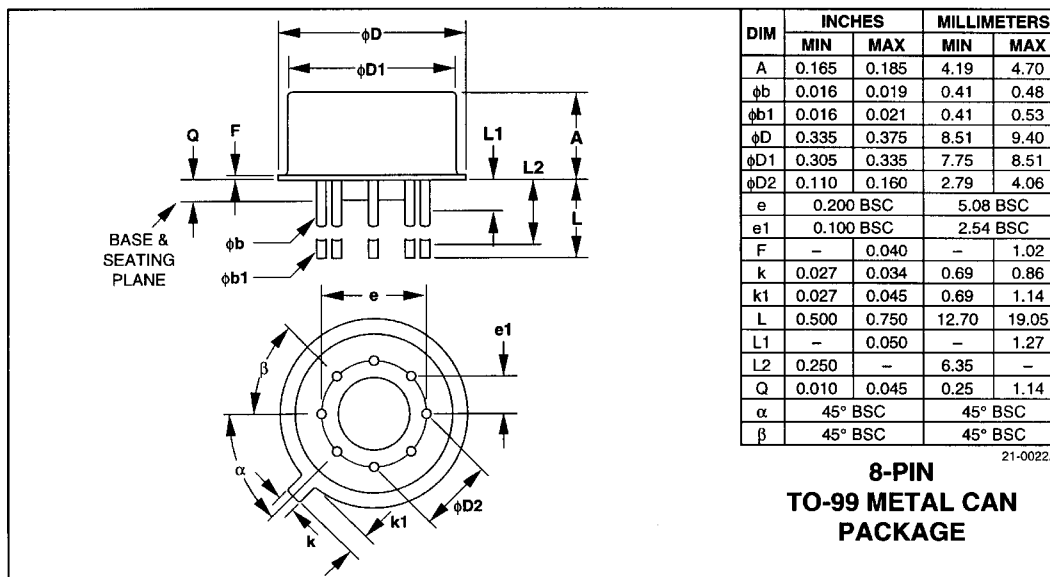
Package Information

OP07



Low Offset Voltage Operational Amplifier

Package Information (continued)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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[OP07DCSA+](#) [OP07DCSA+T](#) [OP07DCSA-T](#) [OP07DP](#) [OP07DP+](#) [OP07ECSA](#) [OP07ECSA+](#) [OP07ECSA+T](#)
[OP07ECSA-T](#) [OP07EJ](#) [OP07EP](#) [OP07EP+](#) [OP07EZ](#) [OP07Z](#) [OP07AC/D](#) [OP07C/D](#) [OP07AJ](#) [OP07D/D](#) [OP07DJ](#)
[OP07J](#)