

# 1:4 Clock Distribution Chip

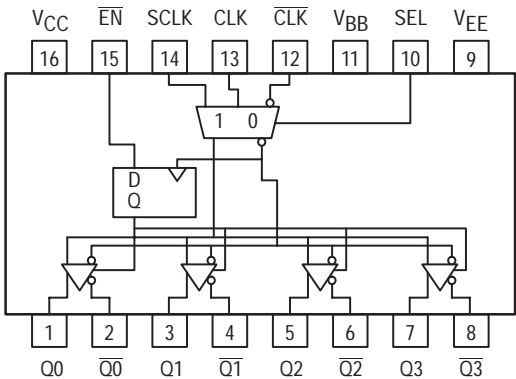
The MC10EL100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the  $V_{BB}$  output should be connected to the  $\overline{CLK}$  input and bypassed to ground via a  $0.01\mu F$  capacitor. The  $V_{BB}$  output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

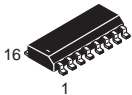
The common enable ( $\overline{EN}$ ) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- 75k $\Omega$  Internal Input Pulldown Resistors
- >1000V ESD Protection

## LOGIC DIAGRAM AND PINOUT ASSIGNMENT



# MC10EL15 MC100EL15



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05

## PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
SCLK	Scan Clock Input
$\overline{EN}$	Sync Enable
SEL	Clock Select Input
$V_{BB}$	Reference Output
Q0-3	Diff Clock Outputs

## FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\* On next negative transition of CLK or SCLK



**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Symbol	Characteristic	Rating	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0V$ )	-8.0 to 0	VDC
$V_I$	Input Voltage ( $V_{CC} = 0V$ )	0 to -6.0	VDC
$I_{out}$	Output Current      Continuous Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$V_{EE}$	Operating Range <sup>1,2</sup>	-5.7 to -4.2	V

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.

2. Parametric values specified at:    100EL Series:    -4.20V to -5.50V  
   10EL Series:    -4.94V to -5.50V

**10EL SERIES****DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min}) - V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}$ <sup>1</sup>)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage	-1080	-890	-1020	-840	-980	-810	-910	-720	mV
$V_{OL}$	Output LOW Voltage	-1950	-1650	-1950	-1630	-1950	-1630	-1950	-1595	mV
$V_{IH}$	Input HIGH Voltage	-1230	-890	-1170	-840	-1130	-810	-1060	-720	mV
$V_{IL}$	Input LOW Voltage	-1950	-1500	-1950	-1480	-1950	-1480	-1950	-1445	mV
$I_{IL}$	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	μA

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0V except where otherwise specified on the individual data sheets.

**100EL SERIES****DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min}) - V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}$ <sup>1</sup>)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
$V_{OH}$	Output HIGH Voltage	-1085	-1005	-880	-1025	-955	-880	mV	$V_{IN} = V_{IH}(\text{max})$ or $V_{IL}(\text{min})$
$V_{OL}$	Output LOW Voltage	-1830	-1695	-1555	-1810	-1705	-1620	mV	
$V_{OHA}$	Output HIGH Voltage	-1095	—	—	-1035	—	—	mV	$V_{IN} = V_{IH}(\text{max})$ or $V_{IL}(\text{min})$
$V_{OLA}$	Output LOW Voltage	—	—	-1555	—	—	-1610	mV	
$V_{IH}$	Input HIGH Voltage	-1165	—	-880	-1165	—	-880	mV	
$V_{IL}$	Input LOW Voltage	-1810	—	-1475	-1810	—	-1475	mV	
$I_{IL}$	Input LOW Current	0.5	—	—	0.5	—	—	μA	$V_{IN} = V_{IL}(\text{max})$

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at  $V_{EE} = -4.5V$  now apply across the full  $V_{EE}$  range of -4.2V to -5.5V. Outputs are terminated through a 50Ω resistor to -2.0V except where otherwise specified on the individual data sheets.

**AC/DC CHARACTERISTICS** ( $V_{EE} = V_{EE(min)}$  to  $V_{EE(max)}$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current 10EL 100EL		25 25	35 35		25 25	35 35		25 25	35 35		25 25	35 38	mA
$V_{BB}$	Output Reference Voltage 10EL 100EL	-1.43 -1.38		-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V
$I_{IH}$	Input High Current			150			150			150			150	μA
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	460 410 410		660 710 710	470 420 420		610 720 720	470 420 420		610 720 720	500 450 470		700 750 750	ps
$t_{SKEW}$	Part-to-Part Skew Within-Device Skew <sup>1</sup>			200 50			200 50			200 50			200 50	ps
$t_S$	Setup Time $\overline{EN}$	150			150			150			150			ps
$t_H$	HoldTime $\overline{EN}$	400			400			400			400			ps
$V_{PP}$	Minimum Input Swing CLK <sup>2</sup>	250			250			250			250			mV
$V_{CMR}$	Common Mode Range CLK <sup>3</sup>	-2.0		-0.4	-2.0		-0.4	-2.0		-0.4	-2.0		-0.4	V
$t_r$ $t_f$	Output Rise/Fall Times Q (20% – 80%)				325		575	325		575	325		575	ps

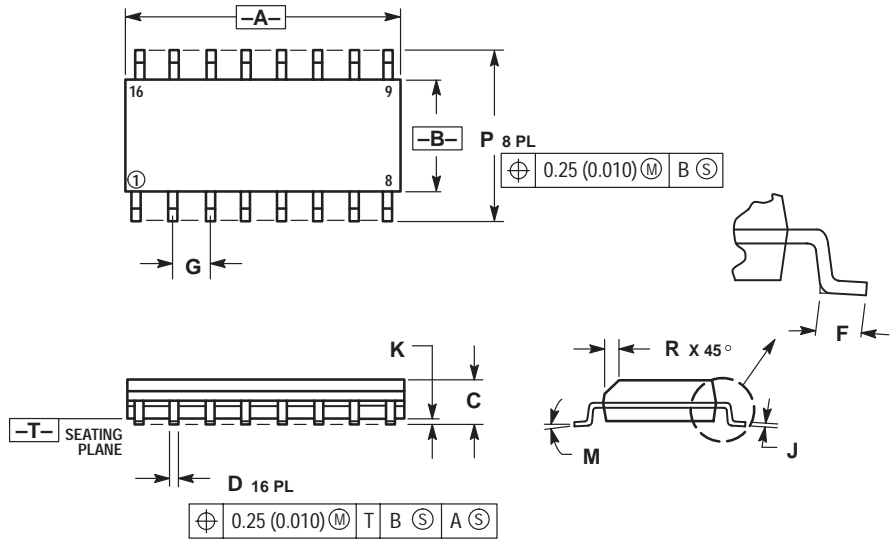
1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.

2. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1V. The lower end of the CMR range is dependent on  $V_{EE}$  and is equal to  $V_{EE} + 2.5V$ .


OUTLINE DIMENSIONS

D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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