

2SK3723

N-channel enhancement mode MOSFET

■ Features

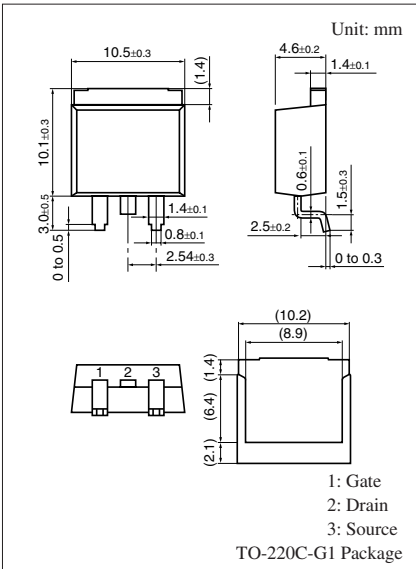
- Low on-resistance, low Q_g
- High avalanche resistance

■ Applications

- For PDP
- For high-speed switching

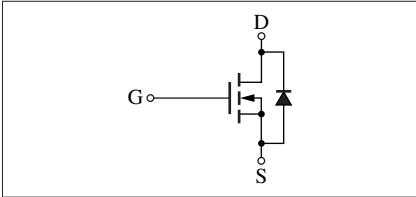
■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V _{DSS}	150	V
Gate-source surrender voltage	V _{GSS}	±30	V
Drain current	I _D	30	A
Peak drain current	I _{DP}	120	A
Power dissipation	P _D	50	W
		3	
T _a = 25°C			
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	−55 to +150	°C



Marking Symbol: K3723

Internal Connection



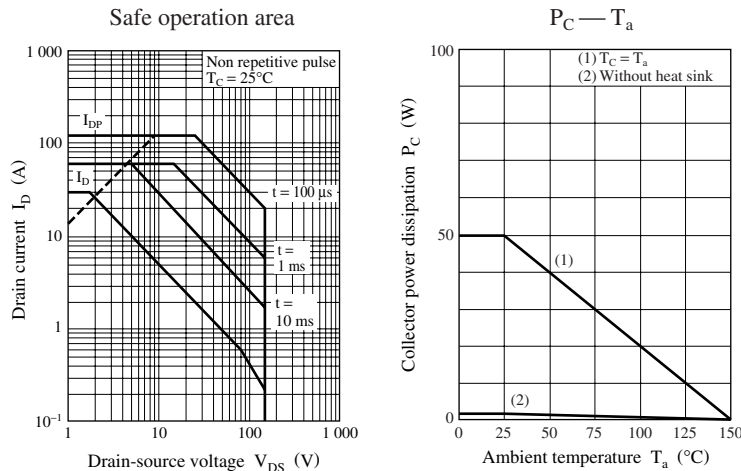
■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	150			V
Gate threshold voltage	V_{th}	$V_{DS} = 25 \text{ V}$, $I_D = 1 \text{ mA}$	2		4	V
Drain-source cutoff current	I_{DSS}	$V_{DS} = 120 \text{ V}$, $V_{GS} = 0$			100	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$			± 1	μA
Drain-source ON resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		33	42	$\text{m}\Omega$
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 25 \text{ V}$, $I_D = 15 \text{ A}$	8	18		S
Short-circuit forward transfer capacitance (Common-source)	C_{iss}	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$		2900		pF
Short-circuit output capacitance (Common-source)	C_{oss}			618		pF
Reverse transfer capacitance (Common-source)	C_{rss}			91		pF
Turn-on delay time	$t_{d(on)}$	$V_{DD} \approx 100 \text{ V}$, $I_D = 15 \text{ A}$ $R_L = 6.7 \Omega$, $V_{GS} = 10 \text{ V}$		32		ns
Rise time	T_r			46		ns
Turn-off delay time	$t_{d(off)}$			227		ns
Fall time	t_f			66		ns

■ Electrical Characteristics (continued) $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode forward voltage	V_{DSF}	$I_{DR} = 30\text{ A}$, $V_{GS} = 0$			-1.5	V
Reverse recovery time	t_{rr}	$L = 230\text{ }\mu\text{H}$, $V_{DD} = 100\text{ V}$ $I_{DR} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		130		ns
Reverse recovery charge	Q_{rr}			533		nC
Gate charge load	Q_g	$V_{DD} = 100\text{ V}$, $I_D = 15\text{ A}$ $V_{GS} = 10\text{ V}$		55.4		nC
Gate-source charge	Q_{gs}			9.1		nC
Gate-drain charge	Q_{gd}			22.4		nC
Thermal resistance (ch-c)	$R_{th(ch-c)}$				2.5	$^\circ\text{C}/\text{W}$
Thermal resistance (ch-a)	$R_{th(ch-a)}$				89.2	$^\circ\text{C}/\text{W}$

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.



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