PRELIMINARY

2V Operation Clock-less Switching Driver for Class D Amplifier

■ GENERAL DESCRIPTION

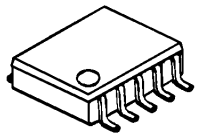
The **NJU8710** is a 2V operation clock-less switching driver for a class D Amplifier with separated power supply between Input and Output.

The **NJU8710** provides powerful drivability in both of sink and source without flow-through current. Therefore, it can be used to the buffer or the switch as a driver IC.

Furthermore it converts 1bit digital signal input, such as PWM or PDM signal, to analog signal output of the hi-fi audio level through a simple external LC low-pass filter.

The **NJU8710** realizes very high power-efficiency because of the class D operation and low voltage operation. Therefore, it is suitable for battery powered applications and others.

■ PACKAGE OUTLINE

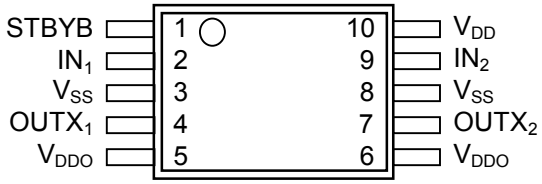


NJU8710R

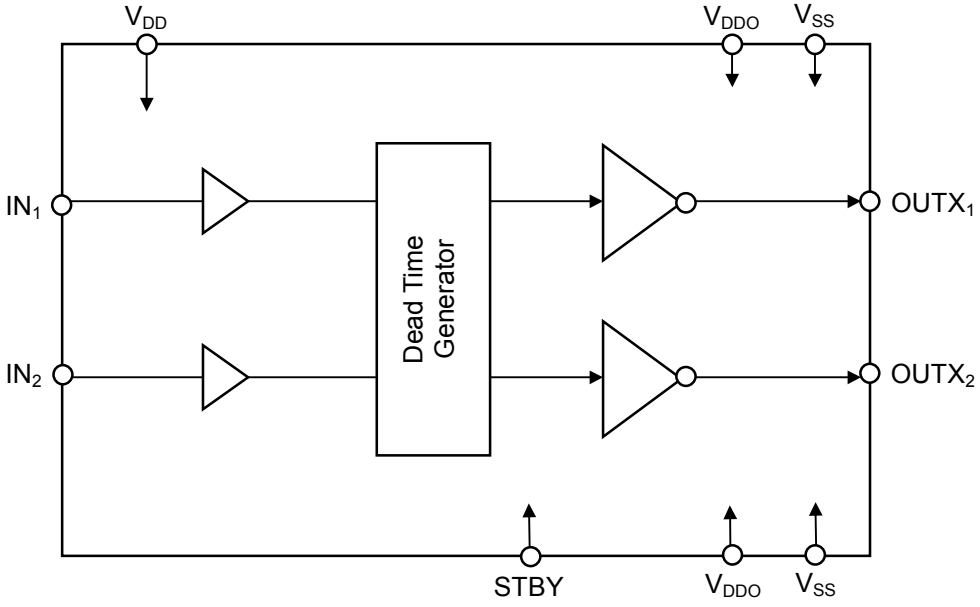
■ FEATURES

- 2-channel 1bit Digital Signal Input
- Standby(Hi-Z) Control function
- Operating Voltage : 1.7V to 2.7V
- Driving Voltage : 1.7V to V_{DD}
- CMOS Technology
- Package Outline : VSP10

■ PIN CONFIGURATION



■ BLOCK DIAGRAM

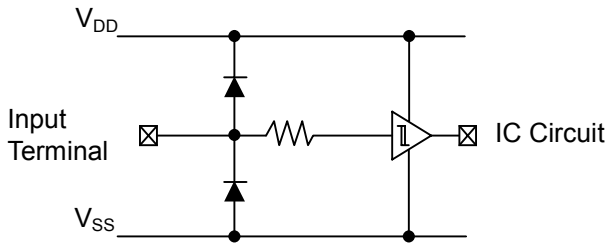


■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
10	V_{DD}	–	Power Supply: V_{DD}=2V
5 6	V_{DDO}	–	Output Power Supply: V_{DDO}=2V
3 8	V_{SS}	–	Power GND and Output GND terminal: V_{SS}=0V
2 9	IN_1 IN_2	I	1-bit Data Input Terminal
4 7	$OUTX_1$ $OUTX_2$	O	Output Terminal $OUTX_1$ terminal outputs the inverted signal of IN_1 terminal, $OUTX_2$ terminal outputs the inverted signal of IN_2 terminal.
1	STBYB	I	Standby Control Terminal (L:Standby)

*V_{SS}(Terminal No.3,8) should be connected at a nearest point to the IC.
*V_{DDO}(Terminal No.5,6) should be connected at a nearest point to the IC.
*STBYB(Terminal No.1) must be connected to V_{DD}, when this function is not used.

■ INPUT TERMINAL STRUCTURE



■ FUNCTIONAL DESCRIPTION

(1) Signal Output ($OUTX_1$, $OUTX_2$ Terminal)

Output signal becomes a inverted input signal. A flow-through current at the signal polarity transition doesn't generate by optimized dead time control circuit. Output signal is converted to analog signal via external 2nd-order or higher LC filter.

A switching regulator with a high response against a voltage fluctuation is the best selection for the $V_{DDO,}$ which is the power supply for output drivers. To obtain better T.H.D. performance, the stabilization of the power is required.

(2) Standby Control Function

By setting the STBYB terminal to “L”, the **NJU8710** becomes standby condition. During standby condition, $OUTX_1$ and $OUTX_2$ are in Hi-Z.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	-0.3 to +4.0	V
		V_{DDO}	-0.3 to +2.7	V
Input Voltage		Vin	-0.3 to V_{DD}+0.3	V
Operating Temperature		Topr	-40 to +85	°C
Storage Temperature		Tstg	-40 to +125	°C
Power Dissipation	VSP10	P_D	450*	mW
Power Supply Voltage Condition		-	$V_{DD} \geq V_{DDO}$	V

* : Mounted on two-layer board of based on the JEDEC.

Note 1) All voltage values are specified as V_{SS}=0V.

Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 3) De-coupling capacitors should be connected between V_{DD}-V_{SS} and V_{DDO}-V_{SS} due to the stabilized operation.

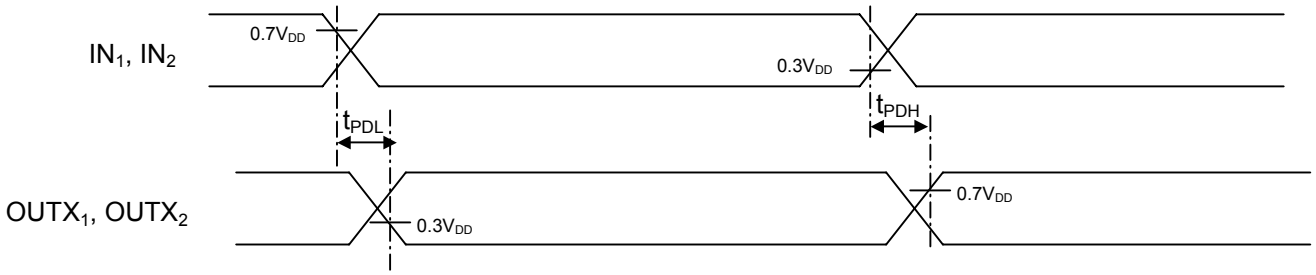
■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} Supply Voltage	V_{DD}		1.7	2.0	2.7	V
V_{DDO} Supply Voltage	V_{DDO}		1.7	2.0	V_{DD}	V
Output Driver High side Resistance	R_H	V_{OUT}=V_{DDO}-0.1V	-	1.5	2	Ω
Output Driver Low side Resistance	R_L	V_{OUT}=0.1V	-	1.5	2	Ω
Operating Current at Hi-Z Output	I_{ST}	IN_1, IN_2, STBYB="L"	-	-	1	μA
Operating Current at no input signal	I_{DD}	No-load operating, IN_1=IN_2=1.4MHz	-	0.05	T.B.D	mA
	I_{DDO}		-	0.6	T.B.D	
Input Voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
Input Leakage Current	I_{LK}		-	-	±1	μA

■ TIMING CHARACTERISTICS

- Signal Spread Characteristics



(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=0.0V unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Maximum Operating Frequency	f_{Max}		-	-	25	MHz
Signal Spread Time (H → L)	t_{PDL}		-	-	20	ns
Signal Spread Time (L→ H)	t_{PDH}		-	-	20	ns

- Output Control Signal Input (STBYB)

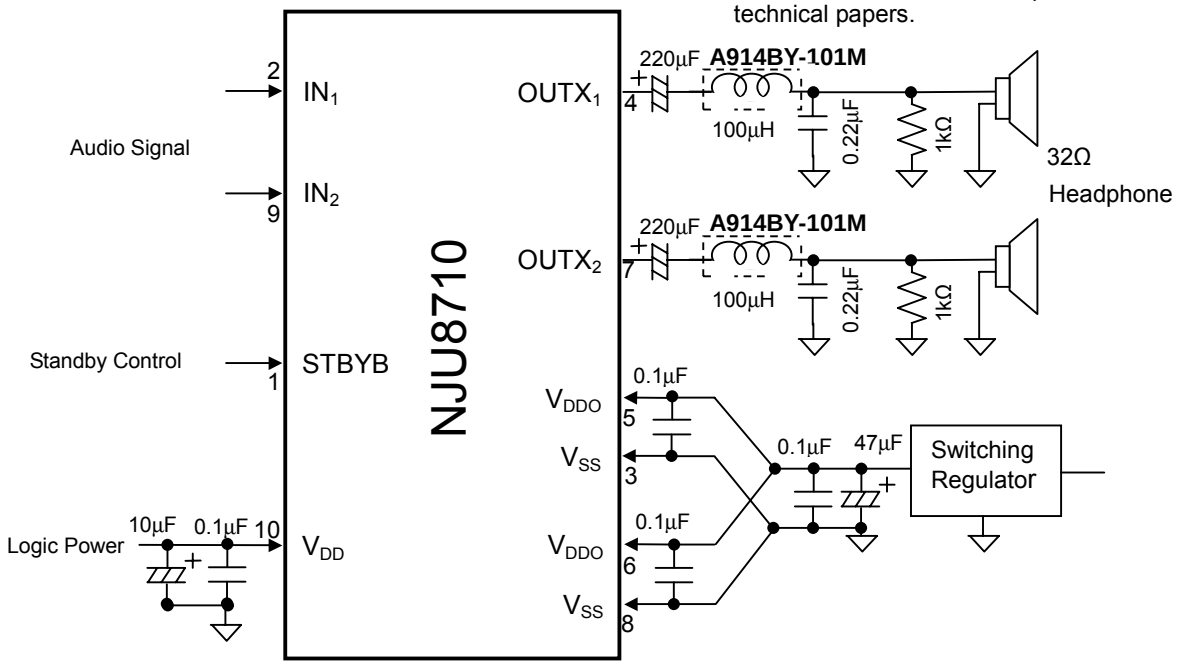
(Ta=25°C, V_{DD}=V_{DDO}=2.0V, V_{SS}=0.0V unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	t_{UP}		-	-	50	ns
Fall Time	t_{DN}		-	-	50	ns

■ APPLICATION CIRCUIT (Analog Signal Output)

- Stereo OTL application example

• A914BY-101M is manufactured by TOKO, INC. For further information, please refer to its technical papers.



- Monaural BTL application example

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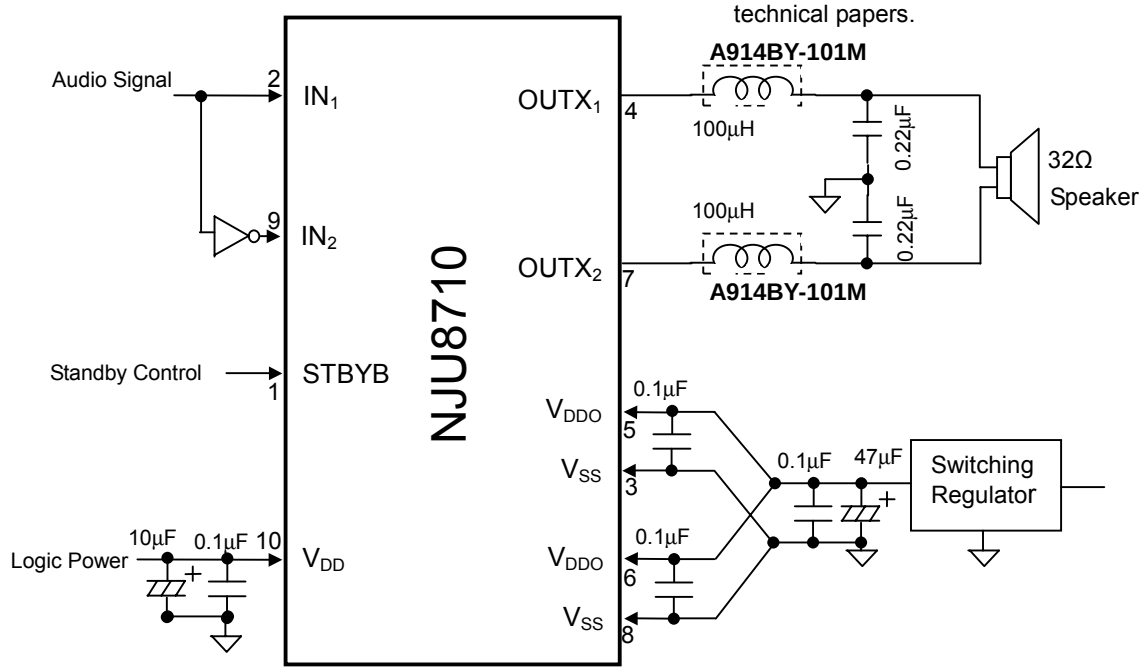

Note 4) De-coupling capacitors must be connected between each power supply terminal and GND terminal.
Note 5) The power supply for V_{DDO} requires fast driving response performance such as a switching regulator for T.H.D..
Note 6) The bigger capacitor value of external AC-coupling capacitors realize better low frequency response characteristics. In addition, ESR(Equivalent Series Resistance) should be low.
Note 7) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

[CAUTION]
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