PRELIMINARY DATA SHEET

SKY77155: System Smart™ PA Module for CDMA / PCS (1750–1780 MHz)

Applications

- Personal Communications Services (PCS)
- Full Korean PCS coverage
- Wireless local loop (WLL)

Features

- Low voltage positive bias supply
  - 3.2 V to 4.2 V
- Low V_{REF}
  - 2.85 V, nominal
- Low I_{REF}
  - less than 1 mA
- Good linearity
- High efficiency
- Large dynamic range
- 8-pin package
  - 3 x 3 x 1.2 mm
- Power down control
- Dynamic bias control
- InGaP
- IS95/CDMA2000/EVDO

Description

The SKY77155 System Smart™ Power Amplifier Module (PAM) is a fully matched 8-pin surface mount module developed for Code Division Multiple Access (CDMA) / Personal Communications Service (PCS) and Wireless Local Loop (WLL) applications. This small and efficient module packs full 1750–1780 MHz bandwidth coverage into a single compact package. The SKY77155 meets the stringent spectral linearity requirements of Code Division Multiple Access (CDMA) PCS transmission, with high power added efficiency for power output of up to 28 dBm. A low current pin (VCONT) is provided to improve efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. The output match is realized off-chip within the module package to optimize efficiency and power performance into a 50-ohm load. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the SKY77155 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with an output in the 3.2 to 4.2 volt range. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

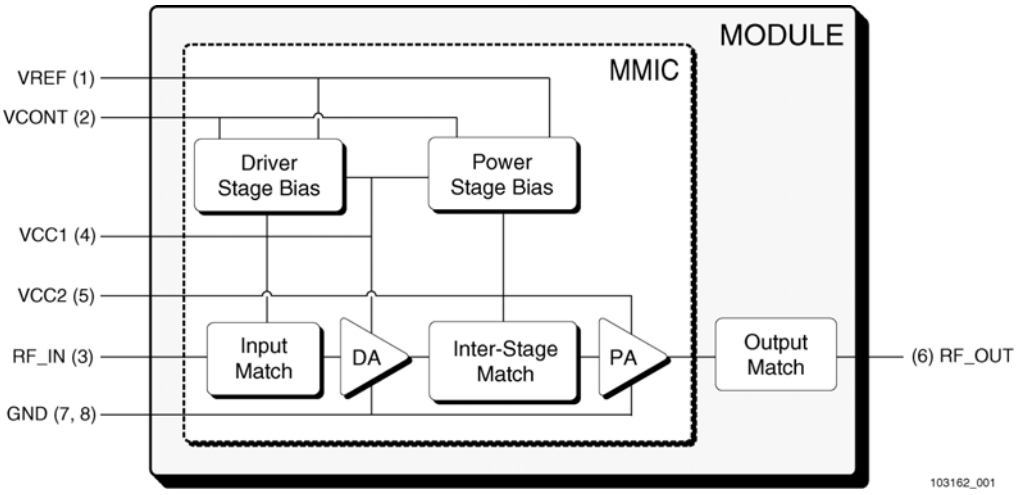


Figure 1. SKY77155 Functional Block Diagram

Preliminary Electrical Target Specifications

The following tables list the electrical characteristics of the SKY77155 Power Amplifier. Table 1 lists the absolute maximum ratings, while Table 2 shows the recommended operating conditions to achieve the performance characteristics listed in Table 4. Table 3 presents a truth table for the power settings.

Table 1. Absolute Maximum Ratings [1]

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	P_{IN}	—	1.0	6.0	dBm
Supply Voltage	V_{CC}	—	3.4	6.0	Volts
Reference Voltage	V_{REF}	—	2.85	3.0	Volts
Case Operating Temperature [2]	T_C	–30	25	+110	°C
Case Storage Temperature	T_{STG}	–55	—	+125	°C

[1] No damage assuming only one parameter is set at limit at a time with all other parameters set at nominal value.

[2] Case Operating Temperature refers to the temperature of the GROUND PAD on the underside of the package.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Power Output		P_O			28.0	dBm
Supply Voltage		V_{CC}	3.2	3.4	4.2	Volts
Reference Voltage		V_{REF}	2.75	2.85	2.95	Volts
Operating Frequency		F_O	1750.0	1765.0	1780.0	MHz
Control Voltage	Low Power	V_{CONT}	0.0	1.25		Volts
	High Power	V_{CONT}		2.0	2.5	
Case Operating Temperature [1]		T_C	–30	+25	+85	°C

[1] Case Operating Temperature refers to the temperature of the GROUND PAD on the underside of the package.

Table 3. Power Range Truth Table

Power Mode	V_{REF}	V_{CONT}	Range [1]
High Power	2.85 V	2.0 V	28 dBm
Low Power	2.85 V	< 1.3 V	≤ 0 dBm
Shut Down	0.0 V	0.0 V	—

[1] In the output power range between –10 dBm and 28 dBm, V_{CONT} can be continuously adjusted to minimize current consumption while meeting required linearity specification.

Table 4. Electrical Specifications for CDMA Nominal Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain conditions		G_{LOW}	V_{CONT} = 1.25 V $P_O \leq 0$ dBm	21.0	24.5	26.0	dB
		G_{MID}	V_{CONT} = 1.55 V $0 \geq PO \leq 16$ dBm	26.0	28.5	30.0	
		G_{HIGH}	V_{CONT} = 2.0 V P_O = 28 dBm	27.0	29.0	30.5	
Gain Sensitivity		G_{SEN}	All conditions fixed except V_{CONT}	5	10	15	dB/Volt
Power Added Efficiency		PAE_{MID}	V_{CONT} = 1.55 V P_O = 16 dBm	8	9	—	%
		PAE_{HIGH}	$V_{CONT} \geq$ 2.0 V P_O = 28 dBm	37	40	—	
Total Supply Current		I_{CC_LOW}	P_O = 0 dBm	—	40	65	mA
		I_{CC_HIGH}	P_O = 28 dBm	—	455	500	
Quiescent Current		I_{Q_LOW}	V_{CONT} = 1.25 V	25	30	45	mA
		I_{Q_HIGH}	V_{CONT} = 2.0 V	65	85	110	
Reference Current		I_{REF}		—	1.0	2.0	mA
Control Current		I_{CTRL}	V_{CONT} = 2.0 V	—	100	250	µA
Total Supply Current in Power-down Mode		I_{PD}	V_{CC} = 3.4 V V_{CONT} = 0.0 V V_{REF} = 0.0 V	—	3.0	5.0	µA
Adjacent Channel Power [2][3]	1.25 MHz offset	$ACP1_{LOW}$	V_{CONT} = 1.25 V $P_O \leq 0$ dBm	—	–56.0	–48.0	dBc
		$ACP1_{HIGH}$	$V_{CONT} \geq$ 2.0 V $P_O \leq$ 28 dBm	—	–50.0	–47.5	
	2.25 MHz offset	$ACP3_{LOW}$	V_{CONT} = 1.25 V $P_O \leq 0$ dBm	—	–80.0	–58.0	
		$ACP3_{HIGH}$	$V_{CONT} \geq$ 2.0 V $P_O \leq$ 28 dBm	—	–59.0	–57.5	
Harmonic Suppression	Second	F_O2	$P_O \leq$ 28 dBm	—	–62	–35	dBc
	Third	F_O3	$P_O \leq$ 28 dBm	—	–43	–40	
Noise Power in RX Band 1840–1870 MHz		RxBN	$P_O \leq$ 28 dBm	—	–138.0		dBm/Hz
Noise Figure		NF	—	—	4.0		dB
Input Voltage Standing Wave Ratio (VSWR)		VSWR	—	—	—	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR All phases	—	—	–70.0	dBc
Ruggedness [4]		Ru	$P_O \leq$ 28 dBm	10:1	—		VSWR
Turn On Time [5]	DC	$T_{ON}DC$		—	40		µs
	RF	$T_{ON}RF$		—	5		
Turn Off Time [5]	DC	$T_{OFF}DC$		—	40		µs
	RF	$T_{OFF}RF$		—	5		

[1] Per Table 2 over dynamic range up to 28 dBm output power, unless otherwise specified

[2] ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[3] For CDMA2000 test configured as [PCH @ –3.75 dB, DCCH–9600 bps @ 0 dB; SCHO–9600 bps @ 0 dB] and other test configurations that yield a peak-to-average up to 4.5 dB for CCDF = 1%, up to 1. dB power back off from the maximum listed for IS95 may be required to meet specified maximum ACP performance under worst-case conditions.

[4] All phases, time = 10 seconds.

[5] $T_{ON}DC$ is time required to reach stable quiescent bias (±10%) after V_{REF} is switched high.
$T_{OFF}DC$ is time required for battery to decrease to < 100 µA after V_{REF} is switched low.
After I_{CQ} is stable, the $T_{ON}RF$ is time to reach final output power (±1 dB) once RF input is applied.
$T_{OFF}RF$ is time required for P_O to drop 30 dB once RF input is removed.

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the SKY77155, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 2 shows the basic schematic of the board for the 1750 MHz to 1780 MHz range.

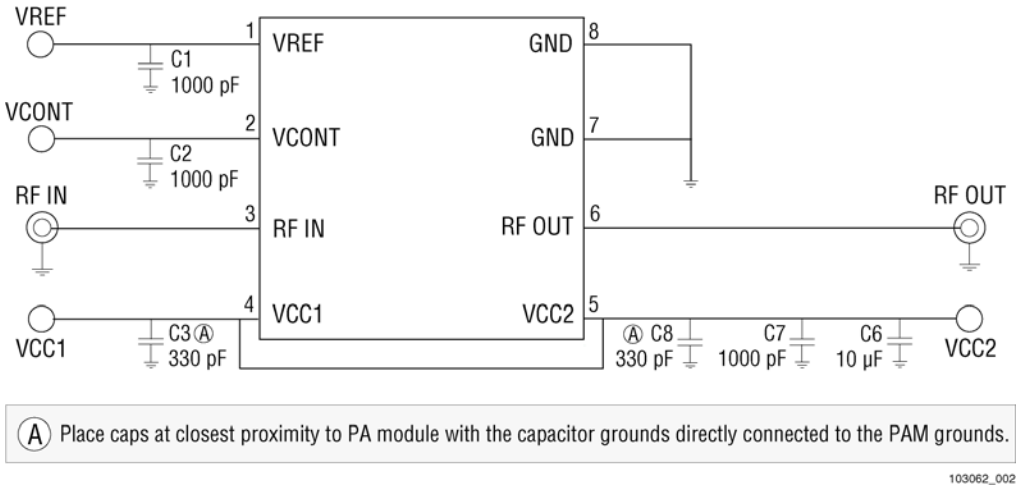


Figure 2. SKY77155 Evaluation Board Schematic

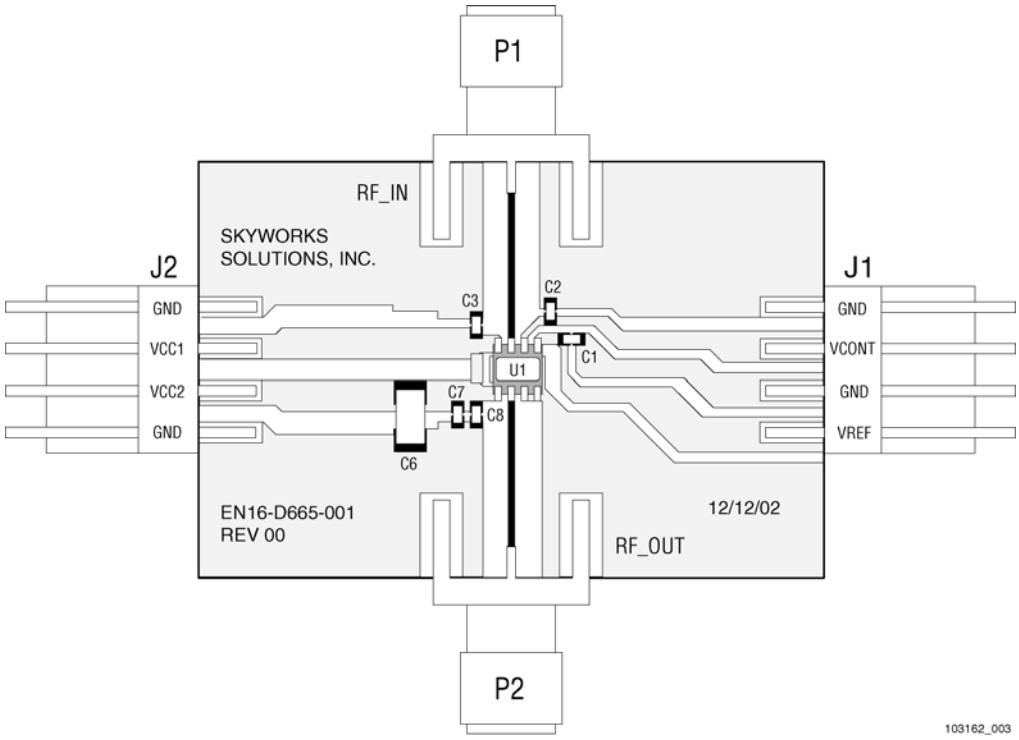
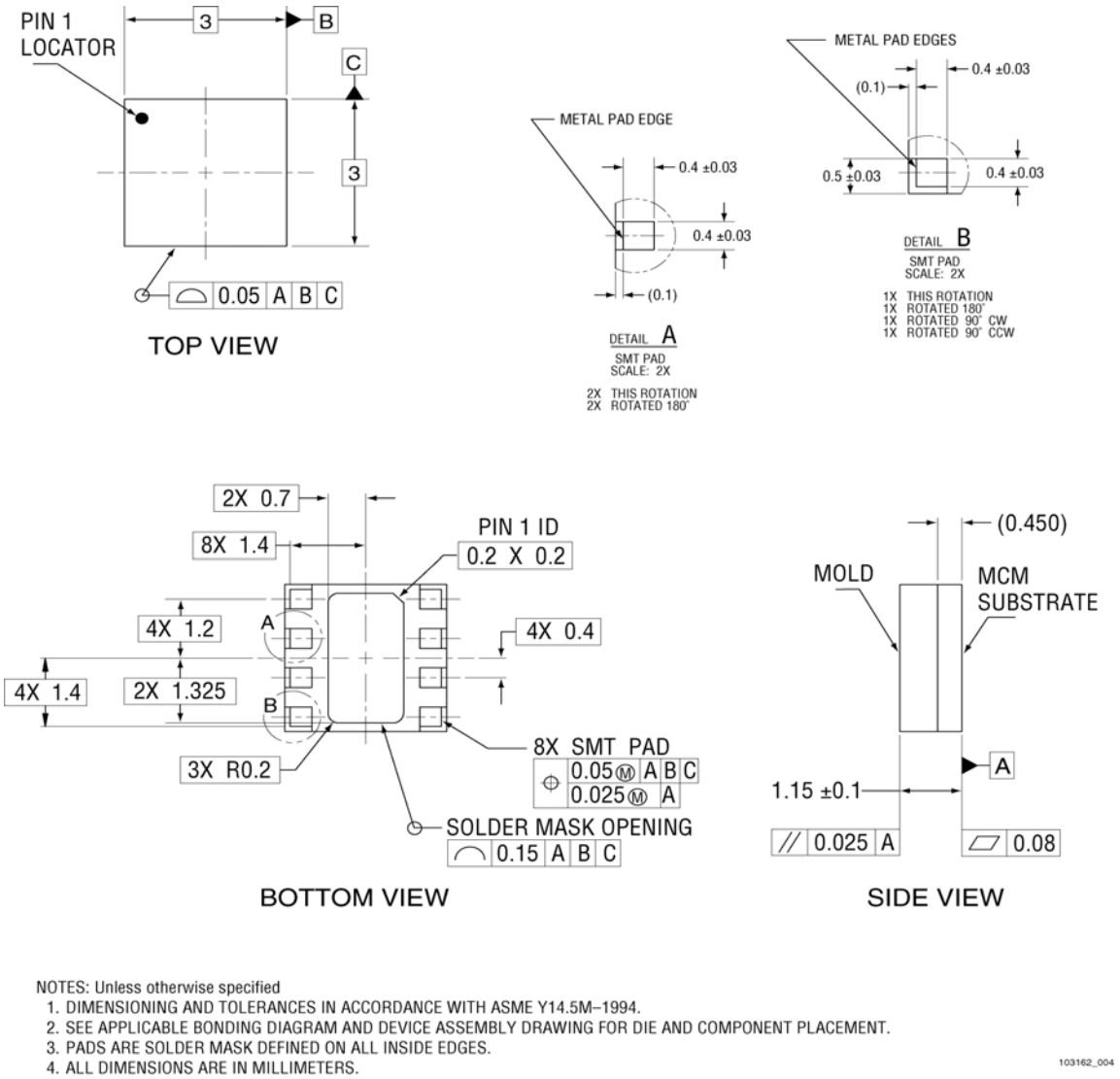


Figure 3. SKY77155 Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions

The SKY77155 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 4 is a mechanical drawing of the pad layout for this package.

Figure 5 shows the pin functions and the pin numbering convention, which starts with pin 1 in the upper left and increments counter-clockwise around the package. Figure 6 illustrates typical case markings.



NOTES: Unless otherwise specified
1. DIMENSIONING AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M–1994.
2. SEE APPLICABLE BONDING DIAGRAM AND DEVICE ASSEMBLY DRAWING FOR DIE AND COMPONENT PLACEMENT.
3. PADS ARE SOLDER MASK DEFINED ON ALL INSIDE EDGES.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

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Figure 4. SKY77155 Package Drawing

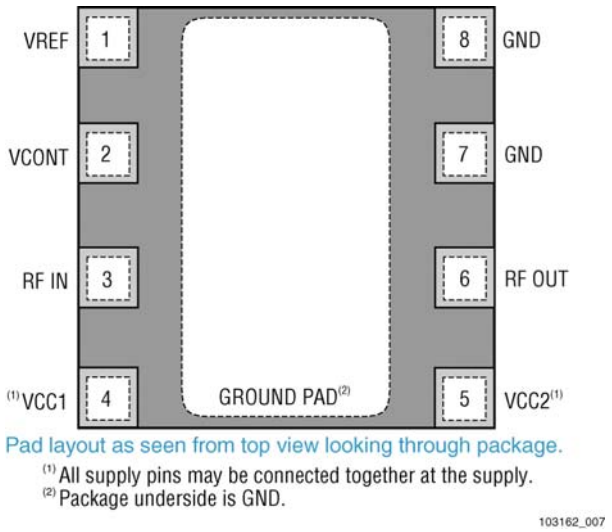

Figure 5. SKY77155 Pin Configuration and Pin Names (Top View)

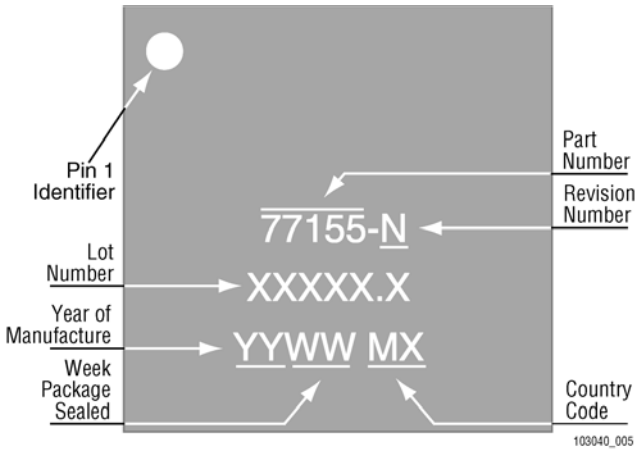

Figure 6. Typical 3x3 Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77155 is capable of withstanding an MSL3/250 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 250 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 250 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Skyworks' Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD–020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Skyworks' Application Note: Tape and Reel, Document Number 101568*.

Electrostatic Discharge Sensitivity

The SKY77155 is a Class 2 device. Figure 7 lists the Electrostatic Discharge (ESD) immunity level for each pin of the SKY77155 product. The numbers in Figure 7 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation.

The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after "the pin fails the electrical specification limits" or "the pin becomes completely non-functional". Skyworks employs most stringent criteria and fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 5.

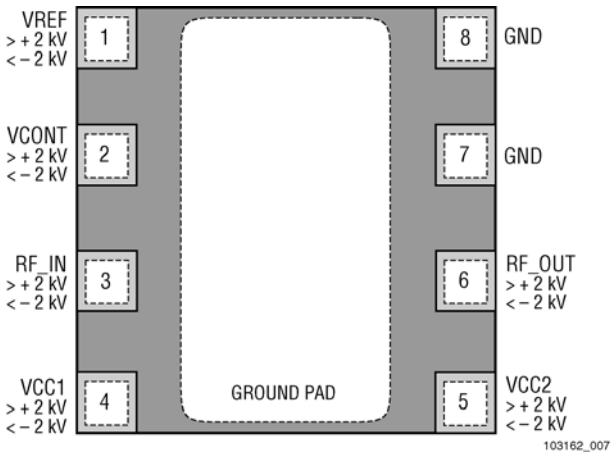

Figure 7. ESD Sentivity Areas

Table 5. Precautions for Handling GaAs IC-based Products to Avoid Induced Damage

Personnel Grounding	Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges
Facility	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Packaging & Transportation	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders
Protective Workstation	Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
SKY77155	SKY77155	–13	3x3LM–10	–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
P1		August 4, 2003	Advance Information
P2		March 18, 2004	Revise: Op. Freq., Tables 2, 4, Figure 6
P3		May 17, 2004	Revise: Tables 2, 4, Figure 7

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Application Note: Tape and Reel, Document Number 101568

Standard SMT Reflow Profiles: JEDEC Standard J–STD–020