

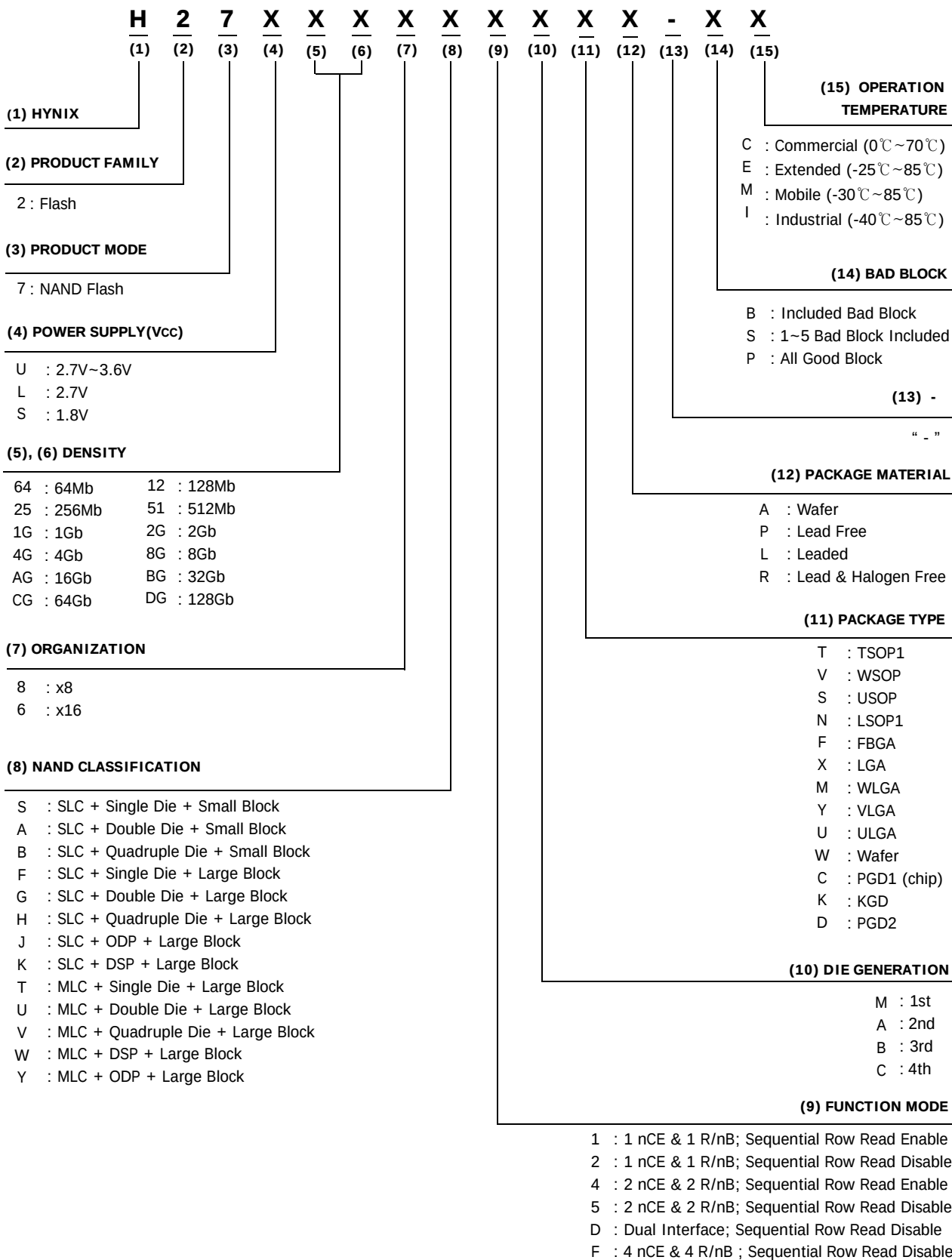
Part Number System Change Notice

Effective from August 6, 2007, a more concise part numbering system is utilized by Hynix with the intention of managing product line with more consistency. Devices developed after August 2007 and their respective products will be Refer to the following pages for more details. (www.hynix.com/pn_notice.jsp)

Part Number with prefix 'HY' -> [Old Part Number Decoder Link](#)

Part Number with prefix 'H' -> [New Part Number Decoder Link](#)

NAND Flash PART NUMBERING



NAND Flash PART NUMBERING

HY	XX	X	X	XX	XX	X	X	-	X	(X)	(X)	(X)	(X)
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	
(1) HYNIX MEMORY													
(2) COMPONENT GROUP													
27 : NAND Flash													
(3) POWER SUPPLY(Vcc)													
U : 2.7V~3.6V													
L : 2.7V													
S : 1.8V													
(4) CLASSIFICATION													
S : SLC + Single Die + S/B													
A : SLC + Double Die + S/B													
B : SLC + Quadruple Die + S/B													
F : SLC + Single Die + L/B													
G : SLC + Double Die + L/B													
H : SLC + Quadruple Die + L/B													
K : SLC + DSP + L/B													
T : MLC + Single Die + L/B													
U : MLC + Double Die + L/B													
V : MLC + Quadruple Die + L/B													
W : MLC + DSP + L/B													
(5) BIT ORGANIZATION													
08 : x8													
16 : x16													
32 : x32													
(6) DENSITY													
64 : 64Mb		28 : 128Mb											
56 : 256Mb		12 : 512Mb											
1G : 1Gb		2G : 2Gb											
4G : 4Gb		8G : 8Gb											
AG : 16Gb		BG : 32Gb											
CG : 64Gb		DG : 128Gb											
ZG : 48Gb													
(7) MODE													
1 : 1 nCE & 1 R/nB; Sequential Row Read Enable													
2 : 1 nCE & 1 R/nB; Sequential Row Read Disable													
4 : 2 nCE & 2 R/nB; Sequential Row Read Enable													
5 : 2 nCE & 2 R/nB; Sequential Row Read Disable													
6 : 1 nCE & 1 R/nB; Sequential Row Read Enable & Auto Read Page 0													
7 : 2 nCE & 2 R/nB; Sequential Row Read Enable & Auto Read Page 0													
8 : 1 nCE & 1 R/nB; Sequential Row Read Disable & Auto Read Page 0													
9 : 2 nCE & 2 R/nB; Sequential Row Read Disable & Auto Read Page 0													
D : Dual Interface; Sequential Row Read Disable													
F : 4 nCE & 4 R/nB ; Sequential Row Read Disable													
T : 3 nCE & 3 R/nB ; Sequential Row Read Disable													
											(13) OPTION(CUSTOMER)		
											Customer Initial Option		
											(12) BAD BLOCK		
											Blank : Wafer		
											B : Included Bad Block		
											S : 1~5 Bad Block		
											P : All Good Block		
											(11) OPERATING TEMPERATURE		
											Blank : Wafer, Chip		
											C : 0℃~70℃		
											E : -25℃~85℃		
											M : -30℃~85℃		
											I : -40℃~85℃		
											(10) PACKAGE MATERIAL		
											Blank : Normal, Wafer, Chip, KGD		
											P : Lead Free		
											H : Halogen Free		
											R : Lead & Halogen Free		
											(9) PACKAGE TYPE		
											T : TSOP1		
											V : WSOP		
											S : USOP		
											E : WELP		
											F : FBGA(63ball)		
											B : FBGA(107ball)		
											G : FBGA(149ball)		
											H : TBGA		
											U : ULGA		
											Y : VLGA		
											M : WLGA		
											W : Wafer		
											C : Chip		
											K : KGD		
											D : PGD2		
											(8) VERSION		
											M : 1st Gen.		
											A : 2nd Gen.		
											B : 3rd Gen.		
											C : 4th Gen.		
											1 : Down Density(1st)		
											2 : Down Density(2nd)		