

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
 - 20 ns
- Low active power
 - 660 mW (commercial)
- Low standby power
 - 110 mW (20 ns)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Available in Pb-free 24-pin Molded SOJ, non Pb-free 24-pin (300-Mil) Molded DIP

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), and active LOW Output Enable ($\overline{OE}$) and tri-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW.

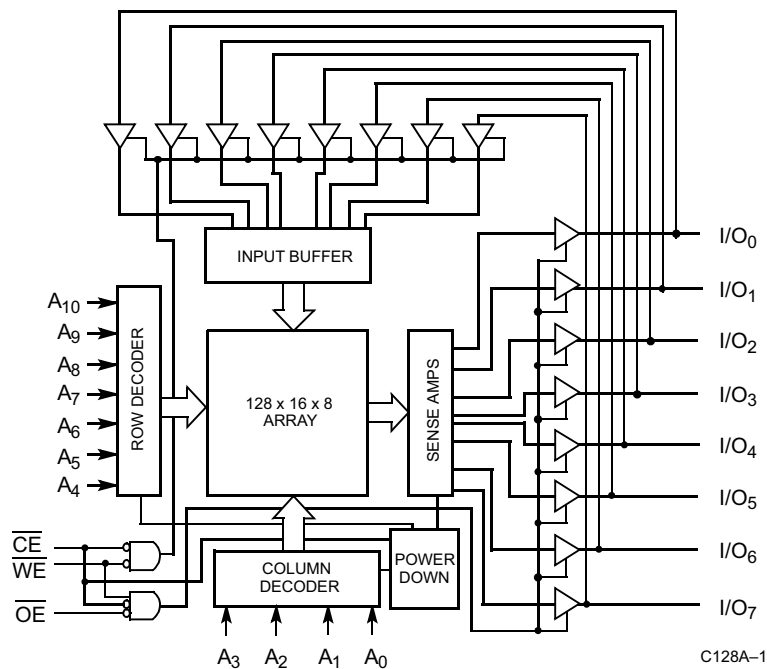
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when Chip Enable ($\overline{CE}$) or Output Enable ($\overline{OE}$) is HIGH or Write Enable ($\overline{WE}$) is LOW.

The CY7C128A utilizes a die coat to insure alpha immunity.

Logic Block Diagram

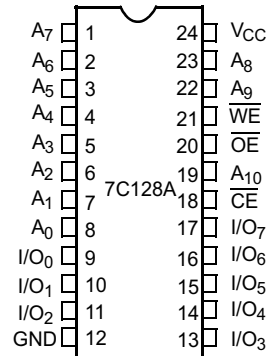


Selection Guide

Description	-20	-45
Maximum Access Time (ns)	20	45
Maximum Operating Current (mA)	120	120
Maximum CMOS Standby Current (mA)	20	20

Pin Configuration

Figure 1. 24-Pin DIP/SOJ (Top View)



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 28 to Pin 14) -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State -0.5V to +7.0V

DC Input Voltage -3.0V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	-20		-45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[3]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} Output Disabled	-10	+10	-10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA		120		120	mA
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		20	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

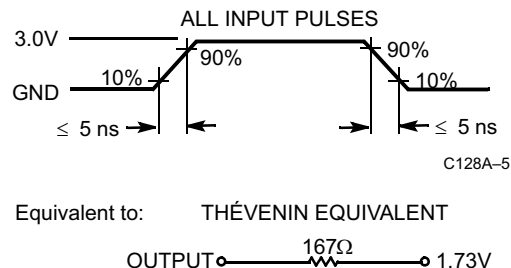
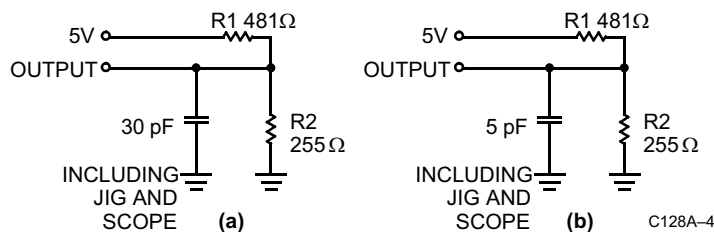
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^[2, 5]

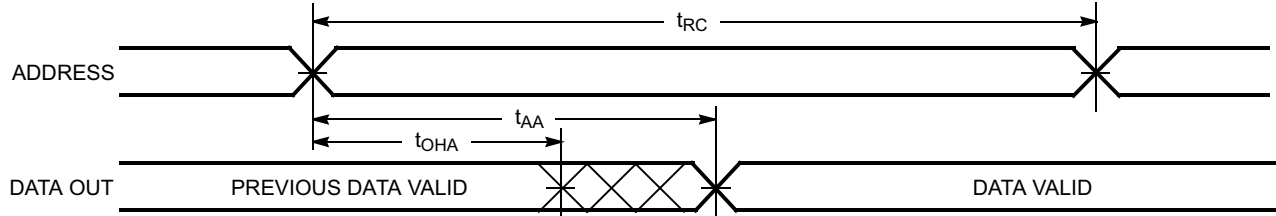
Parameter	Description	-20		-45		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	20		45		ns
t _{AA}	Address to Data Valid		20		45	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	CE LOW to Data Valid		20		45	ns
t _{DOE}	OE LOW to Data Valid		10		20	ns
t _{LZOE}	OE LOW to Low Z	3		3		ns
t _{HZOE}	OE HIGH to High Z ^[6]		8		15	ns
t _{LZCE}	CE LOW to Low Z ^[7]	5		5		ns
t _{HZCE}	CE HIGH to High Z ^[6, 7]		8		15	ns
t _{PU}	CE LOW to Power-Up	0		0		ns
t _{PD}	CE HIGH to Power-Down		20		25	ns
WRITE CYCLE ^[8]						
t _{WC}	Write Cycle Time	20		40		ns
t _{SCE}	CE LOW to Write End	15		30		ns
t _{AW}	Address Set-Up to Write End	15		30		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	15		20		ns
t _{SD}	Data Set-Up to Write End	10		15		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	WE LOW to High Z ^[6]		7		15	ns
t _{LZWE}	WE HIGH to Low Z	5		5		ns

Notes:

- Tested initially and after any design or process changes that may affect these parameters
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5\text{ pF}$ as in part (b) of AC Test Loads. Transition is measured $\pm 500\text{ mV}$ from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

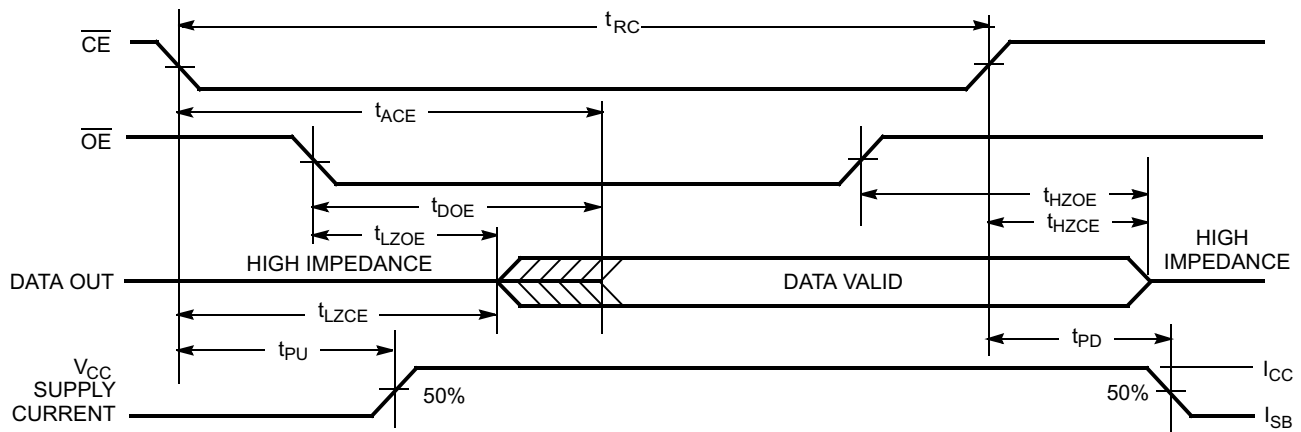
Switching Waveforms

Read Cycle No. 1^[9, 10]



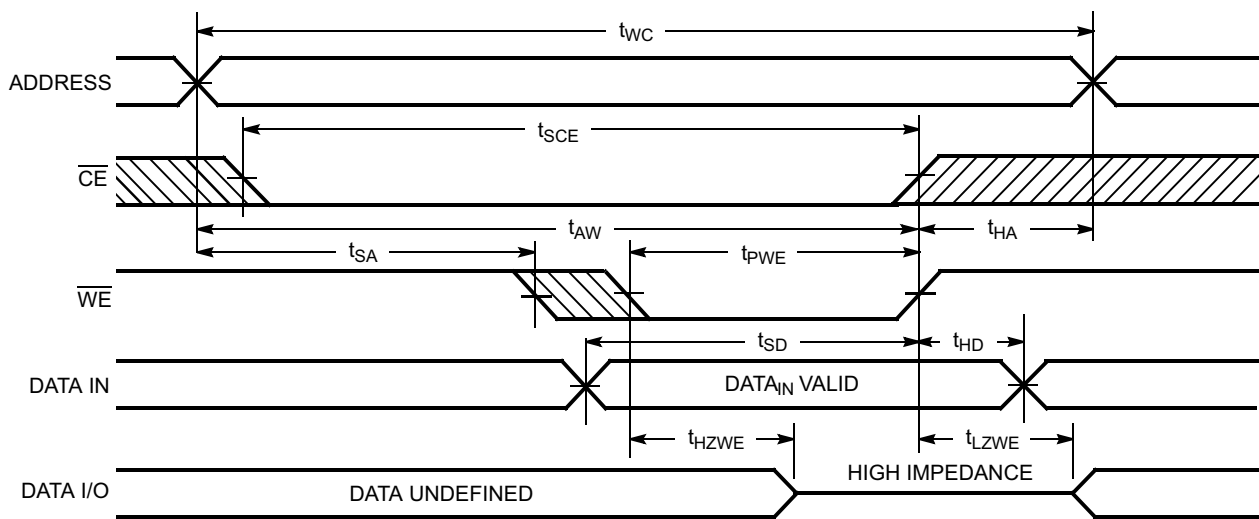
C128A-6

Read Cycle No. 2^[9, 11]



C128A-7

Write Cycle No. 1 (WE Controlled)^[8]



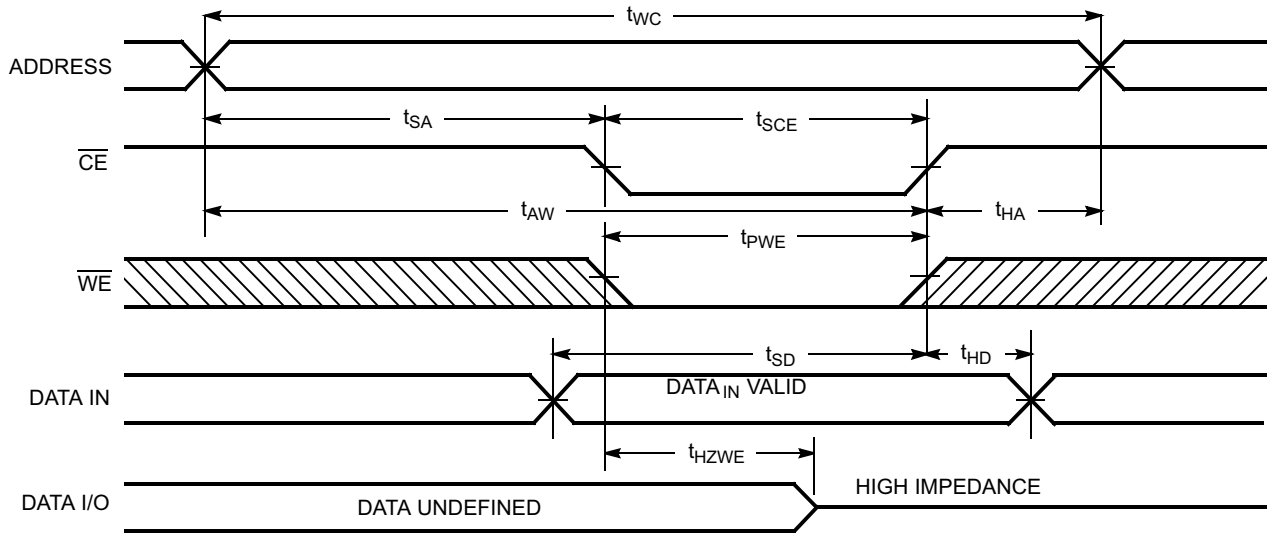
C128A-8

Notes:

9. WE is HIGH for read cycle.
10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[8, 12, 13]

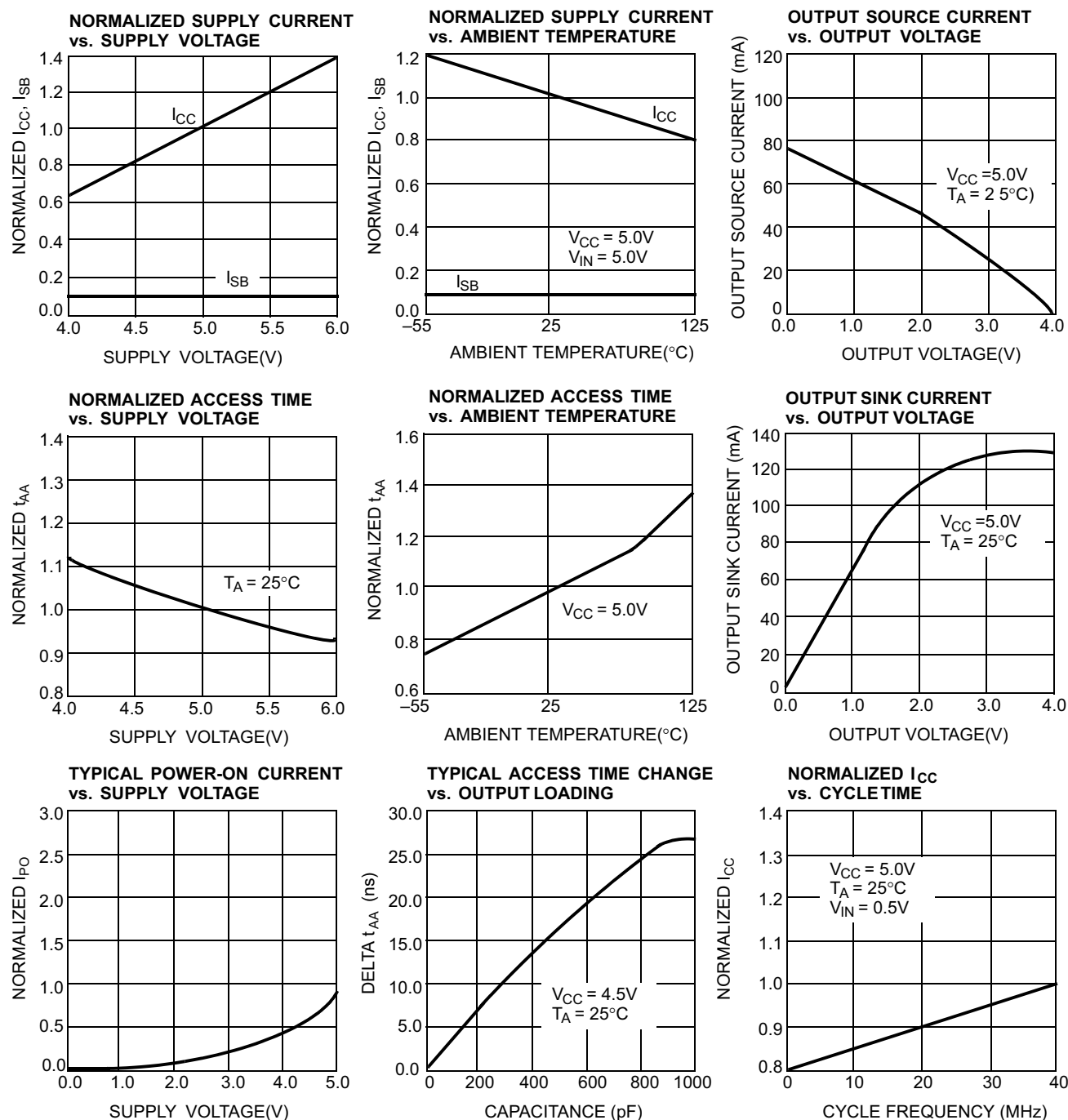


C128A-9

Notes:

12. Data I/O pins enter high-impedance state, as shown, when $\overline{\text{OE}}$ is held LOW during write.
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY7C128A-20VXC	51-85030	24-pin Molded SOJ (Pb-free)	Commercial
45	CY7C128A-45PC	51-85013	24-pin (300-Mil) Molded DIP	Commercial

Please contact local sales representative regarding availability of these parts

Package Diagrams

Figure 2. 24-pin (300-Mil) Molded DIP (51-85013)

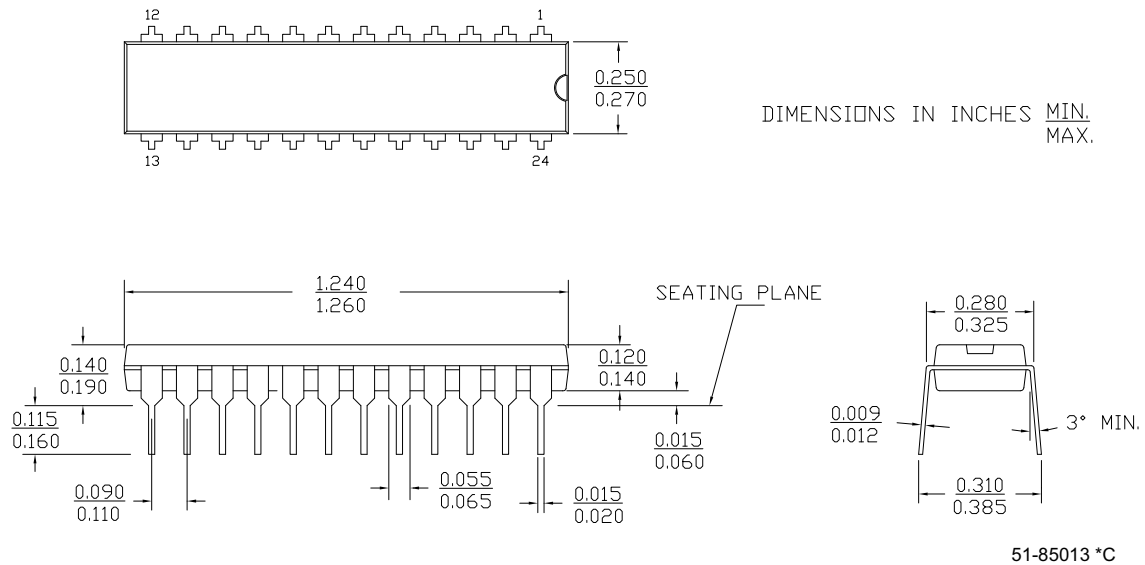
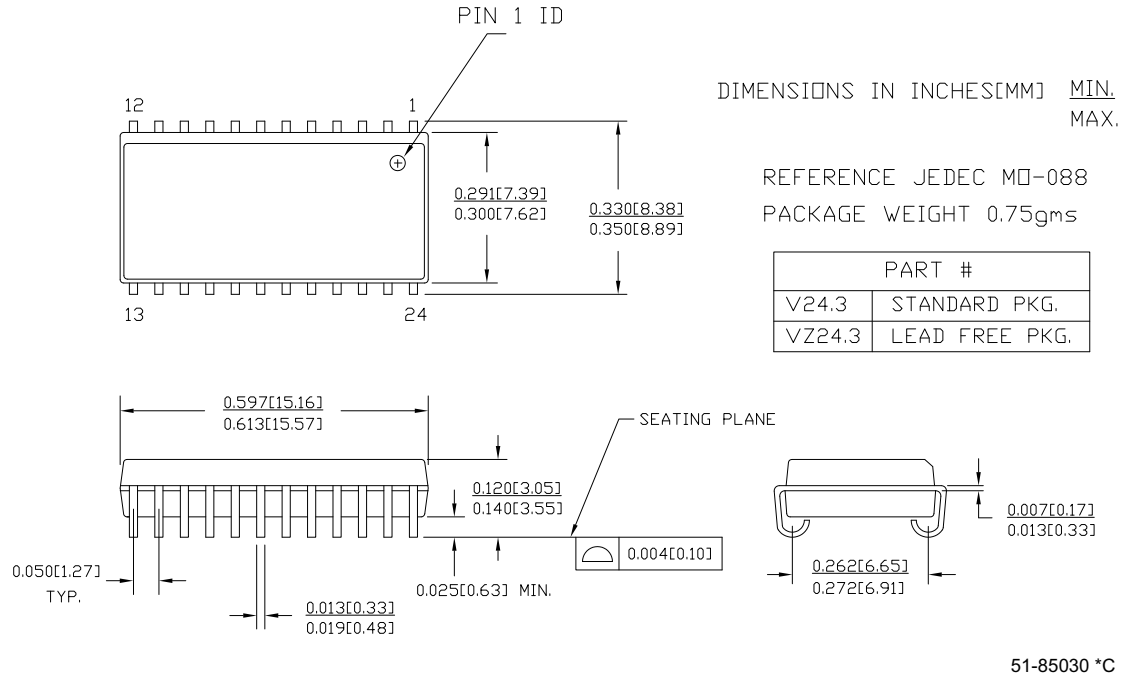


Figure 3. 24-pin (300-Mil) SOJ (51-85030)



Document History Page

Document Title: CY7C128A 2K x 8 Static RAM Document Number: 38-05028				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106814	09/10/01	SZV	Change from Spec number: 38-00094 to 38-05028
*A	493543	See ECN	NXR	Removed 25 ns speed bin Removed Military Operating Range Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated ordering Information Table
*B	2892244	03/19/2010	VKN	Removed 15ns and 35ns speed bin Updated Ordering Information table Updated Package Diagrams (Figure 2 and Figure 3) Added Sales, Solutions, and Legal Information

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
 PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.