

BUK764R0-75C

N-channel TrenchMOS standard level FET

Rev. 01 — 17 August 2006

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package, using Philips Ultra High-Performance (UHP) automotive TrenchMOS technology.

1.2 Features

- TrenchMOS technology
- 175 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

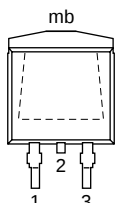
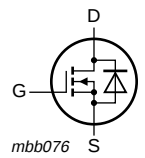
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V, 24 V and 42 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 630 \text{ mJ}$
- $I_D \leq 100 \text{ A}$
- $R_{DS(on)} = 3.4 \text{ m}\Omega$ (typ)
- $P_{tot} \leq 333 \text{ W}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D) ^[1]		
3	source (S)		
mb	mounting base; connected to drain		
		SOT404 (D2PAK)	

[1] It is not possible to make a connection to pin 2 of the SOT404 package.

PHILIPS

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK764R0-75C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	75	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	75	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	[1][2]	199	A
			[2][3]	100	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 2	[2][3]	100	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	797	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; see Figure 1	-	333	W
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$
T_j	junction temperature		-55	+175	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	[1][2]	199	A
			[1][3]	100	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	797	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 100\text{ A}$; $V_{DS} \leq 75\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ }^\circ\text{C}$	-	630	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[4]	-	J

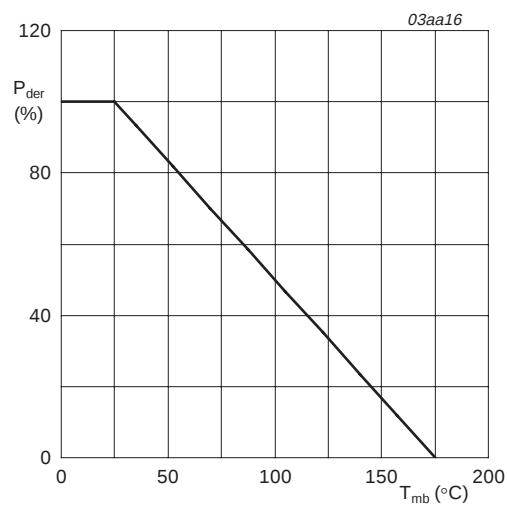
[1] Current is limited by chip power dissipation rating.

[2] Refer to document 9397 750 12572 for further information.

[3] Continuous current is limited by package.

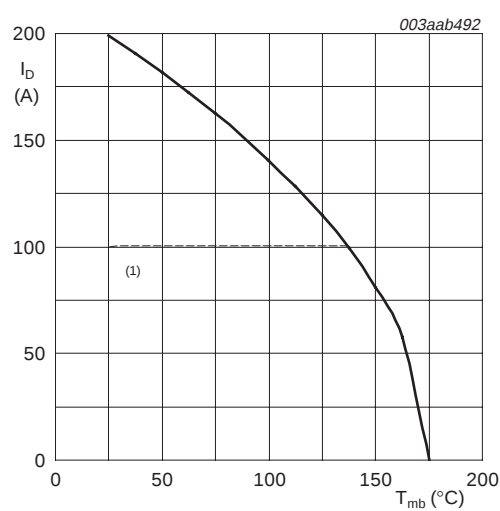
[4] Conditions:

- Maximum value not quoted. Repetitive rating defined in [Figure 16](#).
- Single-pulse avalanche rating limited by $T_{j(max)}$ of $175\text{ }^\circ\text{C}$.
- Repetitive avalanche rating limited by an average junction temperature of $170\text{ }^\circ\text{C}$.
- Refer to application note AN10273 for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

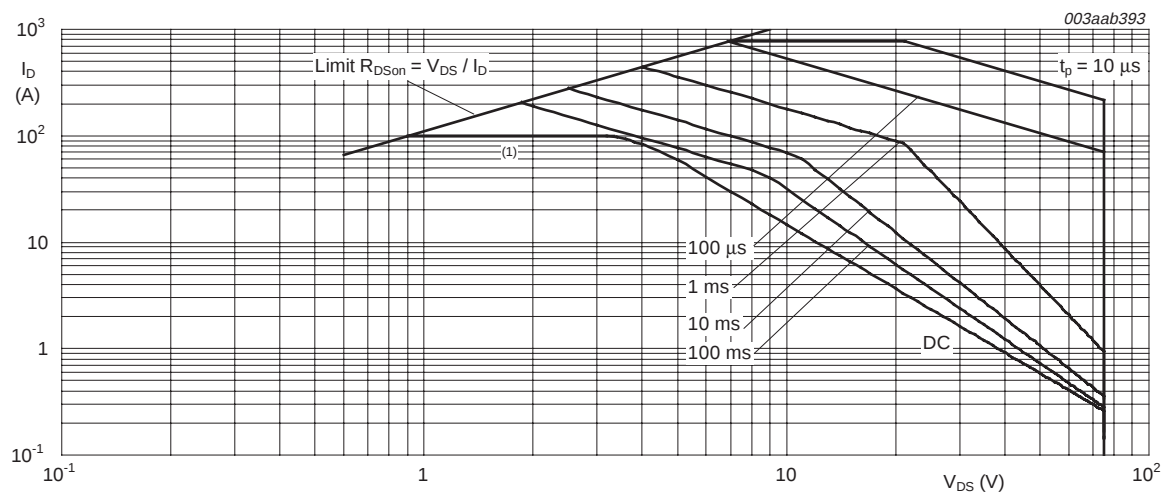
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$V_{GS} \geq 10 \text{ V}$$

(1) Capped at 100 A due to package.

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is single pulse.}$$

(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	-	50	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

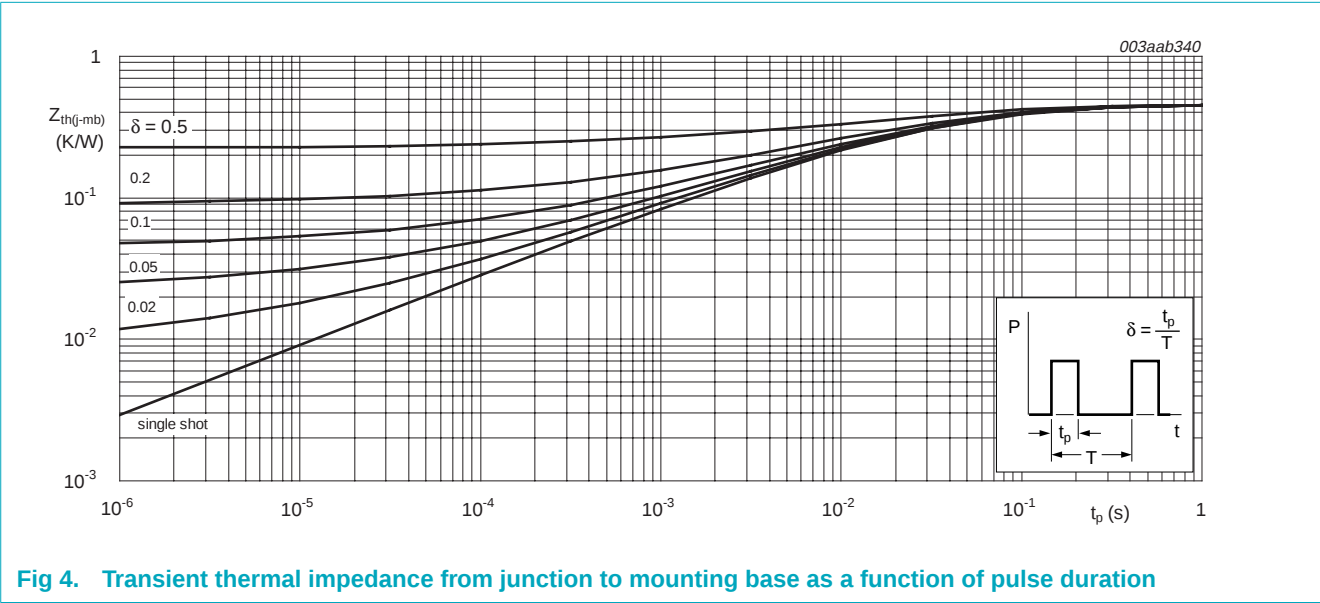
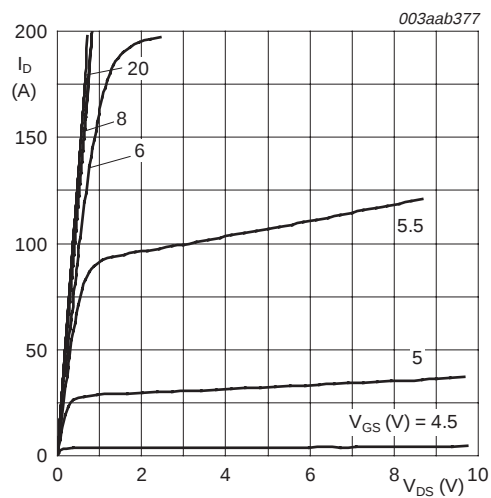


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

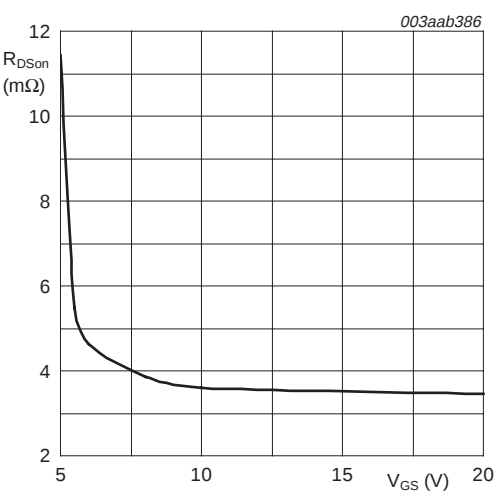
Table 5. Characteristics
 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	75	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	70	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	2	3	4	V
		$T_j = 175\text{ }^{\circ}\text{C}$	1	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 75\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	0.02	1	μA
		$T_j = 175\text{ }^{\circ}\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	3.4	4.0	m Ω
		$T_j = 175\text{ }^{\circ}\text{C}$	-	-	8.4	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DD} = 60\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 14	-	142	-	nC
Q_{GS}	gate-source charge		-	36	-	nC
Q_{GD}	gate-drain charge		-	67	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	5	-	V
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; see Figure 12	-	8744	11659	pF
C_{oss}	output capacitance		-	923	1108	pF
C_{rss}	reverse transfer capacitance		-	579	793	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$	-	65	-	ns
t_r	rise time		-	133	-	ns
$t_{d(off)}$	turn-off delay time		-	146	-	ns
t_f	fall time		-	119	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_R = 25\text{ V}$	-	83	-	ns
Q_r	recovered charge		-	155	-	nC



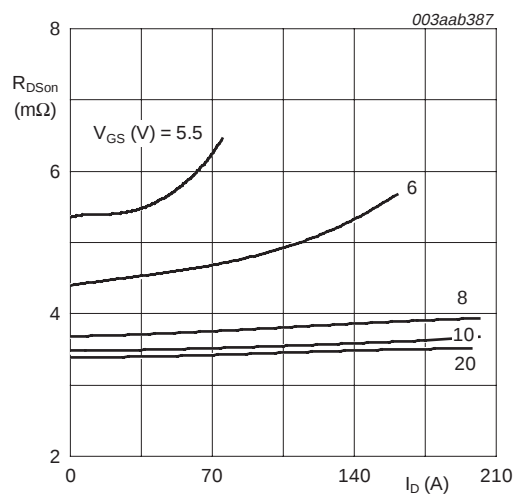
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



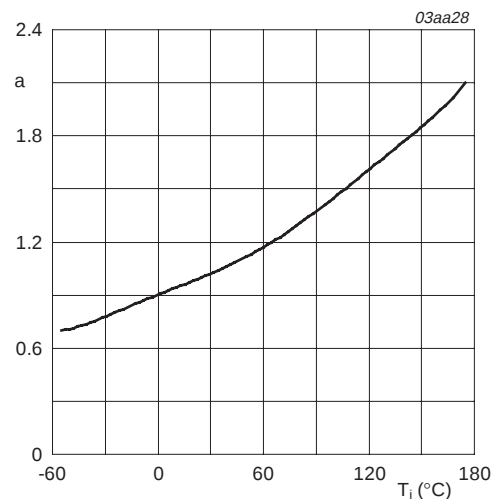
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



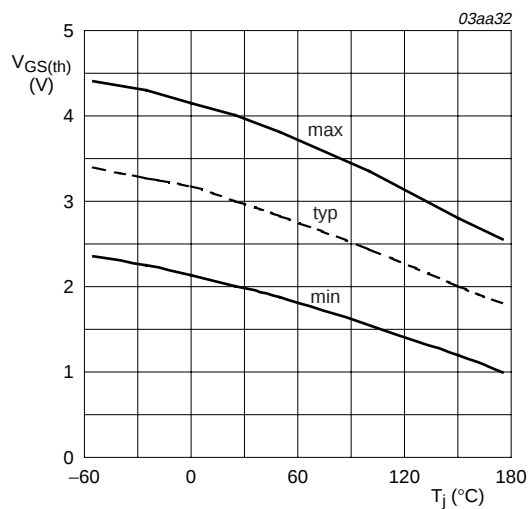
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



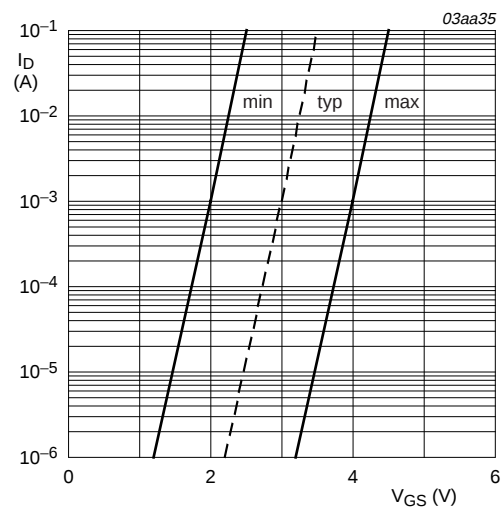
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



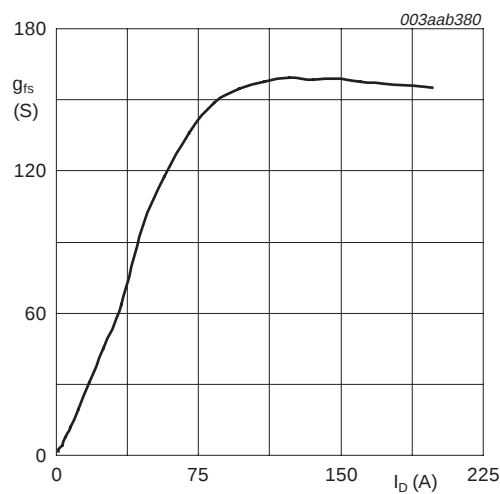
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



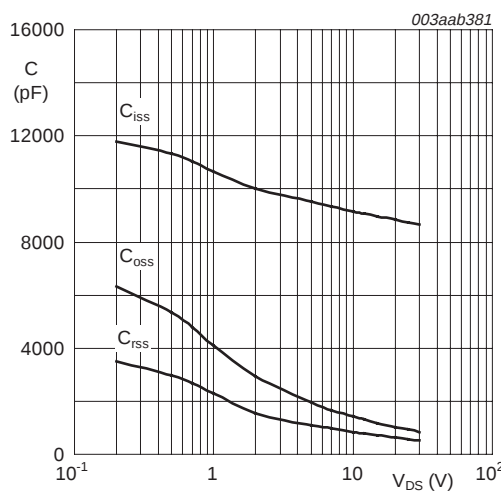
$T_j = 25 \text{ °C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25 \text{ °C}$; $V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

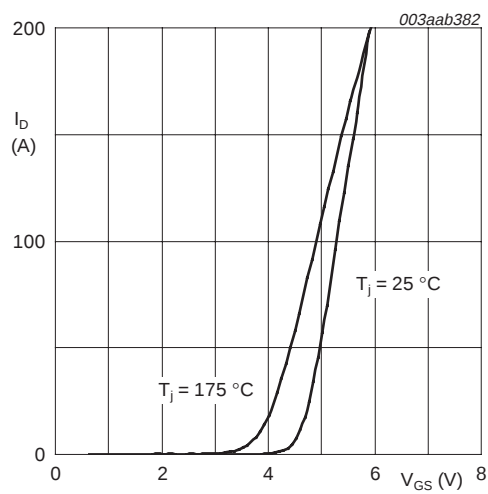


Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values

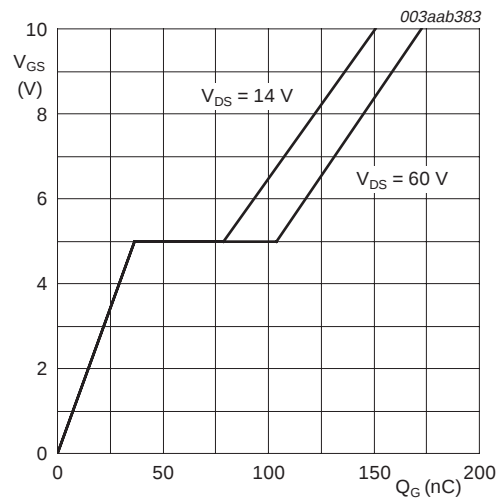


Fig 14. Gate-source voltage as a function of gate charge; typical values

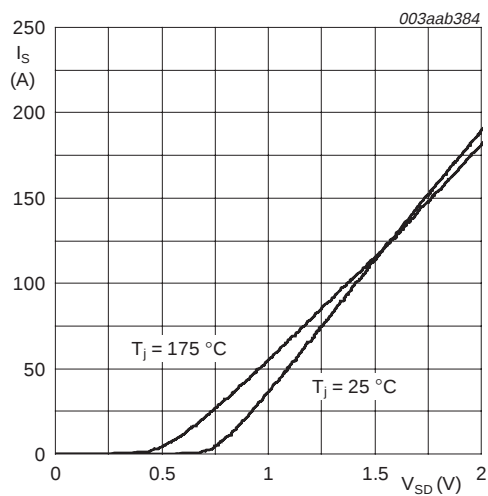
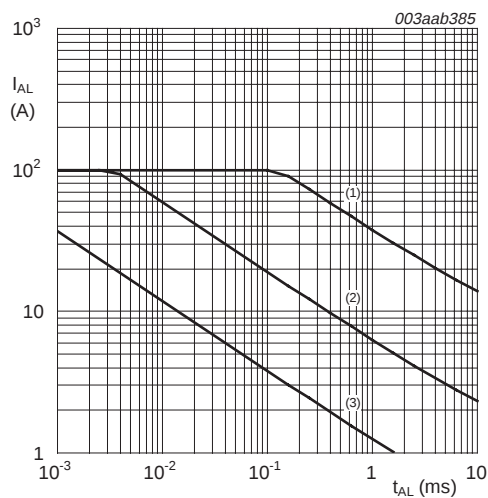


Fig 15. Source current as a function of source-drain voltage; typical values



See [Table note 4](#) of [Table 3 "Limiting values"](#).

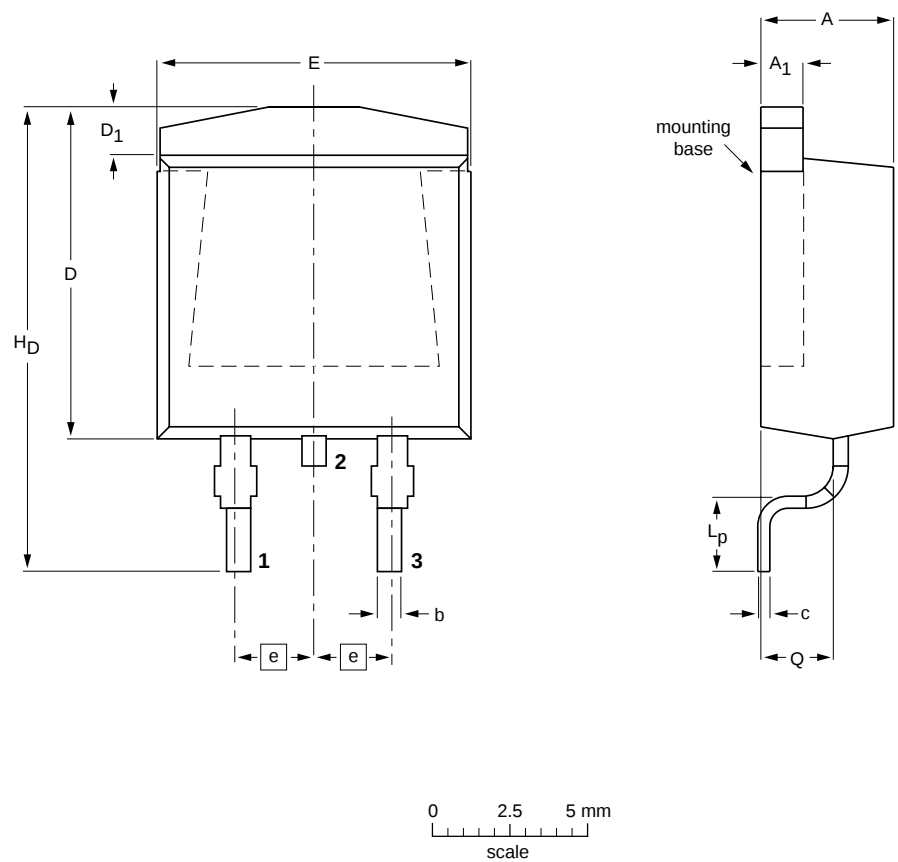
- (1) Single-pulse; $T_J = 25\text{ }^{\circ}\text{C}$.
- (2) Single-pulse; $T_J = 150\text{ }^{\circ}\text{C}$.
- (3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

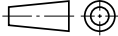
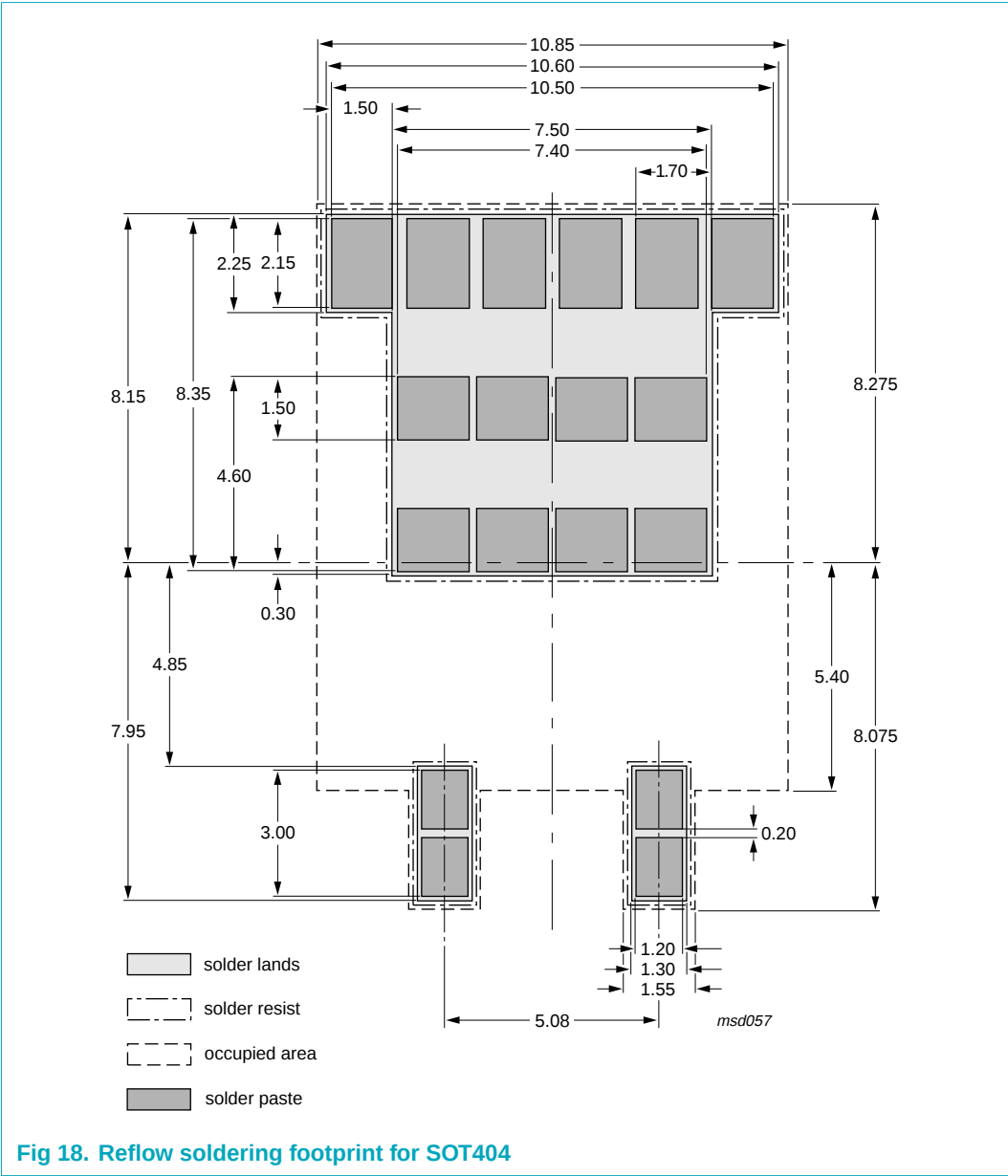
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 17. Package outline SOT404 (D2PAK)

8. Soldering



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK764R0-75C_1	20060817	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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