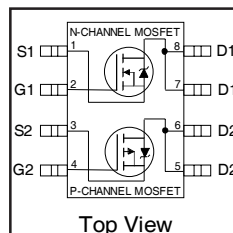


### HEXFET® Power MOSFET

#### Features

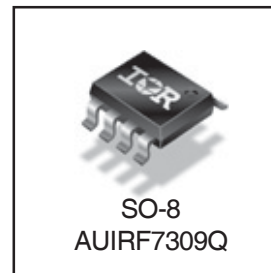
- Advanced Planar Technology
- Low On-Resistance
- Logic Level Gate Drive
- Dual N and P Channel MOSFET
- Dynamic  $dV/dT$  Rating
- 150°C Operating Temperature
- Fast Switching
- Lead-Free, RoHS Compliant
- Automotive Qualified\*



	N-CH	P-CH
$V_{(BR)DSS}$	30V	-30V
$R_{DS(on)}$ max.	0.05Ω	0.10Ω
$I_D$	4.7A	-3.5A

#### Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7309Q	SO-8	Tube	95	AUIRF7309Q
		Tape and Reel	4000	AUIRF7309QTR

#### Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

	Parameter	Max.		Units
		N-Channel	P-Channel	
$I_D$ @ $T_A = 25^\circ\text{C}$	10 Sec. Pulsed Drain Current, $V_{GS}$ @ 10V	4.7	-3.5	A
$I_D$ @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	4	-3.0	
$I_D$ @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	3.2	-2.4	
$I_{DM}$	Pulsed Drain Current ①	16	-12	
$P_D$ @ $T_A = 25^\circ\text{C}$	Power Dissipation ④	1.4		W
	Linear Derating Factor ④	0.011		W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20		V
$dv/dt$	Peak Diode Recovery $dv/dt$ ②	6.9	-6.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150		°C

#### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ④	—	90	°C/W

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\*Qualification standards can be found at <http://www.irf.com/>

**Static Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
		P-Ch	—	-0.037	—		Reference to $25^\circ\text{C}$ , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	$\Omega$	$V_{GS} = 10V, I_D = 2.4A$ ③
			—	—	0.080		$V_{GS} = 4.5V, I_D = 2.0A$ ③
		P-Ch	—	—	0.10		$V_{GS} = -10V, I_D = 1.8A$ ③
			—	—	0.16		$V_{GS} = -4.5V, I_D = 1.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	-3.0		$V_{DS} = V_{GS}, I_D = -250\mu A$
$g_{fs}$	Forward Transconductance	N-Ch	5.2	—	—	S	$V_{DS} = 15V, I_D = 2.4A$
		P-Ch	2.5	—	—		$V_{DS} = -24V, I_D = -1.8A$
$I_{DSS}$	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	$\mu A$	$V_{DS} = 24V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	N-P	—	—	-100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	N-P	—	—	100		$V_{GS} = -20V$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter		Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel $I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V$ ③
		P-Ch	—	—	25		
$Q_{gs}$	Gate-to-Source Charge	N-Ch	—	—	2.9	nC	P-Channel $I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V$
		P-Ch	—	—	2.9		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	7.9	nC	N-Channel $V_{DD} = 10V, I_D = 2.6A, R_G = 6.0\Omega$
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	P-Ch	—	6.8	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega$ $R_D = 4.5\Omega$
		N-Ch	—	11	—		
$t_r$	Rise Time	P-Ch	—	21	—		
		N-Ch	—	17	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	22	—	ns	N-Channel $V_{DD} = 10V, I_D = 2.6A, R_G = 6.0\Omega$ $R_D = 3.8\Omega$
		P-Ch	—	25	—		
$t_f$	Fall Time	N-Ch	—	7.7	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega$ $R_D = 4.5\Omega$
		P-Ch	—	18	—		
$L_D$	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	N-P	—	6.0	—		
$C_{iss}$	Input Capacitance	N-Ch	—	520	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	440	—		
$C_{oss}$	Output Capacitance	N-Ch	—	180	—		
		P-Ch	—	200	—		
$C_{rss}$	Reverse Transfer Capacitance	N-Ch	—	72	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$
		P-Ch	—	93	—		

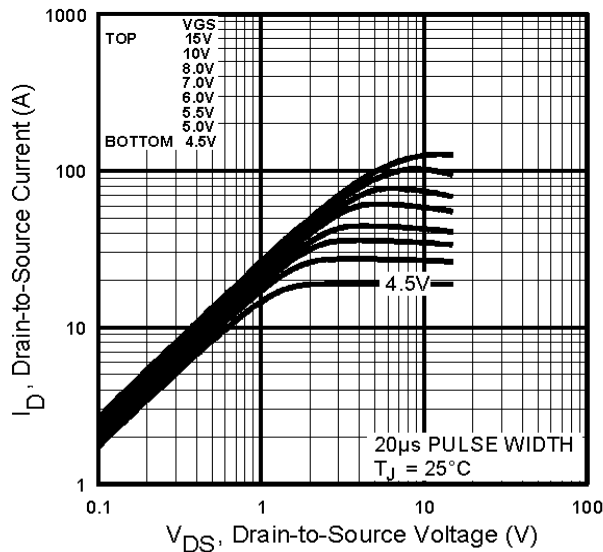
**Diode Characteristics**

	Parameter		Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	N-Ch	—	—	1.8	A	
		P-Ch	—	—	-1.8		
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	16		
		P-Ch	—	—	-12		
V <sub>SD</sub>	Diode Forward Voltage	N-Ch	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 1.8A, V <sub>GS</sub> = 0V ③
		P-Ch	—	—	-1.0		T <sub>J</sub> = 25°C, I <sub>S</sub> = -1.8A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel T <sub>J</sub> = 25°C, I <sub>F</sub> =2.6A, di/dt = 100A/μs
		P-Ch	—	53	80		
Q <sub>rr</sub>	Reverse Recovery Charge	N-Ch	—	56	84	nC	P-Channel T <sub>J</sub> = 25°C, I <sub>F</sub> =-2.2A, di/dt = 100A/μs ③
		P-Ch	—	66	99		
t <sub>on</sub>	Forward Turn-On Time	N-P	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

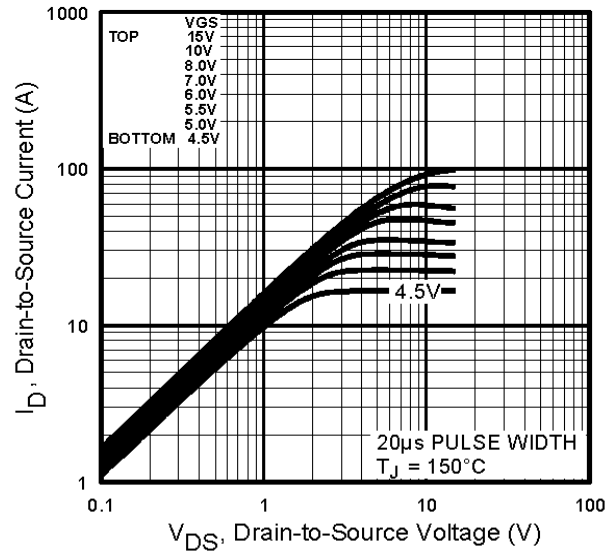
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 23 )
- ② N-Channel  $I_{SD} \leq 2.4A, di/dt \leq 73A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$ .  
P-Channel  $I_{SD} \leq -1.8A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$ .
- ③ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ④ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

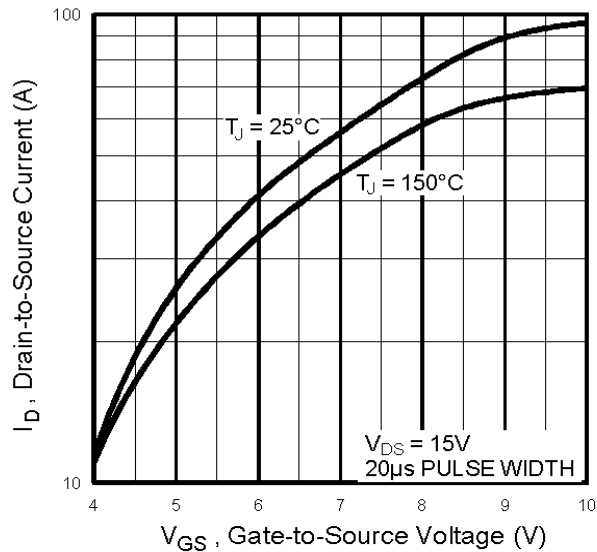
### N-Channel



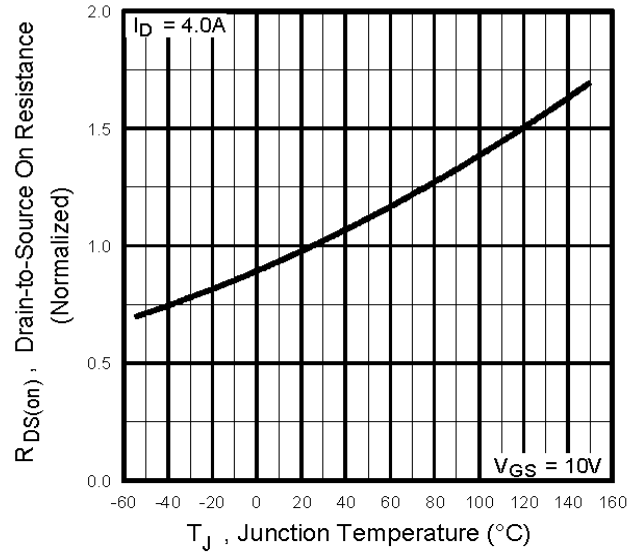
**Fig 1.** Typical Output Characteristics,  
 $T_J = 25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_J = 150^\circ\text{C}$

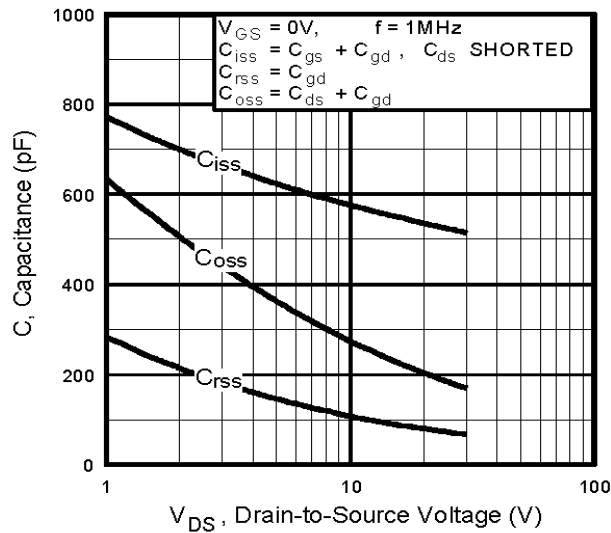


**Fig 3.** Typical Transfer Characteristics

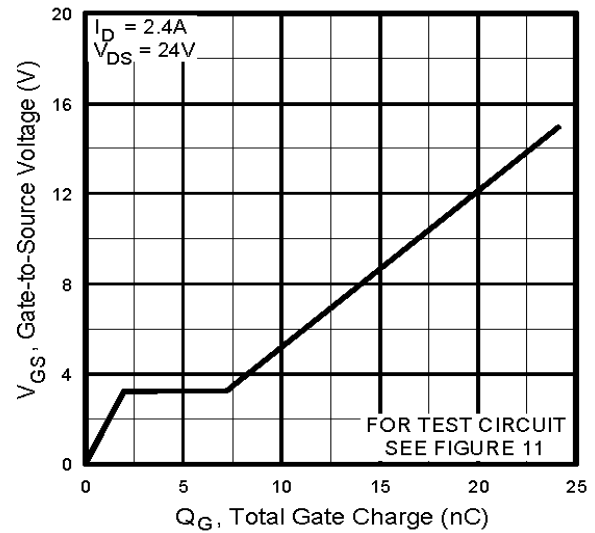


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

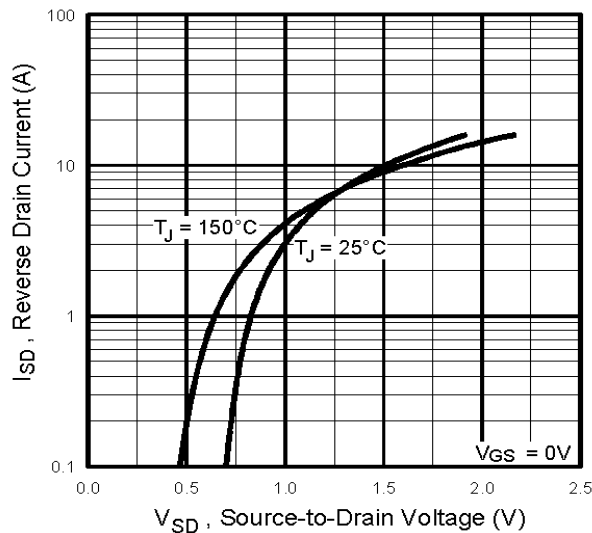
### N-Channel



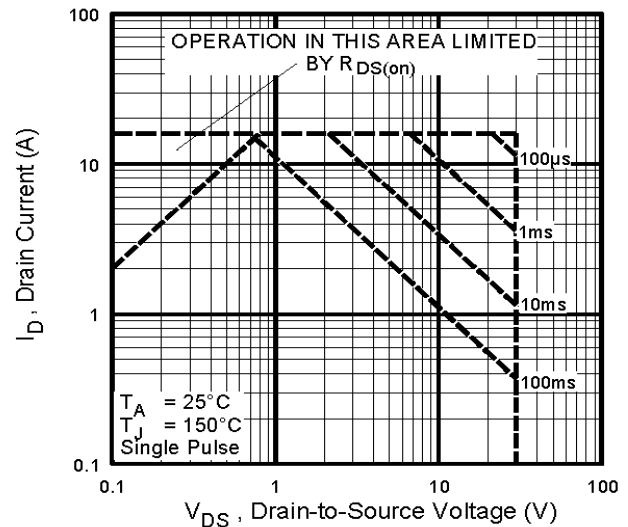
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

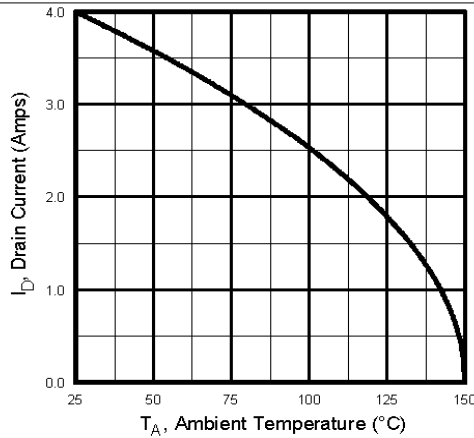


**Fig 7.** Typical Source-Drain Diode Forward Voltage

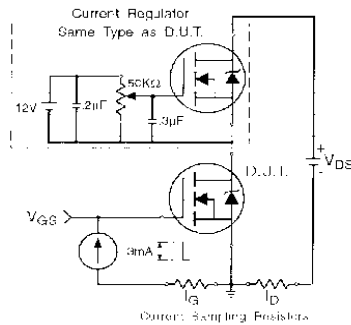


**Fig 8.** Maximum Safe Operating Area

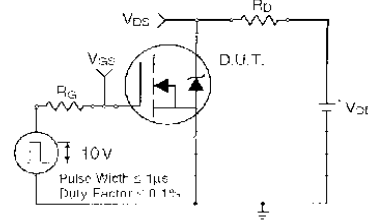
### N-Channel



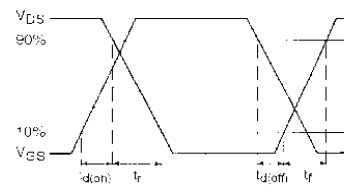
**Fig 9.** Max. Drain Current Vs. Ambient Temp.



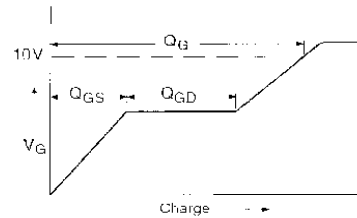
**Fig 11a.** Gate Charge Test Circuit



**Fig 10a.** Switching Time Test Circuit

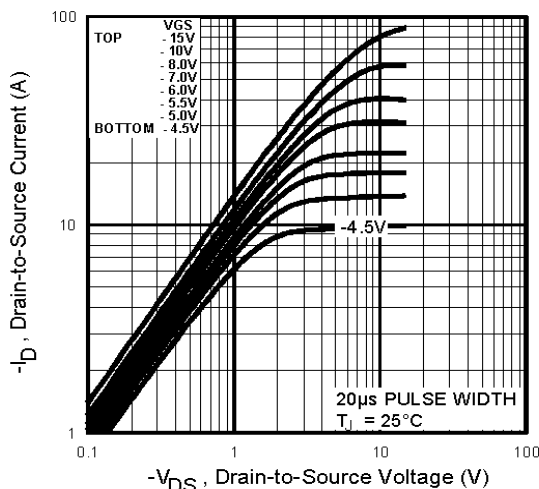


**Fig 10b.** Switching Time Waveforms

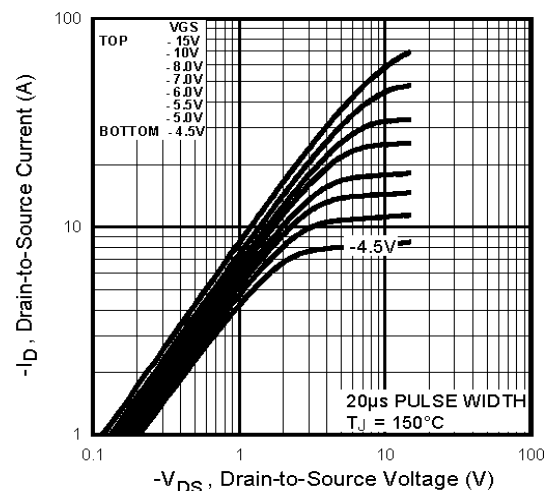


**Fig 11b.** Basic Gate Charge Waveform

### P-Channel

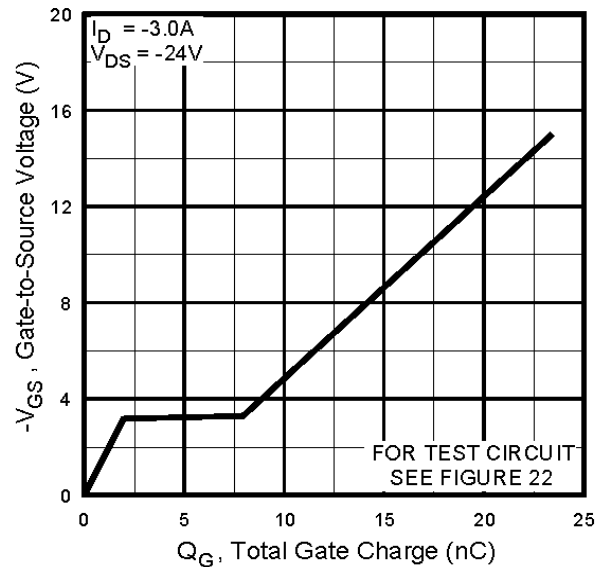
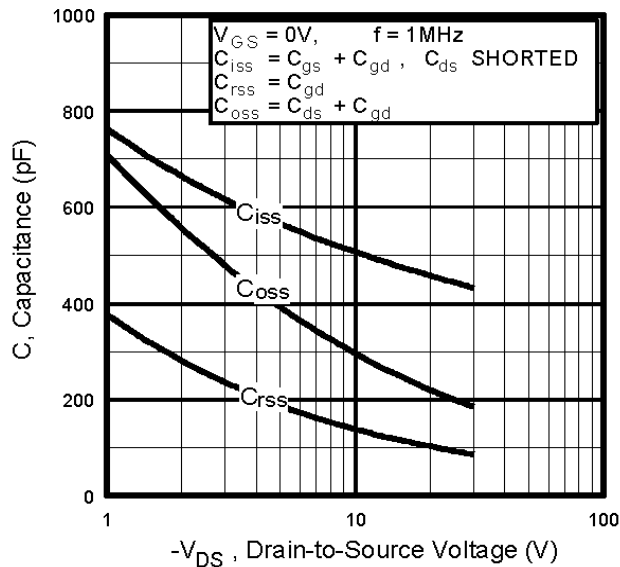
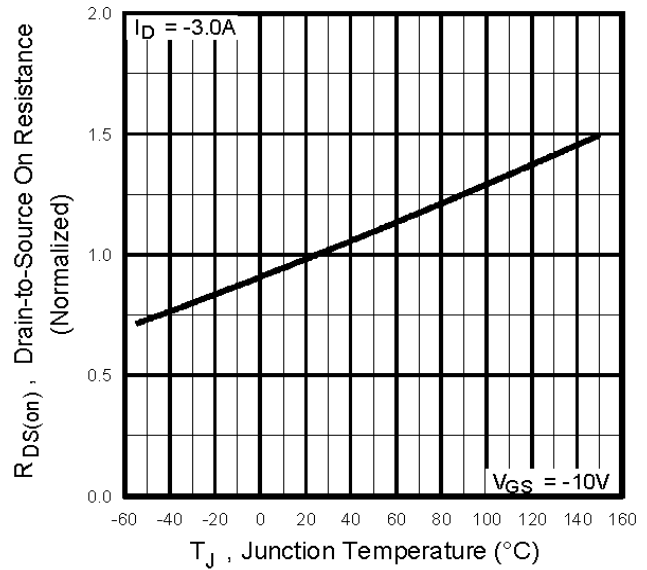
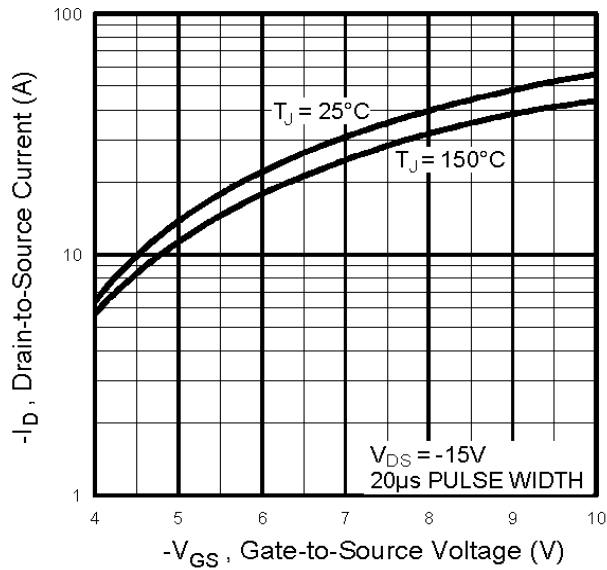


**Fig 12.** Typical Output Characteristics,  $T_J = 25^\circ\text{C}$

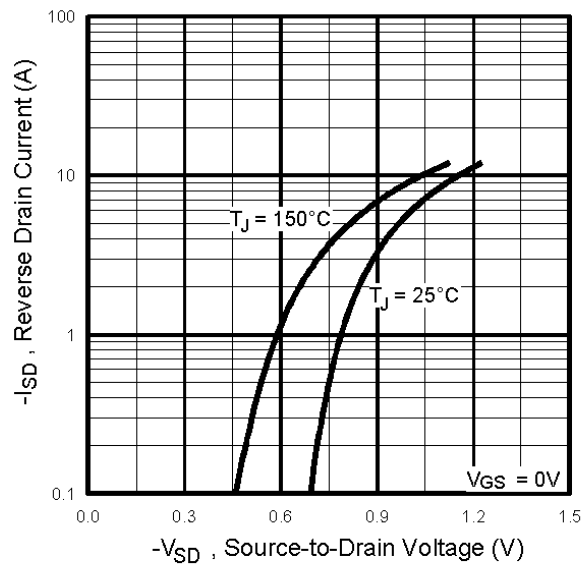


**Fig 13.** Typical Output Characteristics,  $T_J = 150^\circ\text{C}$

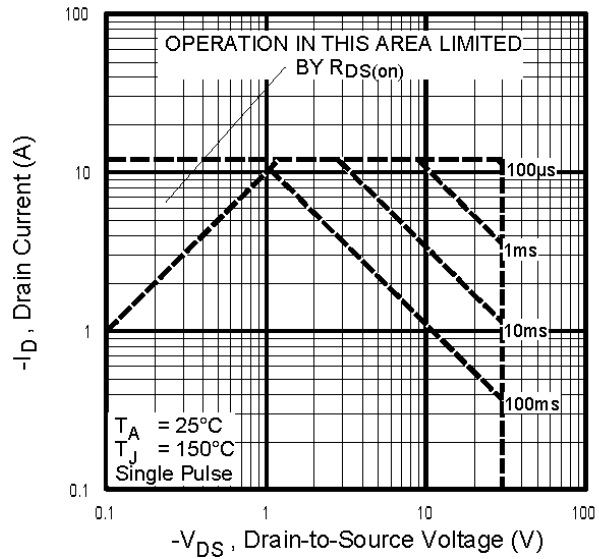
# P-Channel



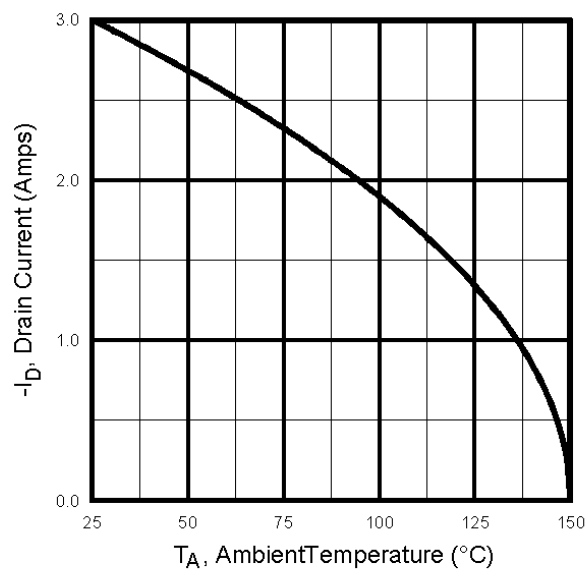
### P-Channel



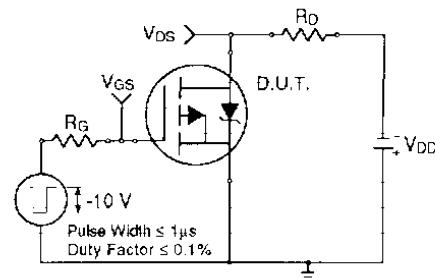
**Fig 18.** Typical Source-Drain Diode Forward Voltage



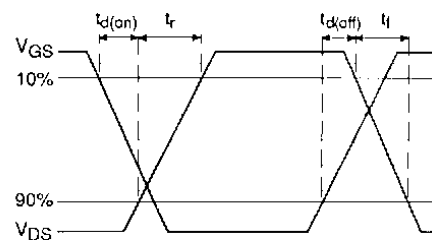
**Fig 19.** Maximum Safe Operating Area



**Fig 20.** Max. Drain Current Vs. Ambient Temp.

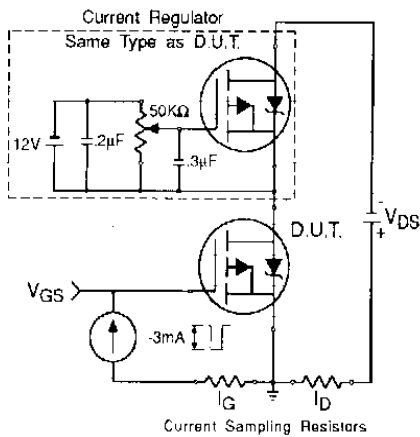


**Fig 21a.** Switching Time Test Circuit

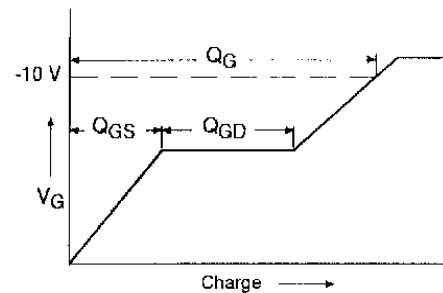


**Fig 21b.** Switching Time Waveforms

## P-Channel

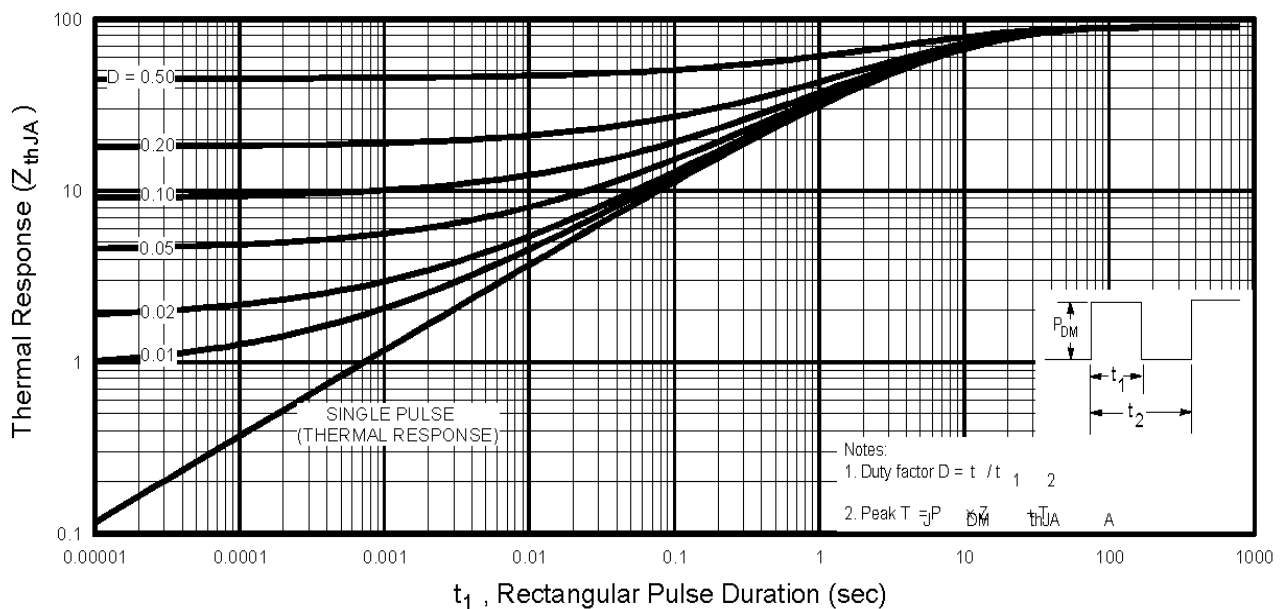


**Fig 22b.** Gate Charge Test Circuit



**Fig 22b.** Basic Gate Charge Waveform

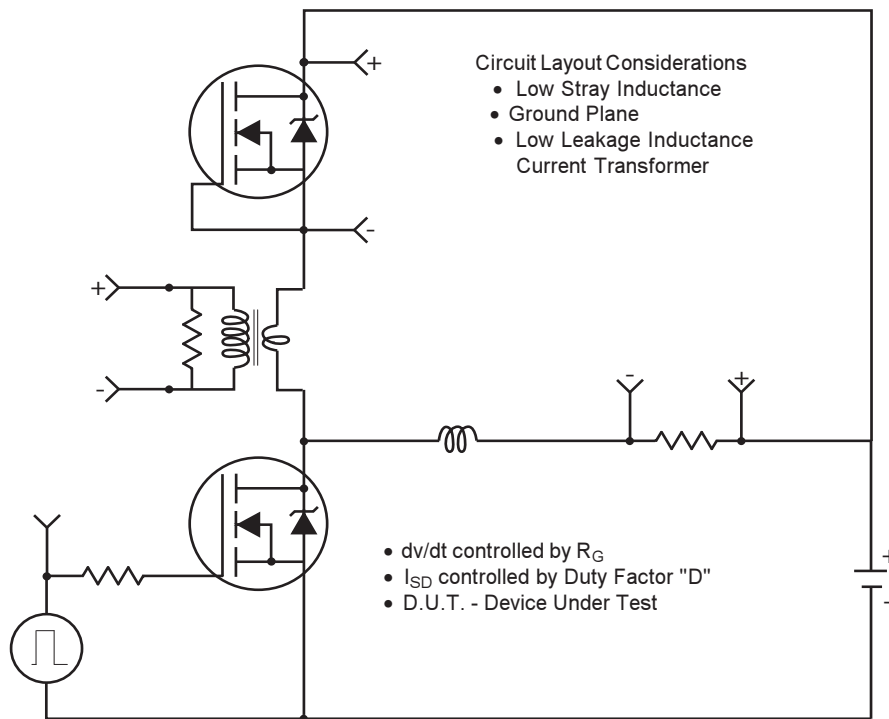
## N- and P-Channel



**Fig 23.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

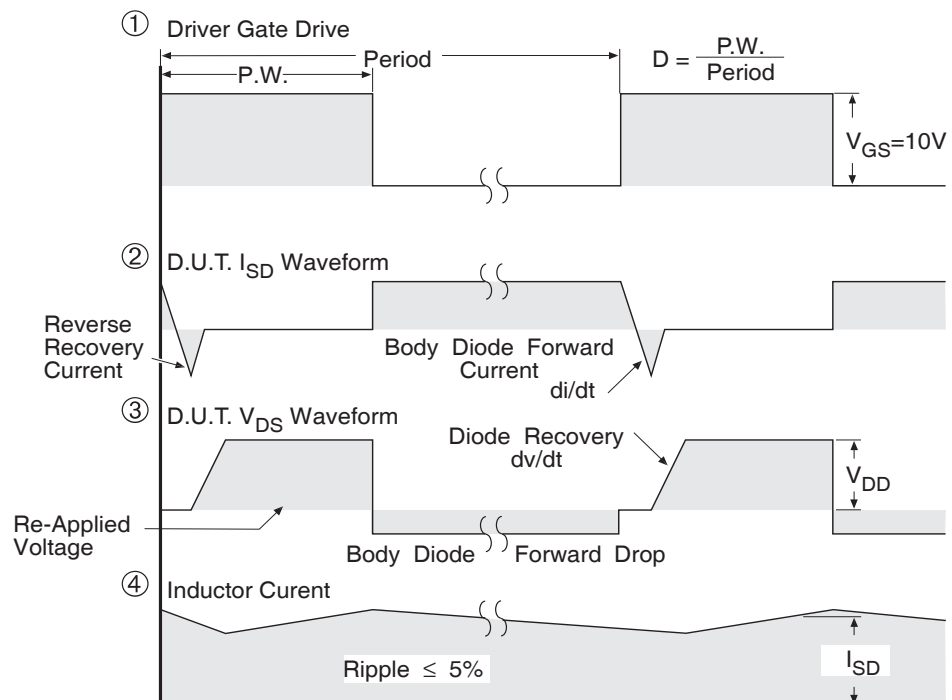


# Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements

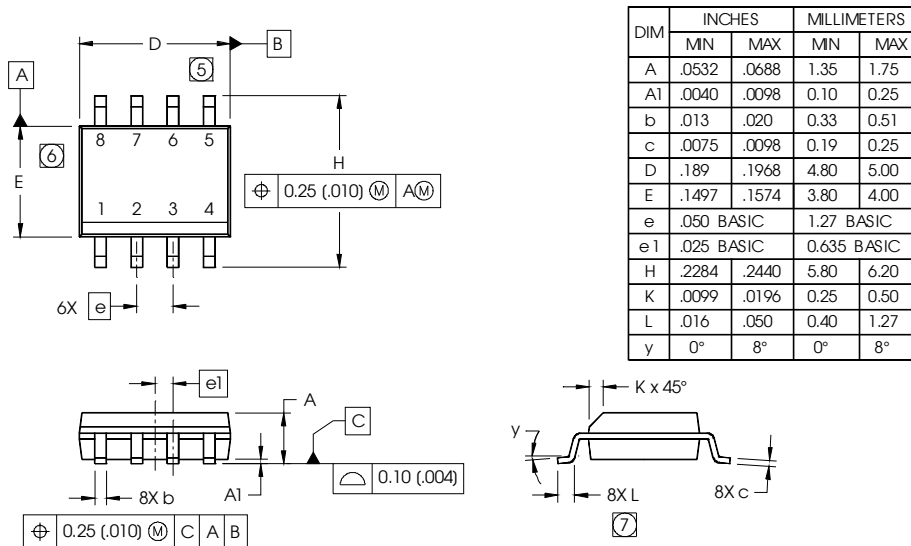


\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 24.** For N and P Channel HEXFETS

## SO-8 Package Outline

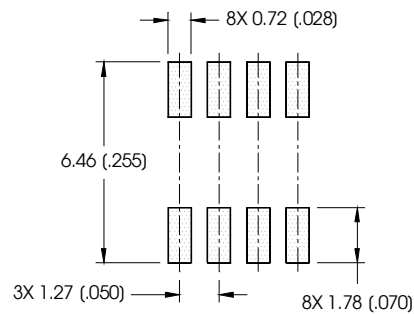
Dimensions are shown in millimeters (inches)



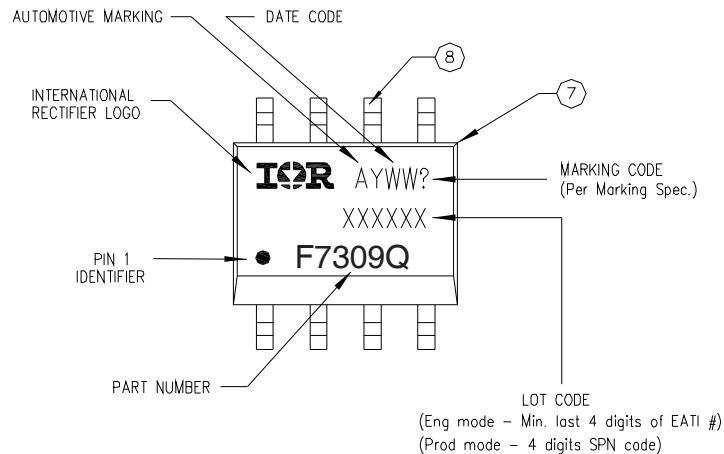
### NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO SUBSTRATE.

### FOOTPRINT



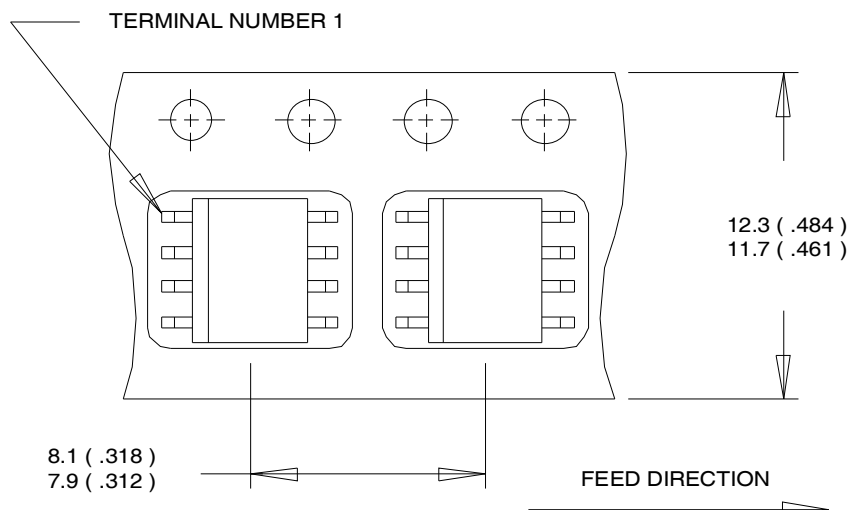
## SO-8 Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

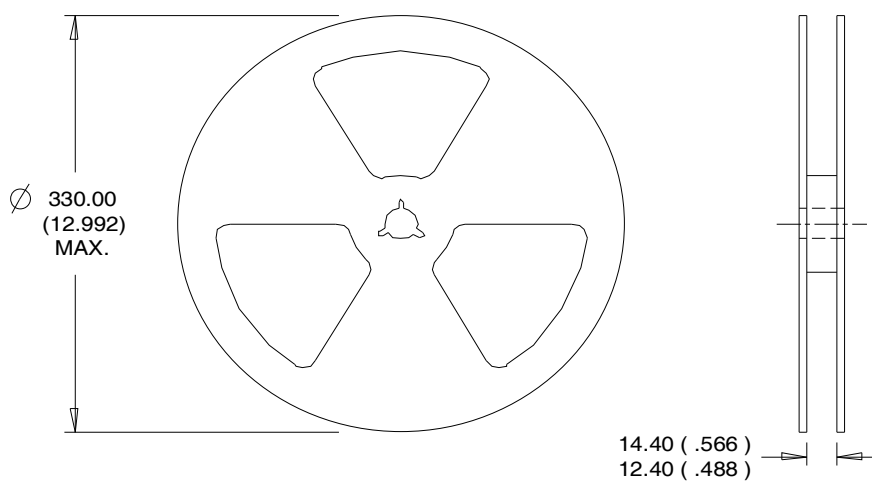
## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



### NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# Qualification Information<sup>†</sup>

Qualification Level		Automotive (per AEC-Q101) <sup>††</sup>	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	N-CH: Class M2 (+/- 150V) <sup>†††</sup> P-CH: Class M2 (+/- 150V) <sup>†††</sup> AEC-Q101-002	
	Human Body Model	N-CH: Class H1A (+/- 500V) <sup>†††</sup> P-CH: Class H0 (+/- 250V) <sup>†††</sup> AEC-Q101-001	
	Charged Device Model	N-CH: Class C5 (+/- 2000V) <sup>†††</sup> P-CH: Class C5 (+/- 2000V) <sup>†††</sup> AEC-Q101-005	
RoHS Compliant		Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

<sup>††</sup> Exceptions to AEC-Q101 requirements are noted in the qualification report.

<sup>†††</sup> Highest passing voltage.

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<http://www.irf.com/technical-info/>

### WORLD HEADQUARTERS:

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# Revision History

Date	Comments
3/28/2014	<ul style="list-style-type: none"> <li>Added "Logic Level Gate Drive" bullet in the features section on page 1</li> <li>Updated data sheet with new IR corporate template</li> </ul>