

## TC74HC166AP, TC74HC166AF

### 8-Bit Shift Register (P-IN, S-OUT)

The TC74HC166A is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

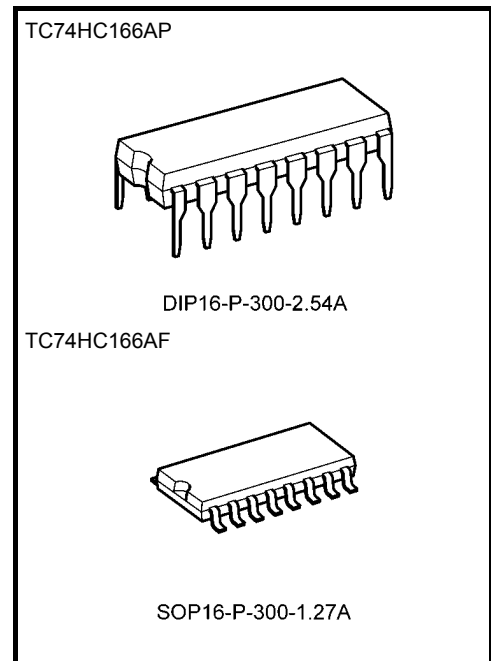
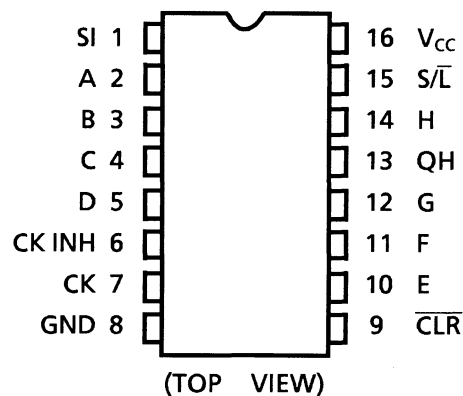
It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CK-INH input should be shifted high only while the CK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{\max} = 57 \text{ MHz}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive immunity: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (\text{opr}) = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS166

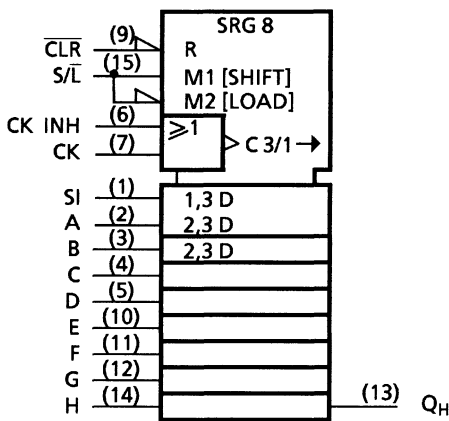
### Pin Assignment



### Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

IEC Logic Symbol



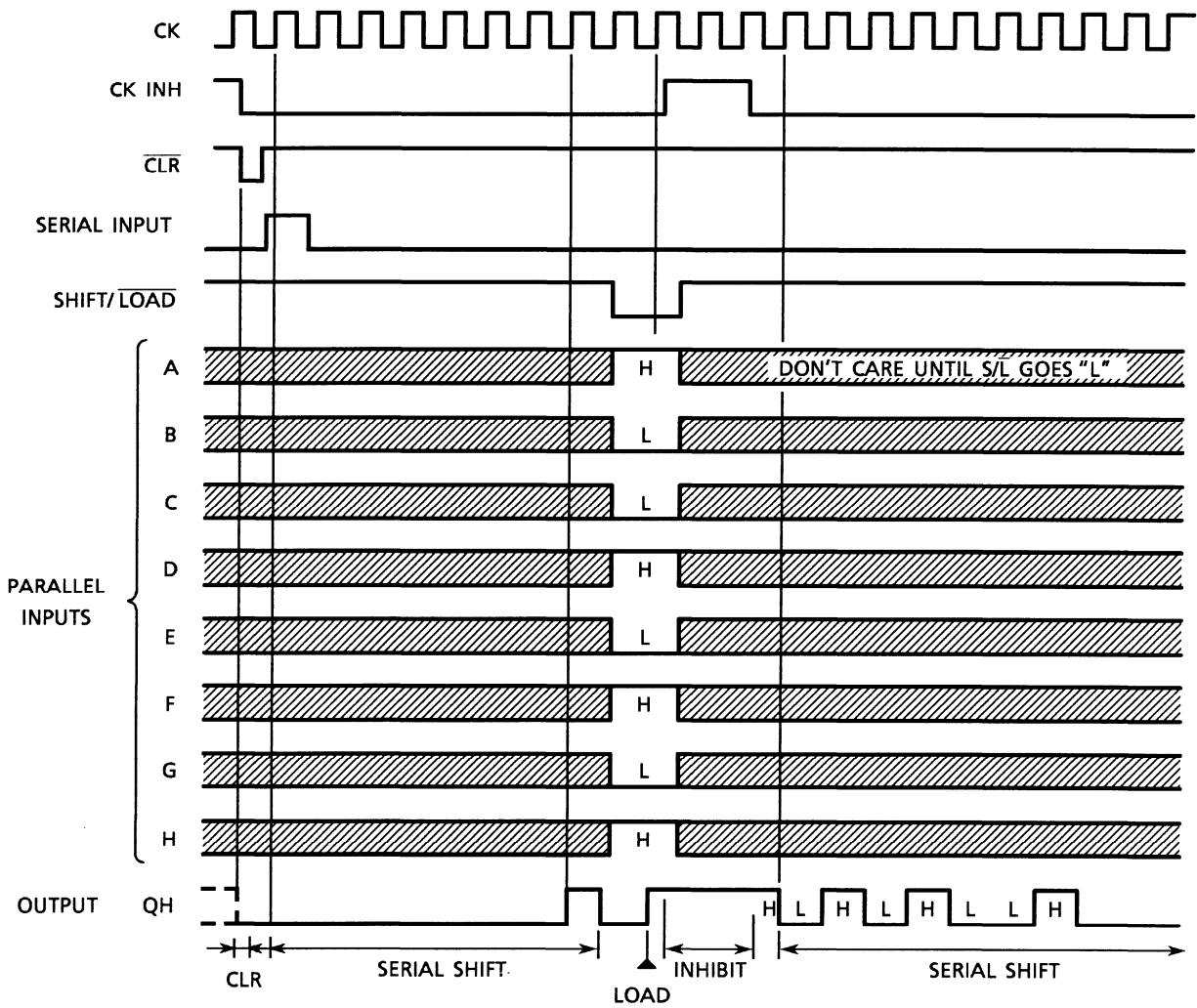
Truth Table

Inputs						Internal Outputs		Output
CLR	SHIFT/LOAD	CK INH.	CK	SERIAL IN	PARALLEL A.....H	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	X		X	X	No Change		
H	L	L		X	a.....h	a	b	h
H	H	L		H	X	H	QAn	QGn
H	H	L		L	X	L	QAn	QGn
H	X	H	X	X	X	No Change		

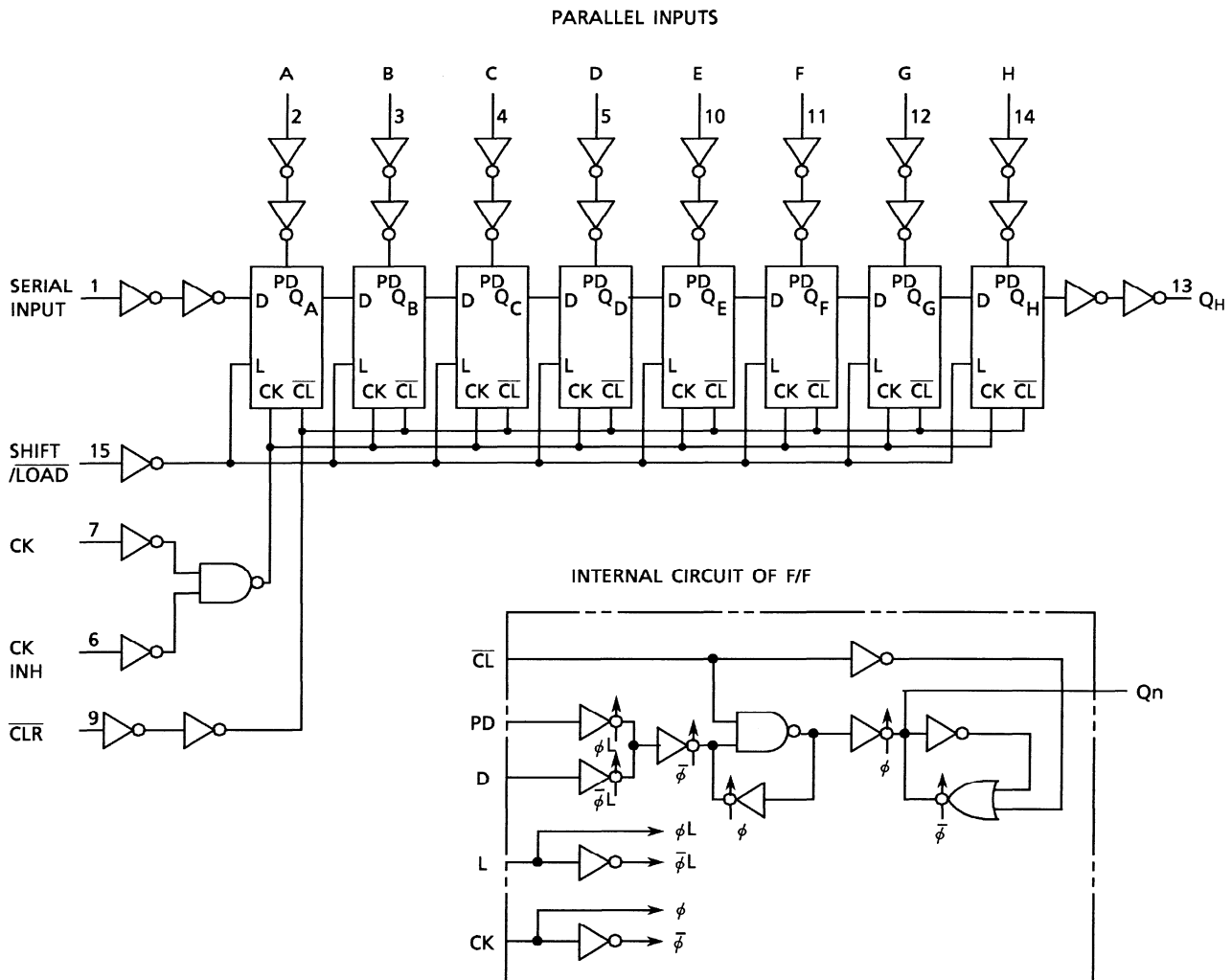
X: Don't care

a.....h: The level of steady state input voltage at inputs A through H respectively

Timing Chart



## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^\circ\text{C}$ . From  $T_a = 65$  to  $85^\circ\text{C}$  a derating factor of  $-10 \text{ mW}/^\circ\text{C}$  shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**Electrical Characteristics**
**DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = –40 to 85°C		Unit	
				VCC (V)	Min	Typ.	Max	Min		Max
High-level input voltage	VIH	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V	
Low-level input voltage	VIL	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High-level output voltage	VOH	VIN = VIH or VIL	IOH = –20 µA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			IOH = –4 mA IOH = –5.2 mA	6.0	5.9	6.0	—	5.9	—	
				4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low-level output voltage	VOL	VIN = VIH or VIL	IOL = 20 µA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			IOL = 4 mA IOL = 5.2 mA	6.0	—	0.0	0.1	—	0.1	
				4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input leakage current	IIN	VIN = VCC or GND		6.0	—	—	±0.1	—	±1.0	µA
Quiescent supply current	ICC	VIN = VCC or GND		6.0	—	—	4.0	—	40.0	µA

Timing Requirements (input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_W$ (H) $t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{\text{CLR}}$ )	$t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (SI, PI)	$t_s$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ( $\text{S}/\overline{\text{L}}$ )	$t_s$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time (SI, PI)	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time ( $\text{S}/\overline{\text{L}}$ )	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ( $\overline{\text{CLR}}$ )	$t_{\text{rem}}$	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{\text{TLH}}$	—	—	4	8	ns
	$t_{\text{THL}}$					
Propagation delay time (CK-QH)	$t_{\text{PLH}}$	—	—	16	26	ns
	$t_{\text{PHL}}$					
Propagation delay time ( $\overline{\text{CLR}}$ -QH)	$t_{\text{pHL}}$	—	—	15	24	ns
Maximum clock frequency	$f_{\text{max}}$	—	33	57	—	MHz

**AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation delay time (CK-QH)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	70	150	—	190
			4.5	—	20	30	—	38
			6.0	—	16	26	—	32
Propagation delay time ( $\overline{\text{CLR}}$ -QH)	$t_{pHL}$	—	2.0	—	60	135	—	170
			4.5	—	18	27	—	34
			6.0	—	14	23	—	29
Maximum clock frequency	$f_{\text{max}}$	—	2.0	6	14	—	5	—
			4.5	31	50	—	25	—
			6.0	36	63	—	29	—
Input capacitance	$C_{\text{IN}}$	—	—	—	5	10	—	10
Power dissipation capacitance	$C_{\text{PD}}$ (Note)	—	—	—	60	—	—	—

Note:  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

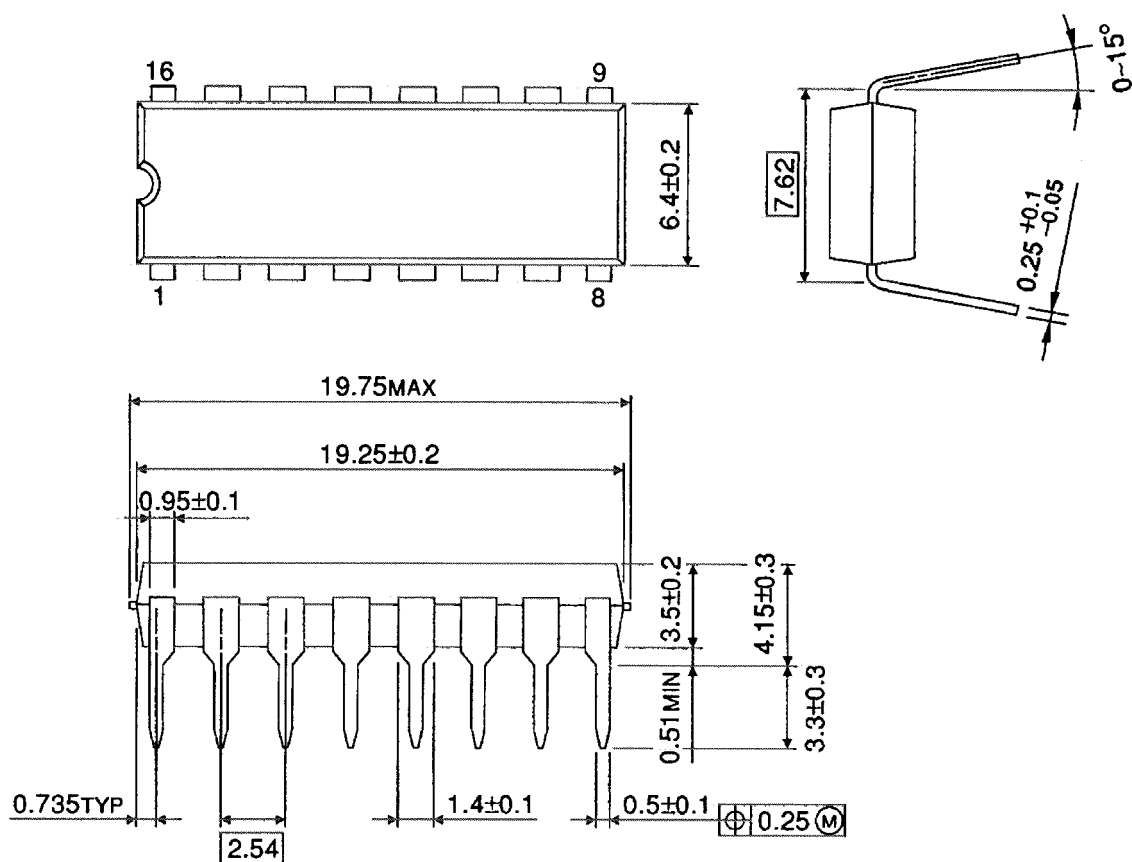
Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

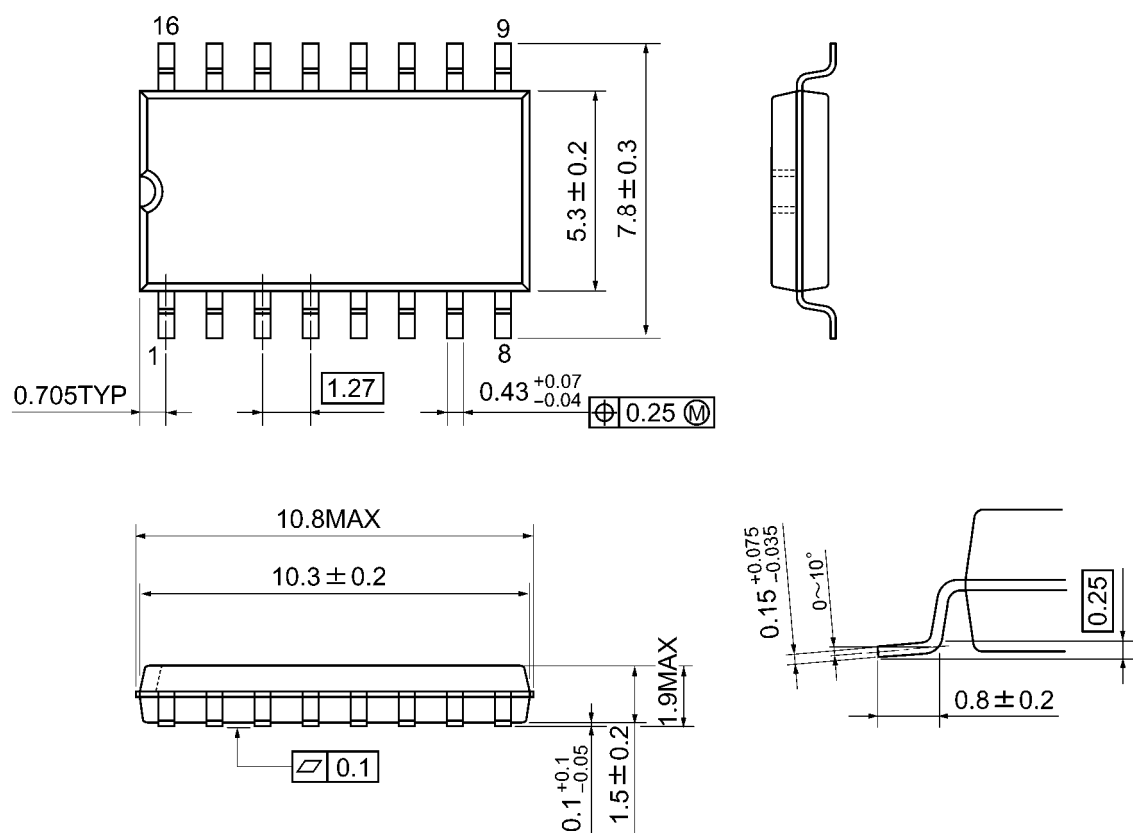


Weight: 1.00 g (typ.)

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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