CMOS 8-Bit Microcontroller

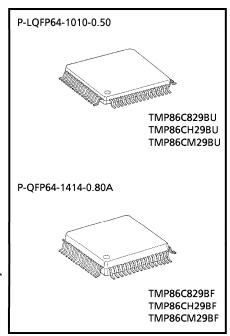
TMP86C829BU/BF, TMP86CH29BU/BF, TMP86CM29BU/BF

The TMP86C829B/H29B/M29B are the high-speed, high-performance and low power consumption 8-bit microcomputer, including ROM, RAM, LCD driver, multi-function timer/counter, serial interface (UART/SIO), a 10-bit AD converter and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86C829BU/BF	8 K × 8 bits	512 × 8 bits	D 1 OFD64 1010 0 F0	
TMP86CH29BU/BF	16 K × 8 bits	4 F K 0 hita	P-LQFP64-1010-0.50	TMP86PM29AU/AF
TMP86CM29BU/BF	32 K × 8 bits	1.5 K × 8 bits	P-QFP64-1414-0.80A	

Features

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: $0.25 \mu s$ (at 16 MHz) 122 μ s (at 32.768 kHz)
- ◆ 132 types and 731 basic instructions
- 19-interrupt sources (External: 5, Internal: 14)
- Input/output ports (39 pins) (Out of which 24 pins are also used as SEG pins)
- ◆ 18-bit timer counter: 1 ch
 - Timer, Event counter, Pulse width measurement, Frequencymeasurement modes
- ◆ 8-bit timer counter: 4 ch
 - Timer, Event counter, PWM output, Programmable divider output, PPG output modes



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- ◆ Time base timer
- ◆ Divider output function
- ♦ Watchdog timer
 - Interrupt source/reset output (programmable)
- ♦ Serial interface
 - 8-bit UART/SIO: 1ch
- ◆ 10-bit successive approximation type AD converter
 - Analog input: 8 ch
- ◆ Four key-on wake-up pins
- ◆ LCD driver/controller
 - Built-in voltage booster for LCD driver
 - With displaymemory
 - LCD direct drive capability (Max 32 seg × 4 com)
 - 1/4, 1/3, 1/2duties or static drive are programmably selectable
- ◆ Dual clock operation
 - Single/dual-clock modes
- ◆ Nine power saving operating modes
 - STOP mode: Oscillation stops. Battery/capacitor back-up. Port output hold/High-impedance.
 - SLOW 1, 2 modes: Low-power consumption operation using low-frequency clock (32.768 kHz)
 - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-

Timer. Release by falling edge of TBTCR < TBTCK > setting.

• IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by

interruputs.

• IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release

by interruputs.

• SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-

Timer. Release by falling edge of TBTCR < TBTCK > setting.

• SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by

interrupts.

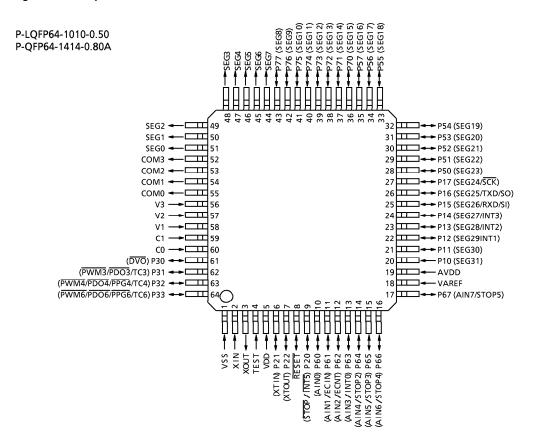
SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release

by interrupts.

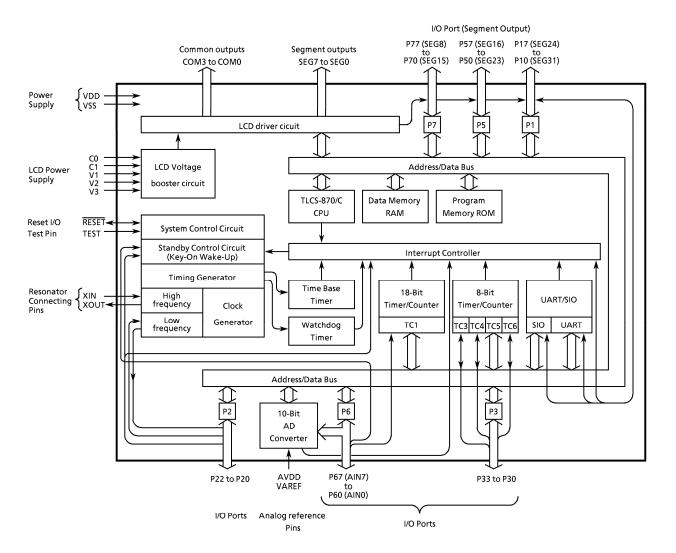
♦ Wide operating voltage: 1.8 to 5.5 V at 4.2 MHz/32.768 kHz,

2.7 to 5.5 V at 8 MHz/32.768 kHz, 4.5 to 5.5 V at 16 MHz/32.768 kHz

Pin Assignments (Top View)



Block Diagram



Pin Functions

Pin Name	Input/Output		Function		
P17 (SEG24, SCK)	1/0 (1/0)		Serial clock input/output		
P16 (SEG25, TxD, SO)	I/O (Output)	8-bit input/output port with latch.	UART data output Serial data output		
P15 (SEG26, RxD, SI)	1/0 (1/0)	When used as input port, an external interrupt input, serial interface input/output or UART data input/	UART data input Serial data input	LCD segment	
P14 (SEG27, INT3)	1/0 (1/0)	output, the P1LCR must be cleared to	External interrupt 3 input	outputs.	
P13 (SEG28, INT2)	1/0 (1/0)	"0" after setting output latch to "1".	External interrupt 2 input		
P12 (SEG29, INT1)	1/0 (1/0)	When used as a LCD segment output, the P1LCR must be set to "1".	External interrupt 1 input		
P11 (SEG30)	I/O (Output)				
P10 (SEG31)	I/O (Output)				
P22 (XTOUT)	I/O (Output)		Resonator connecting pins (32.		
P21 (XTIN)	I/O (Input)	3-bit input/output port with latch. When used as an input port, the	TIN is used and		
P20 (INT5, STOP)	I/O (Input)	output latch must be set to "1".	External interrupt input 5 or ST signal input	OP mode release	
P33 (PWM6, PDO6, PPG6, TC6)	I/O(I/O)	4-bit programmable input/output port (Nch high current output).	Timer counter 6 input/output		
P32 (PWM4, PDO4, PPG4, TC4)	1/0(1/0)	When used as a timer/counter output or divider output, the output latch must be set to "1". When used as an	Timer counter 4 input/output		
P31 (PWM3, PDO3, TC3)	1/0(1/0)	input port or timer/counter input, the P3OUTCR must be cleared to "0"	Timer counter 3 input/output		
P30 (DVO)	I/O(Output)	after P3DR is set to "1".	Divider output		
P57 (SEG16) to P50 (SEG23)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P5LCR must be set to "1".	LCD segment outputs		
P67 (AIN7, STOP5)	I/O (Input)	8-bit programmable input/output	STOP 5 input		
P66 (AIN6, STOP4)	I/O (Input)	port (tri-state). Each bit of this port can be individually configured as an	STOP 4 input		
P65 (AIN5, STOP3)	I/O (Input)	input or an output under software	STOP 3 input		
P64 (AIN4, STOP2)	I/O (Input)	control. When used as an analog input, the P6CR must be cleared to	STOP 2 input	AD converter	
P63 (AIN3, INTO)	I/O (Input)	"0" after clearing output latch to "0".	External interrupt 0 input	analog inputs	
P62 (AIN2, ECNT)	I/O (Input)	When used as an input port, a key on wake up input, an external interrupt			
P61 (AIN1, ECIN)	I/O (Input)	input and timer/counter input, the	Timer/counter 1 input		
P60 (AIN0)	I/O (Input)	P6CR must be clearing to "0" after setting output latch to "1".			
P77 (SEG8) to P70 (SEG15)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the PTLCR must be set to "1".	LCD segment outputs		
SEG7 to SEG0 COM3 to COM0	Output	LCD segment outputs LCD common outputs			
V 3 to V 1	I CD voltage		ro required between CO and C1	nin and \/10/20/2	
C1 to C0	LCD voltage booster pin	LCD voltage booster pin. Capacitors a pin and GND.	·		
XIN, XOUT	Input Output	Resonator connecting pins for high-fre used and XOUT is opened.	quency clock. For inputting ext	ernal clock, XIN is	
RESET	1/0	Reset signal input or watchdog timer ou	utput/address-trap-reset output		
TEST	Input	Test pin for out-going test. Be fixed to l	ow.		
VDD, VSS		+ 5 V, 0 (GND)			
VAREF	Power Supply	Analog reference voltage inputs (High)			
AVDD		AD circuit power supply			

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C829B/H29B/M29B memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C829B/H29B/M29B memory address map. The general-purpose registers are not assigned to the RAM address space.

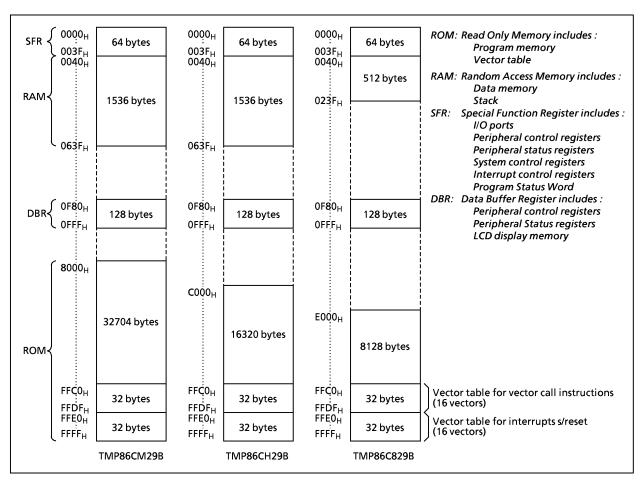


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86C829B has a 8 K×8 bits (address $E000_H$ to FFFF_H), TMP86CH29B has a 16 K×8 bits (address $C000_H$ to FFFF_H), and the TMP87CM29B has a 32 K×8 bits (address 8000_H to FFFF_H) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		- 0.3 to 6.5	
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT1}		- 0.3 to V _{DD} + 0.3	
	I _{OUT1}	P3, P6 Port	- 1.8	
Output Current (Per 1 pin)	I _{OUT2}	P1, P2, P5, P6, P7 Port	3.2	
	I _{OUT3}	P3 Port	30	mA
Output Current (Total)	ΣI _{OUT2}	P1, P2, P5, P6, P7 Port	60	
Output current (Total)	ΣI _{OUT3}	P3 Port	80	
Power Dissipation [T _{opr} = 85 °C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	(Condition	Min	Max	Unit	
			fc = 16 MHz	NORMAL1, 2 modes	4.5			
				IDLE0, 1, 2 modes	4.5			
			6 0 0 0 0 0	NORMAL1, 2 modes	2.7			
			fc = 8 MHz	IDLE0, 1, 2 modes	2.7			
Supply Voltage V _{DD}	V _{DD}			NORMAL1, 2 modes		5.5		
			fc = 4.2 MHz	IDLE0, 1, 2 modes				
			100 700 111 1	SLOW1, 2 modes	1.8			
				SLEEP0, 1, 2 modes				
				STOP mode			V	
	V _{IH1}	Except Hysteresis input	$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.70$			
Input high Level	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$	V_{DD}		
	V _{IH3}		V	_{DD} < 4.5 V	$V_{DD} \times 0.90$			
	V _{IL1}	Except Hysteresis input	.,	_{DD} ≧ 4.5 V		$V_{DD} \times 0.30$		
Input low Level	V _{IL2}	Hysteresis input	V	DD = 4.3 V	0	$V_{DD} \times 0.25$		
	V _{IL3}		V	_{DD} < 4.5 V		$V_{DD} \times 0.10$		
			V_{DD}	= 1.8 to 5.5 V		4.2		
Clock Frequency	fc	XIN, XOUT	V _{DD} = 2.7 to 5.5 V		1.0	8.0	MHz	
Clock Frequency			V _{DD} = 4.5 to 5.5 V			16.0		
	fs	XTIN, XTOUT			30.0	34.0	kHz	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		_	0.9	_	V
	I _{IN1}	TEST					
Input Current	I _{IN2}	Sink Open Drain, Tri-state	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$	_	_	± 2	μA
	I _{IN3}	RESET, STOP					
Innut Posistance	R _{IN1}	TEST Pull-Down		_	70	-	kΩ
Input Resistance	R _{IN2}	RESET Pull-Up		100	220	450	K77
Output Leakage Current	I _{LO}	Sink Open Drain, Tri-state	$V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V/0 V}$	-	-	± 2	μΑ
Output High Voltage	V _{OH2}	C-MOS, Tri-st Port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	-	
Output Low Voltage	V _{OL}	Except XOUT and P3 Port	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{mA}$	_	-	0.4] V
Output Low Current	l _{OL}	High Current Port (P3 Port)	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	_	20	_	
Supply Current in NORMAL 1, 2 modes			$V_{DD} = 5.5 V$ $V_{IN} = 5.3/0.2 V$	-	7.5	9	mA
Supply Current in IDLE 0, 1, 2 modes			fc = 16 MHz fs = 32.768 kHz		5.5	6.5	
Supply Current in SLOW 1 mode	l _{DD}			-	18	42	
Supply Current in SLEEP 1 mode	rrent in	$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$ $fs = 32.768 \text{ kHz}$	-	16	25		
Supply Current in SLEEP 0 mode			LCD driver is not enable.	_	12	20	μΑ
Supply Current in STOP mode			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	_	0.5	10	

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 \text{ V}$

Note 2: Input current (I_{IN1} , I_{IN2}); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

AD Conversion Characteristics

$(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V} \le V_{DD} \le 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		A _{VDD} - 1.0	-	A _{VDD}	
Power Supply Voltage of Analog Control Circuit	A _{VDD}			V _{DD}		v
Analog Reference Voltage Range (Note 4)	$\triangle v_{AREF}$		3.5	-	_	
Analog Input Voltage	V _{AIN}		V _{SS}	-	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.6	1.0	mA
Non linearity Error			-	_	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V},$	-	-	± 2	LSB
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 5.0 \text{ V}$	-	-	± 2	LOB
Total Error		TANEL TO S	-	-	± 2	

$(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V} \le V_{DD} < 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		A _{VDD} - 1.0	-	A _{VDD}	
Power Supply Voltage of Analog Control Circuit	A _{VDD}			V _{DD}] _v
Analog Reference Voltage Range (Note 4)	$\triangle v_{AREF}$		2.5	-	_	1
Analog Input Voltage	V _{AIN}		V _{SS}	-	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 4.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	_	0.5	0.8	mA
Non linearity Error			-	-	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 2.7 \text{ V},$	-	-	± 2	LSB
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 2.7 \text{ V}$	-	-	± 2	1 528
Total Error			_	-	± 2	

(V_{SS} = 0.0 V, 2.0 V \leqq V_{DD} <2.7 V, Topr = -40 to 85°C) Note 5 (V_{SS} = 0.0 V, 1.8 V \leqq V_{DD} <2.0 V, Topr = -10 to 85°C) Note 5

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		A _{VDD} - 0.9	-	A _{VDD}	
Power Supply Voltage of Analog Control Circuit	A _{VDD}			V _{DD}		
Analog Reference Voltage Range (Note 4)	Δv	$1.8 \text{ V} \le \text{V}_{DD} < 2.0 \text{ V}$	1.8	-	_	V
	\triangle V _{AREF}	$2.0 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$	2.0	-	-	
Analog Input Voltage	V _{AIN}		V _{SS}	-	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 2.7 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.3	0.5	mA
Non linearity Error			_	_	± 4	
Zero Point Error		$V_{DD} = A_{VDD} = 1.8 \text{ V},$	_	-	± 4	LCD
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{\Delta REF} = 1.8 \text{ V}$	-	-	± 4	LSB
Total Error		1 AINE	-	-	± 4	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.
- About conversion time, please refer to "2.10.2 Register Framing"
- Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} V_{SS}.

 When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} V_{SS}$ Note 5: When AD is used with $V_{DD} < 2.7 V$, the guaranteed temperature range varies with the operating voltage. Note 6: The A_{VDD} pin should be fixed on the V_{DD} level even though AD convertor is not used.

AC Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 modes				
Machine Cycle Time	tcy	IDLE 1, 2 modes	0.25	_	4	
		SLOW 1, 2 modes	447.6	-	133.3	- μ\$
		SLEEP 1, 2 modes	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	_	31.25	_	ns
Low Level Clock Pulse Width	twcL	fc = 16 MHz				113
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)		15.26	-	
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz	_			μS

$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 modes			4	
Machine Cycle Time	tcy	IDLE 1, 2 modes	0.5	-		
		SLOW 1, 2 modes	447.6		133.3	μS
		SLEEP 1, 2 modes	117.6	_		
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)		62.5	_	ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz	_			113
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)		15.26	-	
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz	_			μS

$(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 2.7 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Machine Cycle Time		NORMAL 1, 2 modes				
	tcy	IDLE 1, 2 modes	0.95	_	4	
		SLOW 1, 2 modes	117.5	-	133.3	μS
		SLEEP 1, 2 modes	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	twcL	fc = 4.2 MHz	_	119.05	_	''3
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)		45.26		
Low Level Clock Pulse Width	twcL	fs = 32.768 kHz	_	15.26	-	μS

Timer Counter 1 input (ECIN) Characteristics $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition		Min	Тур.	Max	Unit
		Frequency measurement mode V _{DD} = 4.5 to 5.5 V	Single edge count	-	-	- 16	
			Both edge count	-	-		MHz
TC1 input (ECIN input)	+	t_{TC1} Frequency measurement mode $V_{DD} = 2.7$ to 4.5 V	Single edge count	-	-	- 8	
TCT Input (ECIN Input)	L LTC1		Both edge count	-	-		
		Frequency measurement mode $V_{DD} = 1.8$ to 2.7 V	Single edge count	-	-	4.2	
			Both edge count	_	_		

Recommended Oscillating Conditions - 1

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Development		Oscillation			Recommended Constant	
Parameter Oscillator		Frequency	Recommended Oscillator		C ₁	C ₂
High-Frequency	Ceramic Resonator	16 MHz	MURATA	CSTLS16M0X51-B0	5pF (built-in)	5pF (built-in)
Oscillation				CSTCV16M0X51J-R0	5pF (built-in)	5pF (built-in)

Recommended Oscillating Conditions - 2

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Davamatar	0.111.1	Oscillation			Recommended Constant	
Parameter Oscillator		Frequency	Recommended Oscillator		C ₁	C ₂
High-Frequency	Ceramic Resonator	8 MHz	MURATA	CSTLS8M00G53-B0	15pF (built-in)	15pF (built-in)
Oscillation				CSTCE8M00G55-R0	33pF (built-in)	33pF (built-in)

Recommended Oscillating Conditions - 3

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.0 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Danamatan		Oscillation			Recommended Constant	
Parameter	Oscillator	Frequency	Recom	ended Oscillator	C ₁	C ₂
High-Frequency Oscillation	Ceramic Resonator	4.19 MHz	MURATA	CSTLS4M19G56-B0	47pF (built-in)	47pF (built-in)

Recommended Oscillating Conditions - 4

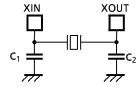
 $(V_{SS} = 0 \text{ V}, V_{DD} = 1.9 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter Oscillator	0.311.4	Oscillation			Recommended Constant	
	Frequency	Recommended Oscillator		C ₁	C ₂	
High-Frequency Oscillation	Ceramic Resonator	4.19 MHz	MURATA	CSTCR4M19G55-R0	39pF (built-in)	39pF (built-in)

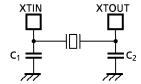
Recommended Oscillating Conditions - 5

 $(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Oscillator	Oscillation	Barrage and ad Oasillaton	Recommended Constant	
		Frequency	Recommended Oscillator	C ₁	C ₂
High-Frequency Oscillation	Ceramic Resonator	4.19 MHz	MURATA CSTLS4M19G56U-B0	47pF (built-in)	47pF (built-in)
			CSTCR4M19G55093-R0	39pF (built-in)	39pF (built-in)
		2 MHz	MURATA CSTLS2M00G56-B0	47pF (built-in)	47pF (built-in)
			CSTCC2M00G56-R0	47pF (built-in)	47pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;http://www.murata.co.jp/search/index.html