

8,1 mm x 11 mm

SLVS334A – DECEMBER 2000 – REVISED SEPTEMBER 2001

## MOBILE CPU POWER SUPPLY CONTROLLER

### FEATURES

- Power Stage Input Voltage Range of 3 V to 28 V
- Single-Chip Dynamic Output Voltage Transition Solution
- Hysteretic Controller Provides Fast Transient Response Time and Reduced Output Capacitance
- Two Linear Regulator Controllers Regulating Clock and I/O Voltages
- Internal 2-A (Typ) Gate Drivers With Bootstrap Diode For Increased Efficiency
- 5-Bit Dynamic VID
- Active Droop Compensation Enables Tight Dynamic Regulation for Reduced Output Capacitance
- VGATE Terminal Provides Power-Good Signal for All Three Outputs
- Enable External Terminal (ENABLE\_EXT)
- 32-Pin TSSOP PowerPAD™ Enhances Thermal Performance
- 1% Reference Voltage Accuracy

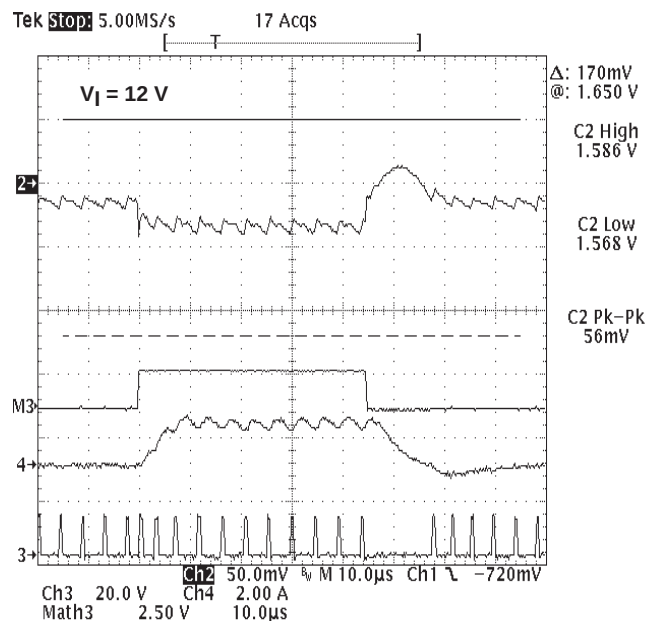
### APPLICATIONS

- Intel Mobile CPUs With SpeedStep™ Technology
- AMD Mobile CPUs With PowerNow!™ Technology
- DSP Processors
- Other One, Two, or Three Output Point-of-Load Applications

### DESCRIPTION

The TPS5300 is a hysteretic synchronous-buck controller, with two on-chip linear regulator controllers, incorporating dynamic output voltage positioning

technology. The TPS5300 provides a precise, programmable supply voltage to a mobile processor or other processor power applications. A ripple regulator provides the core voltage, while two linear regulator drivers regulate external NPN power transistors for the I/O and CLK voltages. A 5-bit voltage identification (VID) DAC allows programming for the ripple regulator voltage to values between 0.925 V to 1.275 V in 25-mV steps and 1.3 V to 2 V in 50-mV steps. Other voltage ranges and steps can be easily set. The fast transient response time and active voltage DROOP positioning reduce the number of output capacitors required to keep the output voltage within tight dynamic voltage regulation limits. The power saving mode (PSM) allows the user to select a single operating ramp or allows the controller to automatically switch to lower frequencies at low loads. The high-gain current sense differential amplifier allows the use of small-value sense resistors that minimize conduction losses.


**Output Voltage Transient Load Response**


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PowerNow is a trademark of Advanced Micro Devices Inc.

PowerPAD is a trademark of Texas Instruments.

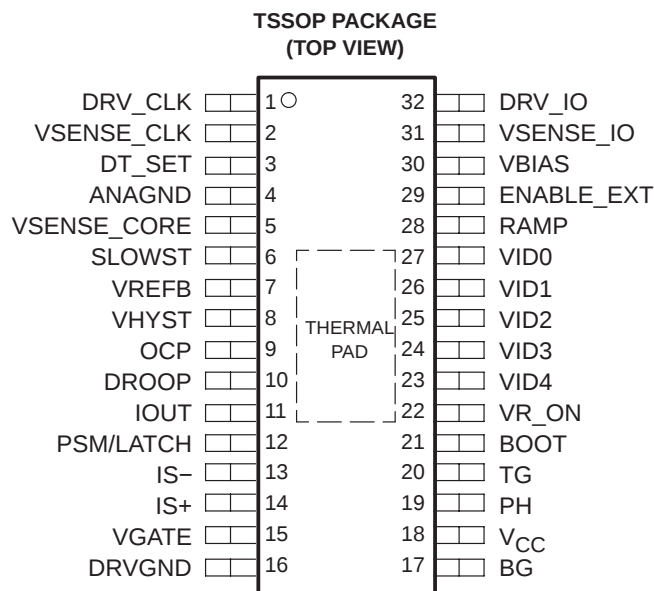
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## description (continued)

The TPS5300 includes high-side and low-side gate drivers rated at 2 A typical, that enable efficient operation at higher frequencies and drive larger or multiple power MOSFETs (such as 50-A output current applications). An adaptive dead-time circuit minimizes dead-time losses while preventing cross-conduction of high-side and low-side switches. All three outputs power up together as they track the same user programmable slowstart voltage. The enable external (ENABLE\_EXT) terminal allows the TPS5300 to activate external switching controllers for additional system power requirements.

The TPS5300 features  $V_{CC}$  undervoltage lockout, output overvoltage protection, output undervoltage protection, and user-programmable overcurrent protection, and is packaged in a small 32-pin TSSOP PowerPAD package.

## pin assignments



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

|                                                                                                                             |                                            |
|-----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|
| Supply voltage, $V_{CC}$ .....                                                                                              | 7 V                                        |
| Input voltage, $V_I$ : VBIAS .....                                                                                          | 7 V                                        |
| VR_ON .....                                                                                                                 | 6 V                                        |
| VID0, VID1, VID2, VID3, VID4 .....                                                                                          | 6 V                                        |
| PSM/LATCH .....                                                                                                             | 6 V                                        |
| IS-, IS+ .....                                                                                                              | 6 V                                        |
| RAMP .....                                                                                                                  | 35 V                                       |
| VSENSE_CORE .....                                                                                                           | 6 V                                        |
| VSENSE_IO .....                                                                                                             | 6 V                                        |
| VSENSE_CLK .....                                                                                                            | 6 V                                        |
| All other input terminals .....                                                                                             | 7 V                                        |
| BOOT to DRV_GND voltage (high-side driver on) .....                                                                         | 35 V                                       |
| BOOT to PH voltage .....                                                                                                    | 7 V                                        |
| BOOT to TG voltage .....                                                                                                    | 7 V                                        |
| PH to DRV_GND voltage .....                                                                                                 | -1 V to 35 V                               |
| ANAGND to DRV_GND voltage .....                                                                                             | ±1 V                                       |
| Output voltage, $V_O$ : VGATE .....                                                                                         | 6 V                                        |
| ENABLE_EXT .....                                                                                                            | 6 V                                        |
| Continuous power dissipation, $P_D$ : Without PowerPad soldered, $T_A = 25^\circ\text{C}$ , $T_J = 125^\circ\text{C}$ ..... | 1.2 W                                      |
| With PowerPad soldered, $T_C = 25^\circ\text{C}$ , $T_J = 125^\circ\text{C}$ .....                                          | 6.25 W                                     |
| Operating junction temperature, $T_J$ .....                                                                                 | $0^\circ\text{C}$ to $125^\circ\text{C}$   |
| Storage temperature, $T_{stg}$ .....                                                                                        | $-65^\circ\text{C}$ to $150^\circ\text{C}$ |
| Lead temperature, $T_{(lead)}$ (soldering, 10 seconds) .....                                                                | $300^\circ\text{C}$                        |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

| PWP                | $T_A < 25^\circ\text{C}$ | Derating Factor <sup>‡</sup> | $T_A = 70^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ |
|--------------------|--------------------------|------------------------------|--------------------------|--------------------------|
| PowerPAD mounted   | 3.58 W                   | 0.0358 W/ $^\circ\text{C}$   | 1.96 W                   | 1.43 W                   |
| PowerPAD unmounted | 1.78 W                   | 0.0178 W/ $^\circ\text{C}$   | 0.98 W                   | 0.71 W                   |

**JUNCTION-CASE THERMAL RESISTANCE TABLE**

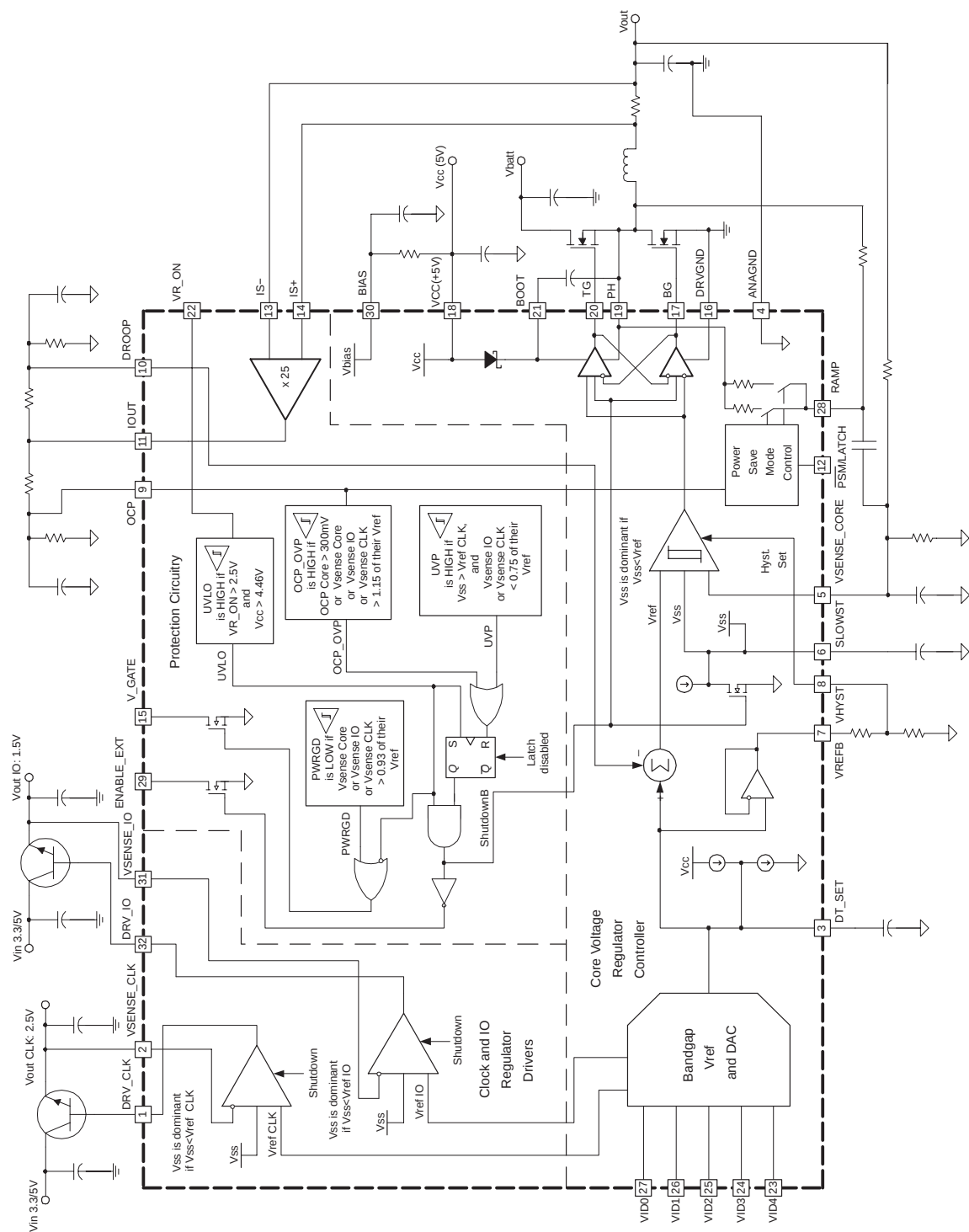
|                                  |                                |
|----------------------------------|--------------------------------|
| Junction-case thermal resistance | 0.72 $^\circ\text{C}/\text{W}$ |
|----------------------------------|--------------------------------|

<sup>‡</sup> Test Board Conditions:

1. Thickness: 0.062"
2. 3" x 3" (for packages < 27 mm long)
3. 4" x 4" (for packages > 27 mm long)
4. 2 oz. Copper traces located on the top of the board (0,071 mm thick )
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1 oz. Copper (0,036 mm thick)
7. Thermal vias, 0,33 mm diameter, 1,5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief SLMA002.

functional schematic



**recommended operating conditions,  $0 < T_J < 125^{\circ}\text{C}$  (unless otherwise noted)**

|                                                                        | MIN | NOM  | MAX | UNIT |
|------------------------------------------------------------------------|-----|------|-----|------|
| Supply voltage, $V_{\text{batt}}$                                      | 3   | 12.5 | 28  | V    |
| Linear regulator supply voltage, $V_{\text{I(}(\text{IO}+\text{CLK})}$ | 3   | 3.3  | 6   | V    |
| Supply voltage range, $V_{\text{CC}}$ , $V_{\text{BIAS}}$              | 4.5 | 5    | 6   | V    |

**dc and ac electrical characteristics over recommended operating free-air temperature range,  $0 < T_J < 125^{\circ}\text{C}$ ,  $V_{\text{IN}} = 3\text{ V} - 28\text{ V}$  (unless otherwise noted)**

| PARAMETER                                     |                                                                                     | TEST CONDITIONS                                                                            | MIN   | TYP | MAX  | UNIT              |
|-----------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-------|-----|------|-------------------|
| Reference/Voltage Identification              |                                                                                     |                                                                                            |       |     |      |                   |
| V <sub>IH</sub> (VID)                         | High-level input voltage, D0–D4                                                     | Current source pullup to V <sub>CC</sub>                                                   | 2.25  |     |      | V                 |
| V <sub>IL</sub> (VID)                         | Low-level input voltage, D0–D4                                                      |                                                                                            |       |     | 1    | V                 |
| Cumulative Reference (see Note 1)             |                                                                                     |                                                                                            |       |     |      |                   |
| V(CUM_ACCRR)                                  | Initial accuracy ripple regulator                                                   | 0.925 V ≤ V <sub>ref(core)</sub> ≤ 2 V,<br>Hysteresis window = 30 mV (see Note 2)          | –1.5% |     | 1.5% |                   |
|                                               |                                                                                     | 0.925 V ≤ V <sub>ref(core)</sub> ≤ 2 V, T <sub>J</sub> = 25°C<br>Hysteresis window = 30 mV | –1%   |     | 1%   |                   |
| Buffered Reference                            |                                                                                     |                                                                                            |       |     |      |                   |
| V <sub>O</sub> (VREFB)                        | Output voltage, VREFB                                                               | I(VREFB) = 50 μA (see Note 2)                                                              | –2.5% |     | 2.5% |                   |
| Hysteretic Comparator (core)                  |                                                                                     |                                                                                            |       |     |      |                   |
| t <sub>PHL</sub> (HC)                         | Propagation delay time from (AC)<br>VSENSE_CORE to TG or BG<br>(excluding deadtime) | 20-mV overdrive, pulse<br>0.925 V ≤ V <sub>ref</sub> ≤ 2 V (see Note 2)                    |       | 220 | 250  | ns                |
| t <sub>PHL</sub> (HC_ramp)                    |                                                                                     | Ramp circuit from 0 into 26 mV ramp<br>(see Note 2)                                        |       | 220 |      | ns                |
| Overcurrent Protection (core)                 |                                                                                     |                                                                                            |       |     |      |                   |
| V(OCP)                                        | Trip point, OCP                                                                     | Normal operation                                                                           | 235   | 300 | 365  | mV                |
|                                               |                                                                                     | During dynamic VID change                                                                  |       | 400 |      |                   |
| Overvoltage Protection (core, IO, CLK)        |                                                                                     |                                                                                            |       |     |      |                   |
| V(OVP)                                        | Trip point, OVP                                                                     | Upper threshold                                                                            | 111   | 115 | 119  | %V <sub>ref</sub> |
| Undervoltage Protection (IO, CLK)             |                                                                                     |                                                                                            |       |     |      |                   |
| V(UVP)                                        | Trip point, UVP                                                                     | Lower threshold                                                                            |       | 75  |      | %V <sub>ref</sub> |
| Bias UVLO (Resets fault latch)                |                                                                                     |                                                                                            |       |     |      |                   |
| V <sub>IT</sub> (start UVLO)                  | Start threshold                                                                     |                                                                                            |       |     | 4.46 | V                 |
| V <sub>IT</sub> (stop UVLO)                   | Stop threshold                                                                      |                                                                                            | 3.3   |     |      | V                 |
| V <sub>hys</sub>                              | Hysteresis                                                                          |                                                                                            |       | 500 |      | mV                |
| VBIAS quiescent current, I <sub>(ving1)</sub> |                                                                                     | VR_ON connected to GND and V <sub>I</sub> above<br>UVLO start threshold                    |       | 20  |      | μA                |
| VR_ON UVLO (Resets fault latch)               |                                                                                     |                                                                                            |       |     |      |                   |
| V <sub>IT</sub> (start VR_ON)                 | Start threshold                                                                     |                                                                                            |       |     | 2.5  | V                 |
| V <sub>IT</sub> (stop VR_ON)                  | Stop threshold                                                                      |                                                                                            | 1.3   |     |      | V                 |
| V <sub>hys</sub>                              | Hysteresis                                                                          |                                                                                            |       | 475 |      | mV                |

NOTES: 1. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals to the average of the low-level and high-level thresholds of the hysteretic comparator.  
2. Ensured by design, not production tested.

electrical characteristics over recommended operating free-air temperature range,  $0 < T_J < 125^{\circ}\text{C}$ ,  
 $V_{IN} = 3\text{ V} - 28\text{ V}$  (unless otherwise noted) (continued)

| PARAMETER                                                                               |                                                                             | TEST CONDITIONS                                                                                        | MIN  | TYP  | MAX  | UNIT  |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------|------|------|-------|
| Slowstart                                                                               |                                                                             |                                                                                                        |      |      |      |       |
| I(chg)                                                                                  | Charge current (I(chg) = (I(REFB)/5)                                        | V(SS) = 0.5 V,<br>I(VREFB) = 65 μA VREFB = 1.35 V,<br>I(chg) = (I(VREFB)/5)                            | 10.4 | 13   | 15.6 | μA    |
| I(dischg)                                                                               | Discharge current                                                           | V(SS) = 1.35 V,<br>Design for VIN(min) = 4.5 V                                                         |      | 3    |      | mA    |
| VGATE (CORE, IO, CLK) (PWRGD of three outputs with open drain output)                   |                                                                             |                                                                                                        |      |      |      |       |
| V(VGATE)                                                                                | Undervoltage trip point<br>(VSENSE_CORE, VSENSE_IO, and<br>VSENSE_CLK)      | VIN and V(drv) above UVLO thresholds                                                                   | 85   | 90   | 95   | %Vref |
| VO(VGATE)                                                                               | Output saturation voltage                                                   | IO = 2.5 mA                                                                                            |      | 0.5  | 0.75 | V     |
| Enable EXT (SHUTDOWN of IC with open-drain output. Use pullup resistor to 5 V or 3.3 V) |                                                                             |                                                                                                        |      |      |      |       |
| VO(EN_EXT)                                                                              | Output saturation voltage                                                   | IO = 2.5 mA                                                                                            |      | 0.5  | 0.75 | V     |
| DROOP Compensation                                                                      |                                                                             |                                                                                                        |      |      |      |       |
|                                                                                         | Maximum output CMR                                                          |                                                                                                        |      | 200  |      | mV    |
| tPHL(HC)                                                                                | Propagation delay                                                           | 15-mV to 150-mV swing,<br>0.925 V ≤ Vref ≤ 2 V, VCC = 5 V<br>(see Note 2)                              |      | 200  | 500  | ns    |
| Current Sensing                                                                         |                                                                             |                                                                                                        |      |      |      |       |
| G(CS)                                                                                   | Gain                                                                        | See Note 2                                                                                             |      | 25   |      | V/V   |
| VO(SO)                                                                                  | Output systematic offset                                                    | V(IS+) – V(IS–) = 1 mV,<br>1 mV input (see Note 2)                                                     |      | 26   |      | mV    |
| VO(RO)                                                                                  | Output random offset                                                        | See Note 2                                                                                             |      | ±15  |      | mV    |
| VOM                                                                                     | Maximum output voltage swing                                                |                                                                                                        |      | 1.75 |      | V     |
| t(VDSRESP)                                                                              | Response time (measured from 50% of<br>(V(IS+) – V(IS–)) to 50% of V(IOUT)) | V(IS–) = 0.925 V – 2 V, V(IS+) is pulsed<br>from V(IS–) to (V(IS–) + 50 mV),<br>VCC = 5 V (see Note 2) |      |      | 500  | ns    |
| PSM/LATCH Power Saving Mode (PSM Comparator)                                            |                                                                             |                                                                                                        |      |      |      |       |
| V(startINH)                                                                             | PSM comparator start threshold                                              |                                                                                                        | 2.1  | 2.3  |      | V     |
| V(stopINH)                                                                              | PSM comparator stop threshold                                               |                                                                                                        | 1.8  |      |      | V     |
| Vhys(INH)                                                                               | Hysteresis                                                                  |                                                                                                        | 100  |      |      | mV    |
| V(PSMth1)                                                                               | OCP voltage trip points for PSM                                             | OCP↑                                                                                                   | 90   | 120  | 150  | mV    |
| V(PSMth2)                                                                               |                                                                             |                                                                                                        | 30   | 60   | 90   |       |
| V(PSMth3)                                                                               |                                                                             |                                                                                                        |      |      |      |       |
| V(PSMth4)                                                                               |                                                                             |                                                                                                        |      |      |      |       |
| Vhys(PSM)                                                                               | Hysteresis                                                                  |                                                                                                        | 10   |      |      | mV    |
| R(tPSM1)                                                                                | PSM ramp timing resistance                                                  | PH to CT, PSM = GND,<br>V(OCP) = 150 mV (see Note 3)                                                   | 8    | 10   | 12   | kΩ    |
| R(tPSM2)                                                                                |                                                                             | PH to CT, PSM = GND,<br>V(OCP) = 85 mV (see Note 3)                                                    | 16   | 20   | 24   |       |
| R(tPSM3)                                                                                |                                                                             | PH to CT, PSM = GND,<br>V(OCP) = 15 mV (see Note 3)                                                    | 1    |      |      |       |

NOTES: 2. Ensured by design, not production tested.

3. The VBIAS voltage is required to be a quiet bias supply for the TPS5300 control logic. External noisy loads should use VCC instead of the VBIAS voltage.

electrical characteristics over recommended operating free-air temperature range,  $0 < T_J < 125^{\circ}\text{C}$ ,  $V_{\text{IN}} = 3\text{ V} - 28\text{ V}$  (see test circuits) (unless otherwise noted) (continued)

| PARAMETER                             |                                            | TEST CONDITIONS                                                                            | MIN          | TYP   | MAX | UNIT |
|---------------------------------------|--------------------------------------------|--------------------------------------------------------------------------------------------|--------------|-------|-----|------|
| PSM/LATCH Fault Latch Disable         |                                            |                                                                                            |              |       |     |      |
| V(No_Latch/PSM)                       | Disable latch threshold<br>PSM enabled     |                                                                                            | VBIAS + 0.7  |       |     | V    |
| V(No_Latch)                           | Disable latch threshold<br>PSM disabled    |                                                                                            | ANAGND – 0.7 |       |     | V    |
| V(Latch_enabled)                      | Enable latch threshold                     |                                                                                            | ANAGND       | VBIAS |     | V    |
| Thermal Shutdown                      |                                            |                                                                                            |              |       |     |      |
| T(OTP)                                | Over temperature trip<br>point             | See Note 2                                                                                 | 155          |       |     | °C   |
| T(hyst)                               | Hysteresis                                 | See Note 2                                                                                 | 25           |       |     | °C   |
| Dynamic VID Change (No current limit) |                                            |                                                                                            |              |       |     |      |
| IΔtSRC/SNK                            | Voltage change timing<br>current           | VCC = 5 V, V(ref1) = 1.35 V,<br>DT_SET = 0.925 Vsrc/Vsnk                                   | 14           |       |     | μA   |
| Output Drivers (see Note 4)           |                                            |                                                                                            |              |       |     |      |
| IO(src_TG)                            | Peak output current (see<br>Notes 2 and 4) | Duty cycle < 2%, tpw < 100 μs,<br>V(BOOT) – V(PH) = 4.5 V,<br>V(TG) – V(PH) = 0.5 V (src)  | 1.2          | 2     |     | A    |
| IO(sink_TG)                           |                                            | Duty cycle < 2%, tpw < 100 μs,<br>V(BOOT) – V(PH) = 4.5 V,<br>V(TG) – V(PH) = 4 V (sink)   | 1.2          | 3.3   |     | A    |
| IO(src_BG)                            |                                            | Duty cycle < 2%, tpw < 100 μs,<br>VCC = 4.5 V, V(BG) = 0.5 V (src)                         | 1.4          | 2     |     | A    |
| IO(sink_BG)                           |                                            | Duty cycle < 2%, tpw < 100 μs,<br>VCC = 4.5 V, V(BG) = 4 V (src)                           | 1.3          | 3.3   |     | A    |
| ro(src_TG)                            | Output resistance (see<br>Note 4)          | V(BOOT) – V(PH) = 4.5 V, V(TG) = 4 V                                                       | 2.5          |       |     | Ω    |
| ro(sink_TG)                           |                                            | V(BOOT) – V(PH) = 4.5 V, V(TG) = 0.5 V                                                     | 1.5          |       |     | Ω    |
| ro(src_BG)                            |                                            | VCC = 4.5 V, V(BG) = 4 V                                                                   | 2.5          |       |     | Ω    |
| ro(sink_BG)                           |                                            | VCC = 4.5 V, V(BG) = 0.5 V                                                                 | 1.5          |       |     | Ω    |
| tf(TG)                                | TG fall time (AC) (see<br>Note 5)          | CI = 3.3 nF, V(BOOT) = 4.5 V,<br>V(PH) = GND                                               | 10           |       |     | ns   |
| tr(TG)                                | TG rise time (AC) (see<br>Note 5)          |                                                                                            |              |       |     |      |
| tf(BG)                                | BG fall time (AC) (see<br>Note 5)          | CI = 3.3 nF, VCC = 4.5 V                                                                   | 10           |       |     | ns   |
| tr(BG)                                | BG rise time (AC) (see<br>Note 5)          |                                                                                            |              |       |     |      |
| High-Side Driver Quiescent Current    |                                            |                                                                                            |              |       |     |      |
| IQ(highdrq1)                          | Highdrive (TG)<br>quiescent current        | VR_ON grounded, or VCC below UVLO<br>threshold; V(BOOT) = 5 V,<br>PH grounded (see Note 2) | 2            |       |     | μA   |

NOTES: 2. Ensured by design, not production tested.

4. The pulldown (sink) circuit of the high-side driver is a MOSFET transistor referenced to  $DRV_{\text{GND}}$ . The driver circuits are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current rating from the bipolar and MOSFET transistors. The output resistance is the  $r_{\text{ds(on)}}$  of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.
5. Rise and fall times are measured from 10% to 90% of pulsed values.

electrical characteristics over recommended operating free-air temperature range,  $0 < T_J < 125^{\circ}\text{C}$ ,  
 $V_{IN} = 3\text{ V} - 28\text{ V}$  (see test circuits) (unless otherwise noted) (continued)

| PARAMETER                                                     |                                                                 | TEST CONDITIONS                                                                                                 | MIN    | TYP | MAX   | UNIT          |
|---------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|--------|-----|-------|---------------|
| <b>Adaptive Deadtime Circuit</b>                              |                                                                 |                                                                                                                 |        |     |       |               |
| $V_{IH(TG)}$                                                  | TG – PH High-level input voltage                                | $V_{(IS-)} = 0.925\text{ V} - 2\text{ V}$ (see Note 2)                                                          | 2.4    |     |       | V             |
| $V_{IL(TG)}$                                                  | TG – PH Low-level input voltage                                 | $V_{(IS-)} = 0.925\text{ V} - 2\text{ V}$ (see Note 2)                                                          |        |     | 1.33  | V             |
| $V_{IH(BG)}$                                                  | BG High-level input voltage                                     | $V_{(IS-)} = 0.925\text{ V} - 2\text{ V}$ (see Note 2)                                                          | 3      |     |       | V             |
| $V_{IL(BG)}$                                                  | BG Low-level input voltage                                      | $V_{(IS-)} = 0.925\text{ V} - 2\text{ V}$ (see Note 2)                                                          |        |     | 1.7   | V             |
| $t_{(NUL)}$                                                   | Driver nonoverlap time (AC)                                     | CBG = 9 nF, 10% threshold on BG,<br>$V_{CC} = 5\text{ V}$ (see Note 2)                                          |        |     | 50    | ns            |
| <b>Linear Regulator OUTPUT DRIVERS (IO, CLK) (see Note 4)</b> |                                                                 |                                                                                                                 |        |     |       |               |
| $I_{O(src\_LDODR\_IO)}$                                       | Peak output current linear regulator driver IO                  | $V_{CC} = 5\text{ V}$ ,<br>$V_{SENSE\_IO} = 0.9 \times V_{(REF\_IO)}$<br>(see Note 2)                           | 134    |     |       | mA            |
| $I_{O(sink\_LDODR\_IO)}$                                      |                                                                 | $V_{CC} = 5\text{ V}$ ,<br>$V_{SENSE\_IO} = 1.1 \times V_{(REF\_IO)}$<br>(see Note 2)                           | 14     |     |       | $\mu\text{A}$ |
| $V_{(CUM\_ACC\_IO)}$                                          | Initial accuracy IO condition:<br>closed loop; linear regulator | $V_{CC} = 5\text{ V}$ , $V_{ref} = 1.5\text{ V}$ , $I_O = 134\text{ mA}$                                        | -1.7%  |     | 1.7%  |               |
| $V_{(CC\_Line\_Reg\_IO)}$                                     | $V_{IN}$ line regulation IO                                     | $5.5\text{ V} \geq V_{CC} \geq 4.5\text{ V}$ ,<br>$3\text{ V} \leq V_{IN} (IO) \leq 6\text{ V}$ , (see Note 2)  |        | 5   |       | mV            |
| $I_{O(src\_LDODR\_CLK)}$                                      | Peak output current regulator, driver CLK                       | $V_{CC} = 5\text{ V}$ ,<br>$V_{SENSE\_IO} = 0.9 \times V_{O(REF\_IO)}$<br>(see Note 2)                          | 10     |     |       | mA            |
| $I_{O(sink\_LDODR\_CLK)}$                                     |                                                                 | $V_{CC} = 5\text{ V}$ ,<br>$V_{SENSE\_IO} = 1.1 \times V_{O(REF\_IO)}$<br>(see Note 2)                          | 14     |     |       | $\mu\text{A}$ |
| $V_{(CUM\_ACCCLK)}$                                           | Initial accuracy CLK condition:<br>closed loop                  | $V_{CC} = 5\text{ V}$ , $V_{ref} = 2.5\text{ V}$ , $I_O = 10\text{ mA}$                                         | -1.55% |     | 1.55% |               |
| $V_{CC(LineReg\_CLK)}$                                        | Line regulation CLK                                             | $5.5\text{ V} \geq V_{CC} \geq 4.5\text{ V}$ ,<br>$3\text{ V} \leq V_{IN} (CLK) \leq 6\text{ V}$ , (see Note 2) |        | 5   |       | mV            |

NOTES: 2. Ensured by design, not production tested.

4. The pulldown (sink) circuit of the high-side driver is a MOSFET transistor referenced to DRVGN. The driver circuits are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current rating from the bipolar and MOSFET transistors. The output resistance is the  $r_{ds(on)}$  of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

## Terminal Functions

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                         |
|------------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ANAGND           | 4   |     | Analog ground                                                                                                                                                                                                                                                                                                                                                                                       |
| BG               | 17  | O   | Bottom gate drive. BG is an output drive to the low-side synchronous rectifier FET.                                                                                                                                                                                                                                                                                                                 |
| BOOT             | 21  | I   | Bootstrap. Connect a 1-μF low-ESR ceramic capacitor to PH to generate a floating drive for the high-side FET driver.                                                                                                                                                                                                                                                                                |
| DROOP            | 10  | I   | Active voltage droop position voltage. DROOP is a voltage input used to set the amount of output-voltage, set-point droop as a function of load current. The amount of droop compensation is set with a resistor divider between IOUT and ANAGND. A voltage divider from V <sub>O</sub> to VSENSE_CORE sets the no-load offset.                                                                     |
| DRV_CLK          | 1   | O   | CLK voltage regulator. DRV_CLK drives an external NPN bipolar power transistor for regulating CLK voltage to VREF_CLK.                                                                                                                                                                                                                                                                              |
| DRVGND           | 16  |     | Drive ground. Ground for FET drivers. Connect to FET PWRGND                                                                                                                                                                                                                                                                                                                                         |
| DRV_IO           | 32  | O   | Drives an external NPN bipolar power transistor for regulating IO voltage to VREF_IO.                                                                                                                                                                                                                                                                                                               |
| DT_SET           | 3   | I   | DT_SET sets the transition time for speed step output voltage positioning. Attach a capacitor from DT_SET to ground to program time.                                                                                                                                                                                                                                                                |
| ENABLE_EXT       | 29  | O   | Open drain output. ENABLE_EXT enables the external converters when the internal enable signal is high (good), and disables when there is a fault with any regulator (OVP, UVP, OCPrr), VR_ON UVLO is low, or the VBIAS UVLO is low. Can be connected to the enable terminal of an external linear regulator or switching controller. A pullup resistor is required to set the desired voltage rail. |
| IS-              | 13  | I   | Current sense negative Kelvin connection. Connect to the node between the current sense resistor and the output capacitors. Keep the PCB trace short and route trace next to the IS+ trace to help reduce loop inductance noise pickup and cancel common mode noise through mutual coupling.                                                                                                        |
| IS+              | 14  | I   | Current sense positive Kelvin connection. Connect to the node between the output inductor and the current sense resistor. Keep the PCB trace short and route trace next to the IS-trace to help reduce loop inductance noise and cancel common mode noise through mutual coupling.                                                                                                                  |
| IOUT             | 11  | O   | Current sense differential amplifier output. The voltage on IOUT equals $25 \times (V_{I(+)} - V_{I(-)}) = 25 \times (R_{\text{sense}}) \times I_L$ .                                                                                                                                                                                                                                               |
| OCP              | 9   | I   | Overcurrent protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND. The typical OCP trip point should be set at $1.30 \times I_{(\text{max})}$ . The OCP voltage also sets the PSM automatic trip points.                                                                                                                                                      |
| PH               | 19  | I/O | Phase voltage node. PH is used for bootstrap low reference. PH connects to the junction of the high-side and low-side FET's.                                                                                                                                                                                                                                                                        |
| PSM/LATCH        | 12  | I   | PSM. Power saving mode boosts efficiency at low-load current by automatically decreasing the switching frequency toward the natural converter operating frequency. A logic low (<1.8) disables PSM, maintaining the higher switching frequency range set by ramp components. See Figure 1.<br>LATCH. Allows disabling fault latch. Recommend enabling fault latch protection                        |
| RAMP             | 28  | I/O | Sets a ramp on the feedback signal to increase the switching frequency. Add a resistor from PH to RAMP and connect RAMP to VSENSE_CORE for a dc-coupled ramp. Add a capacitor from RAMP to VSENSE_CORE to set an ac-coupled ramp.                                                                                                                                                                   |
| SLOWST           | 6   | I   | Slowstart (softstart). A capacitor from SLOWST to GND sets the slowstart time for the ripple regulator and the two linear regulators. The three converters will ramp up together while tracking the output voltage. A current equal to $I_{(\text{VREFB})}/5$ charges the capacitor.                                                                                                                |
| TG               | 20  | O   | Top gate drive. TG is an output drive to the high-side power switching FET's. It is also used in the anticross-conduction circuit to eliminate shoot-through current.                                                                                                                                                                                                                               |
| VBIAS            | 30  | I   | Analog VBIAS. It is recommended that at least a 1-μF capacitor be connected to ANAGND. Supply from V <sub>CC</sub> through RC filter                                                                                                                                                                                                                                                                |
| V <sub>CC</sub>  | 18  |     | Supply voltage. V <sub>CC</sub> is the supply voltage for the FET drivers. Add an external resistor/capacitor filter from V <sub>CC</sub> to VBIAS. It is recommended that a 1-μF capacitor be connected to the DRVGND terminal.                                                                                                                                                                    |
| VGATE            | 15  | O   | Logical and output of the combined core, IO, and CLK powergood. VGATE outputs a logic high when all (core, IO, CLK) output voltages are within 7% of the reference voltage. An open drain output allows setting to desired voltage level through a pullup resistor.                                                                                                                                 |

## Terminal Functions (Continued)

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION                                                                                                                                                                                                                                                                      |
|------------------|-----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VHYST            | 8   | I   | Ripple regulator hysteresis set terminal. The hysteresis is set with a resistor divider from VREFB to ANGND. The hysteresis voltage window will be $\pm$ the voltage between VREFB and VHYST.                                                                                    |
| VID0             | 27  | I   | Voltage identification inputs 0, 1, 2, 3, and 4. These terminals are digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in the terminal functions table. These terminals are internally pulled up to VBIAS. |
| VID1             | 26  | I   |                                                                                                                                                                                                                                                                                  |
| VID2             | 25  | I   |                                                                                                                                                                                                                                                                                  |
| VID3             | 24  | I   |                                                                                                                                                                                                                                                                                  |
| VID4             | 23  | I   |                                                                                                                                                                                                                                                                                  |
| VREFB            | 7   | O   | Buffered ripple regulator reference voltage from VID network                                                                                                                                                                                                                     |
| VR_ON            | 22  | I   | Enables the drive signals to the MOSFET drivers. The comparator input can be used to monitor voltage, such as the linear regulators' input supply using a resistor divider.                                                                                                      |
| VSENSE_CLK       | 2   | I   | CLK feedback voltage sense. Connect to CLK linear regulator output voltage to regulate.                                                                                                                                                                                          |
| VSENSE_CORE      | 5   | I   | Feedback voltage sense input for the core. Connect to ripple regulator output voltage to sense and regulate output voltage. It is recommended that an RC low-pass filter be connected at this pin to filter high-frequency noise.                                                |
| VSENSE_IO        | 31  | I   | I/O feedback voltage sense. Connect to I/O linear regulator output voltage to regulate.                                                                                                                                                                                          |

## detailed description

## reference/voltage identification

The reference /voltage programming (VP) section consists of a temperature-compensated, bandgap reference and a 5-bit voltage selection network. The five VID pins are inputs to the VID selection network and are TTL compatible inputs that are internally pulled up to  $V_{CC}$  with pullup resistors. The internal reference voltage can be programmed from 0.925 V to 2 V with the VID pins. The VID codes are listed in Table 1. The output voltage of the VP network,  $V_{ref}$ , is within  $\pm 1.5\%$  of the nominal setting. The  $\pm 1.5\%$  tolerance is over the full VP range of 0.925 V to 2 V, and includes a junction temperature range of 0°C to 125°C, and a  $V_{CC}$  range of 4.5 V to 5.5 V. The output of the reference/VP network is indirectly brought out through a buffer to the VREFB pin. The voltage on this pin will be within  $\pm 5$  mV of  $V_{ref}$ . It is not recommended to drive loads with VREFB, other than setting the hysteresis of the hysteretic comparator, because the current drawn from VREFB sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

## detailed description (continued)

Table 1. Voltage Programming Code

| VID PINS<br>0 = GROUND, 1 = FLOATING, OR PULLUP TO 5 V |      |      |      |      | V <sub>ref</sub><br>(V <sub>dc</sub> ) |
|--------------------------------------------------------|------|------|------|------|----------------------------------------|
| VID4                                                   | VID3 | VID2 | VID1 | VID0 |                                        |
| 1                                                      | 1    | 1    | 1    | 1    | No CPU – Off                           |
| 1                                                      | 1    | 1    | 1    | 0    | 0.925                                  |
| 1                                                      | 1    | 1    | 0    | 1    | 0.950                                  |
| 1                                                      | 1    | 1    | 0    | 0    | 0.975                                  |
| 1                                                      | 1    | 0    | 1    | 1    | 1.000                                  |
| 1                                                      | 1    | 0    | 1    | 0    | 1.025                                  |
| 1                                                      | 1    | 0    | 0    | 1    | 1.050                                  |
| 1                                                      | 1    | 0    | 0    | 0    | 1.075                                  |
| 1                                                      | 0    | 1    | 1    | 1    | 1.100                                  |
| 1                                                      | 0    | 1    | 1    | 0    | 1.125                                  |
| 1                                                      | 0    | 1    | 0    | 1    | 1.150                                  |
| 1                                                      | 0    | 1    | 0    | 0    | 1.175                                  |
| 1                                                      | 0    | 0    | 1    | 1    | 1.200                                  |
| 1                                                      | 0    | 0    | 1    | 0    | 1.225                                  |
| 1                                                      | 0    | 0    | 0    | 1    | 1.250                                  |
| 1                                                      | 0    | 0    | 0    | 0    | 1.275                                  |
| 0                                                      | 1    | 1    | 1    | 1    | No CPU – Off                           |
| 0                                                      | 1    | 1    | 1    | 0    | 1.300                                  |
| 0                                                      | 1    | 1    | 0    | 1    | 1.350                                  |
| 0                                                      | 1    | 1    | 0    | 0    | 1.400                                  |
| 0                                                      | 1    | 0    | 1    | 1    | 1.450                                  |
| 0                                                      | 1    | 0    | 1    | 0    | 1.500                                  |
| 0                                                      | 1    | 0    | 0    | 1    | 1.550                                  |
| 0                                                      | 1    | 0    | 0    | 0    | 1.600                                  |
| 0                                                      | 0    | 1    | 1    | 1    | 1.650                                  |
| 0                                                      | 0    | 1    | 1    | 0    | 1.700                                  |
| 0                                                      | 0    | 1    | 0    | 1    | 1.750                                  |
| 0                                                      | 0    | 1    | 0    | 0    | 1.800                                  |
| 0                                                      | 0    | 0    | 1    | 1    | 1.850                                  |
| 0                                                      | 0    | 0    | 1    | 0    | 1.900                                  |
| 0                                                      | 0    | 0    | 0    | 1    | 1.950                                  |
| 0                                                      | 0    | 0    | 0    | 0    | 2.000                                  |

NOTE: If the VID bits are set to 11111 or 01111, then the high-side and low-side driver outputs will be set low.

## detailed description (continued)

### dynamic VID change

Dynamic VID change controls the rate of change of the programmed VID to allow transitioning within 100  $\mu$ s, while controlling the  $dv/dt$  to avoid large input surge currents. VID could change with any input voltage, output voltage, or output current. A new change is ignored until the current transition is finished. Program the transition by adding a capacitor from DT\_SET to ANAGND.

$$C_{DT\_SET} = \frac{I_{\Delta t} \times \Delta t}{\Delta V_{REF}} = \frac{14 \mu A \times \Delta t}{V_{REF2} - V_{REF1}}$$

### hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by two external resistors and is centered around VREFB. The two external resistors form a resistor divider from VREFB to ANAGND, and the divided down voltage connects to the VHYST terminal. The hysteresis of the comparator will be equal to twice the voltage that is across the VREFB and VHYST pins. The maximum hysteresis setting is 60 mV.

### ramp generator

The ramp generator circuit is partially composed of the PSM circuit. An external resistor from PH to VSENSE\_CORE superimposes a ramp (proportional to  $V_I$  and  $V_O$ ) onto the feedback voltage. This allows increasing the operating frequency, and reduces frequency dependance on the output filter values. A capacitor can be used to provide ac-coupling. Also, connecting a resistor from  $V_I$  to VSENSE\_CORE allows feed forward to counteract any dc offsets due to the ramp generator or propagation delays limiting duty cycle.

### power saving mode/latch

The power saving mode circuit reduces the operating frequency of the ripple regulator during light load. This helps boost the efficiency during light loads by reducing the switching losses. Care should be taken to not allow rms current losses to exceed the switching losses. A 2-bit binary weighted resistor ramp circuit allows setting four operating frequencies.

The PSM/LATCH terminal allows disabling of the fault latch (see Table 2). This allows the user to troubleshoot or implement an external protection circuit.

**Table 2. PSM Program Modes**

|   | Pin Voltage        | Function                            |
|---|--------------------|-------------------------------------|
| 1 | < (ANAGND – 0.3 V) | Disable PSM and disable fault latch |
| 2 | ANAGND to 1.8 V    | Disable PSM and enable fault latch  |
| 3 | 2.3 V to VBIAS     | Enable PSM and enable fault latch   |
| 4 | > (VBIAS + 0.3 V)  | Enable PSM and disable fault latch  |

### active voltage DROOP positioning

The droop compensation network reduces the load transient overshoot/undershoot on  $V_O$ , relative to  $V_{ref}$ .  $V_{O(max)}$  is programmed to a voltage greater than  $V_{ref}$  in the *Application Information* drawing by an external resistor divider from  $V_O$  to the VSENSE\_CORE pin to reduce the undershoot on  $V_{OUT}$  during a low to high load transient. The overshoot during a high-to-low load transient is reduced by subtracting the voltage that is on the DROOP pin from  $V_{ref}$ . The voltage on the IOUT pin is divided down with an external resistor divider, and connected to the DROOP pin. Thus, under loaded conditions,  $V_O$  is regulated to  $V_{O(max)} - V_{(DROOP)}$ . The continuous sensing of the inductor current allows a fast regulating voltage adjustment allowing higher transient repetition rates.

---

## detailed description (continued)

### low-side driver

The low-side driver is designed to drive low  $r_{ds(on)}$  N-channel MOSFETs. The current of the driver is typically 2-A source and 3.3-A sink. The supply to the low-side driver is internally connected to  $V_{CC}$ .

### high-side driver

The high-side driver is designed to drive low  $r_{ds(on)}$  N-channel MOSFETs. The current of the driver is typically 2-A source and 3.3-A sink. The high-side driver is configured as a floating bootstrap driver. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky diode for improved drive efficiency. The maximum voltage that can be applied between the BOOT pin and ground is 35 V.

### deadtime control

The deadtime control prevents shoot-through current from flowing through the main power FET's during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is below 1.7 V. The low-side driver is not allowed to turn on until the gate drive voltage from the high-side FET to PH is below 1.3 V.

### current sensing

Current sensing is achieved by sensing the voltage across a current-sense resistor placed in series between the output inductor and the output capacitors. The sensing network consists of a high bandwidth differential amplifier with a gain of 25x to allow using sense resistors with values as low as 1 m $\Omega$ . Sensing occurs at all times to allow having *real-time* information for quick response during an active voltage droop positioning transition. The voltage on the IOUT pin equals 25 times the sensed voltage.

### VR\_ON

The VR\_ON terminal is a TTL compatible digital pin that is used to enable the controller. When VR\_ON is low, the output drivers are low, the linear regulator drivers are off, and the slowstart capacitor is discharged. When VR\_ON goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system logic supply is connected to the VR\_ON pin, the VR\_ON pin can control power sequencing by locking out controller operation until the system logic supply exceeds the input threshold voltage of the VR\_ON circuit. Thus,  $V_{CC}$  and the system logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. Likewise, a microprocessor or other external logic can also control the sequencing through VR\_ON.

### VBIAS undervoltage lockout

The VBIAS undervoltage-lockout circuit disables the controller, while VBIAS is below the 4.46-V start threshold during power up. The controller is disabled when VBIAS goes below 3.3 V. While the controller is disabled, the output drivers will be low and the slowstart capacitor will be shorted. When VBIAS exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins.

### IO linear regulator driver

The IO linear regulator driver circuit drives a high power NPN external power transistor, allowing external power dissipation. The IO voltage is ramped up with the slowstart with the other two converters. Under voltage protection protects against hard shorts or extreme loading. The VSENSE\_IO voltage is monitored by the VGATE (powergood) circuit. A fault or shutdown on any converter will shut down the linear regulator.

### CLK linear regulator driver

The CLK linear regulator driver circuit drives a lower power NPN external power transistor, allowing external power dissipation. The CLK voltage is ramped up with the slowstart with the other two converters. Under voltage protection protects against hard shorts or extreme loading. The VSENSE\_CLK voltage is monitored by the VGATE (powergood) circuit. A fault or shutdown on any converter will shut down the linear regulator.

**detailed description (continued)****slowstart**

The slowstart circuit controls the rate at which  $V_{OUT}$  powers up. A capacitor is connected between the SLOWST and ANAGND pins and is charged by an internal current source. The value of the current source is proportional to the reference voltage, so that the charging rate of  $C_{(SLOWST)}$  is proportional to the reference voltage. By making the charging current proportional to  $V_{ref}$ , the power up time for  $V_O$  will be independent of  $V_{ref}$ . Thus,  $C_{(SLOWST)}$  can remain the same value for all VP settings. The slowstart charging current is determined by the following equation:

$$I_{SLOWSTART} = \frac{I(VREFB)}{5} \quad (\text{amps})$$

where,  $I(VREFB)$  is the current flowing out of the VREFB terminal. It is recommended that no additional loads be connected to VREFB, other than the resistor divider for setting the hysteresis voltage. Thus, these resistor values will determine the slowstart charging current. The maximum current that can be sourced by the VREFB circuit is 500  $\mu\text{A}$ . The equation for setting the slowstart time is:

$$t_{SLOWSTART} = 5 \times C_{(SLOWSTART)} \times R(VREFB) \quad (\text{seconds})$$

where,  $R(VREFB)$  is the total external resistance from VREFB to ANAGND.

**VGATE**

The VGATE circuit monitors for an undervoltage condition on  $V_O(VSENSE\_CORE)$ ,  $V_O(VSENSE\_IO)$ , and  $V_O(VSENSE\_CLK)$ . If any  $V_O$  is 7% below its reference voltage, or if any  $UVLO(V_{CC}, VR\_ON)$  threshold is not reached, then the VGATE pin is pulled low. The VGATE terminal is an open drain output.

**overvoltage protection**

The overvoltage protection circuit monitors  $V_O(VSENSE\_CORE)$ ,  $V_O(VSENSE\_IO)$ , and  $V_O(VSENSE\_CLK)$  for an overvoltage condition. If any  $V_O$  is 15% above its reference voltage, then a fault latch is set, then both the ripple regulator output drivers and the linear regulator drivers are turned off. The latch will remain set until VBIAS goes below the undervoltage lockout value or until  $VR\_ON$  is pulled low.

**overcurrent protection**

The overcurrent protection circuit monitors the current through the current sense resistor. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND terminals, with the divider voltage connected to the OCP terminal. If the voltage on the OCP terminal exceeds 200 mV, then a fault latch is set and the output drivers (ripple regulator and linear regulators) are turned off. The latch remains set until VBIAS goes below the undervoltage lockout value or until  $VR\_ON$  is pulled low.

**thermal shutdown**

Thermal shutdown disables the controller if the junction temperature exceeds the 165°C thermal shutdown trip point. The hysteresis is 10°C.

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## APPLICATION INFORMATION

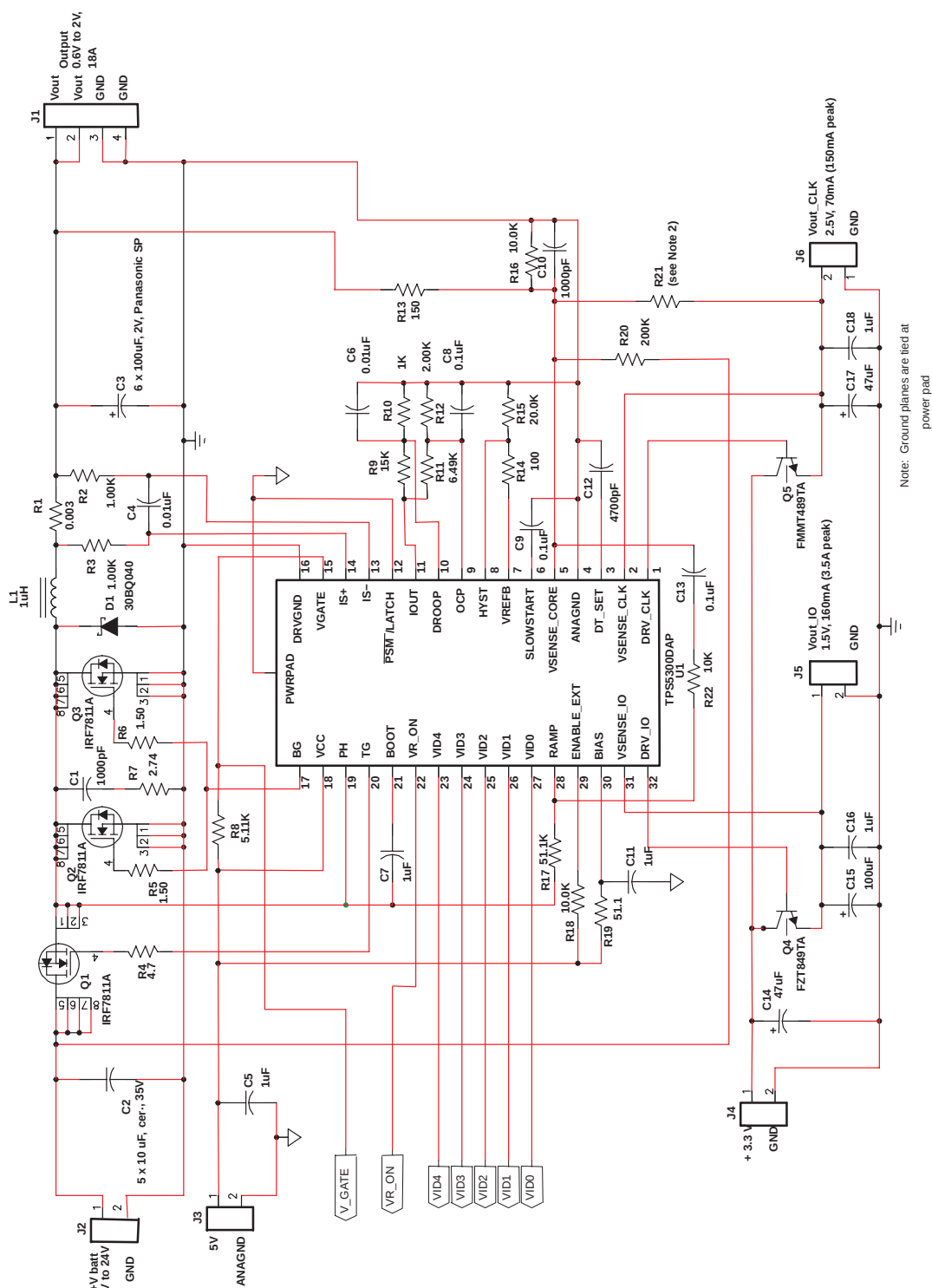
Figure 1 is a standard application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage that includes the power FETs (Q1–Q3), input capacitor (C2), output filter (L1 and C3), and the current sense resistor (R1) must be tailored to the input/output requirements of the application. The design documentation and test results for different mobile CPU power supplies covering core current from 13 A and up to 40 A is available from the factory upon request or can be found in applications notes. The control circuit is basically the same for all applications with minor tweaking of specific values.

The main waveforms are shown in Figure 2 through Figure 5. These waveforms include the following:

- The output ripple and  $V_{ds}$  voltage of the low-side FET in the whole input voltage range (see Figure 2).
- The dynamic output voltage change between the performance and battery modes of operation (see Figure 3).
- The transient response characteristics on the load current step up and down transitions (see Figure 4).
- The typical start-up waveforms for core, clock and I/O voltages (see Figure 5).

The waveforms confirm the excellent dynamic characteristics of the hysteretic controller. The modification, that includes an additional ramp signal superimposed to the input  $V_{SENSE\_CORE}$  internally and externally by circuits R17, R22, C13, and C10 makes the switching frequency independent of the output filter characteristics. It also decreases the comparator delay times by increasing efficiency overdrive. This approach is shown in Figure 6.

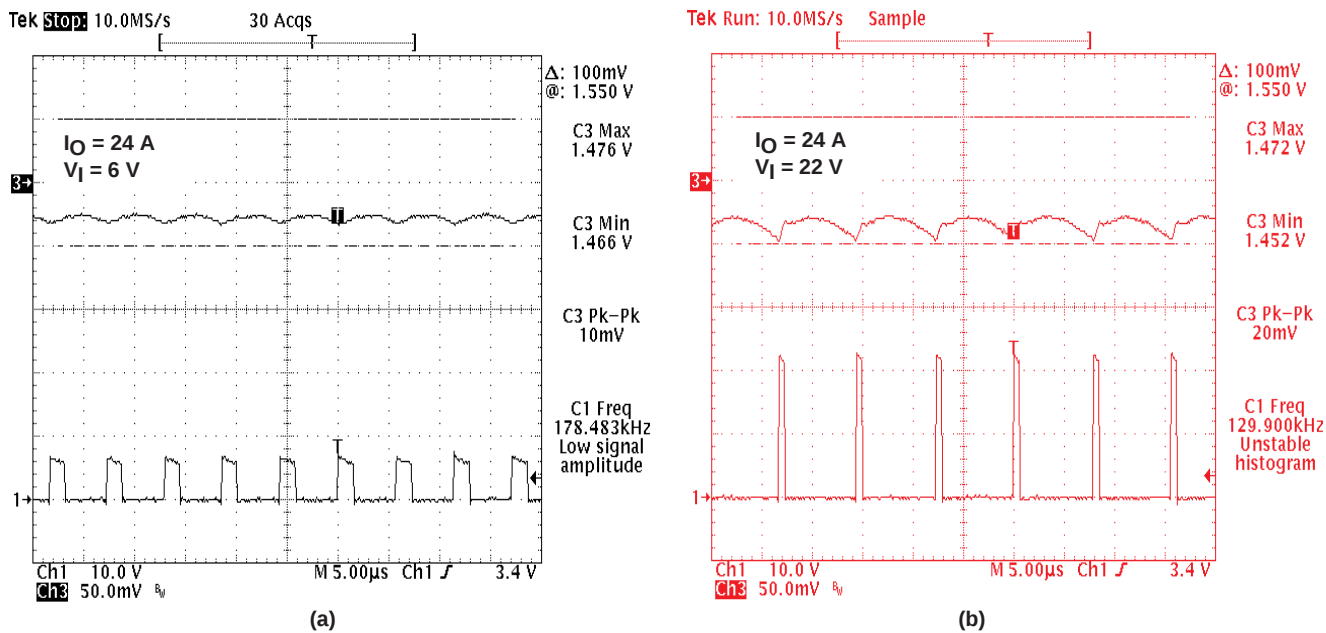
## APPLICATION INFORMATION



- NOTES: A. Contact factory or see application notes for documentation and test results of different mobile core regulator applications at the output current up to 40 A.
- B. R21 allows VID code voltage adjustment.

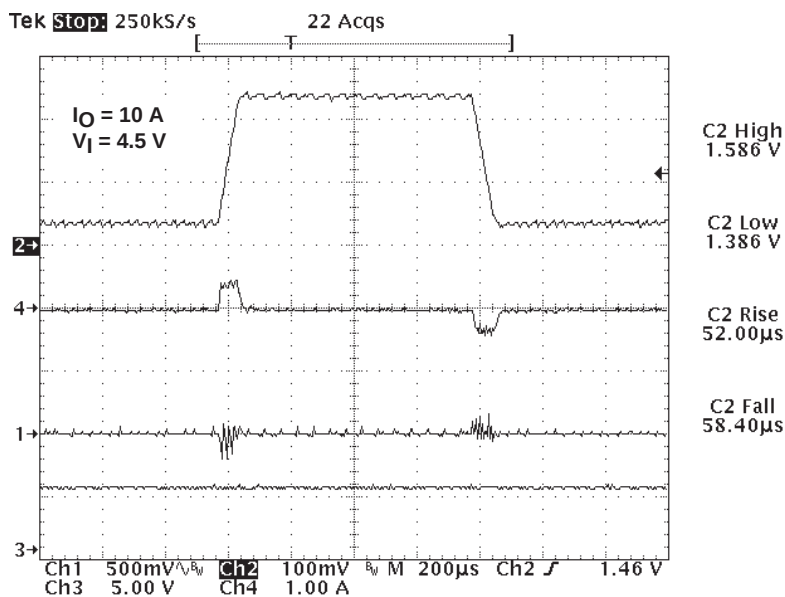
Figure 1. Standard Application Circuit

## APPLICATION INFORMATION



NOTE: Channel 1 = drain source voltage (10 V/div), Channel 2 = output voltage ripple (50 nV/div)

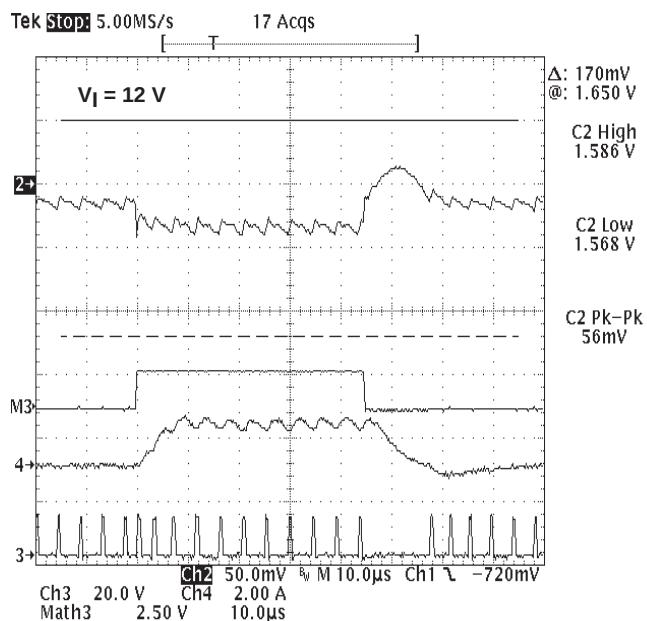
Figure 2. Output Voltage Ripple and Low-Side FET Drain-Source Voltage



NOTE: Channel 1 = input voltage ripple, Channel 2 = output voltage, Channel 3 = VGATE signal, Channel 4 = input current.

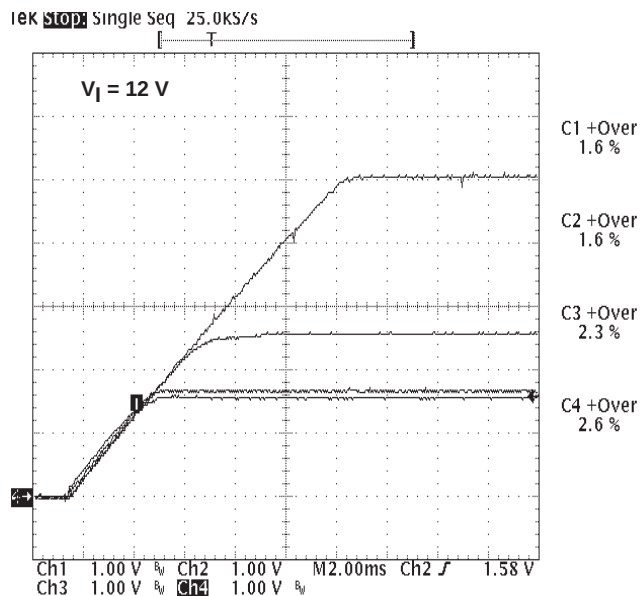
Figure 3. Dynamic VID-Code Change Waveforms From 1.35 V to 1.6 V and Back

## APPLICATION INFORMATION



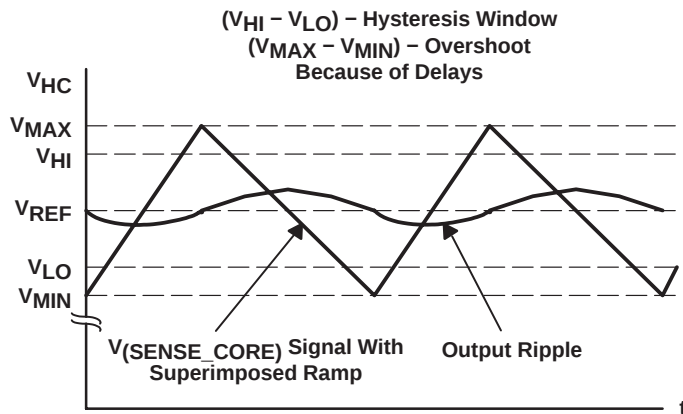
NOTE: The load current (M3) has 10-A step with a slew rate of 30 A/μs. Channel 3 = drain source of low-side FET, and channel 4 = input current.

**Figure 4. Output Voltage Transient Response (Channel 2)**



NOTE: From bottom to top:  $V_{OUT\ IO}$ ,  $V_{OUT\ core}$ ,  $V_{OUT\ CLK}$ , and the voltage of the slow-start capacitor.

**Figure 5. Start-Up Waveforms at 12 V Input Voltage and 10-A Load Current on the Switching Regulator**



**Figure 6. Hysteretic Comparator Input Waveforms**

## APPLICATION INFORMATION

## switching cycle and frequency calculation

The switching cycle calculation is shown below.

$$T_s = \frac{V_I \times C_{add} \times Hyst \times R_{add}}{V_O \times (V_I - V_O)} + T_{del1} \times \frac{V_I}{V_O} + T_{del2} \times \frac{V_I}{V_I - V_O}$$

where,  $V_I$  = input voltage,  $V_O$  = output voltage,  $C_{add}$  = C10 and  $R_{add}$  = R22 + R17 in Figure 1, Hyst is the hysteresis window,  $T_{del1}$  and  $T_{del2}$  are the comparator and drive circuit delays when the high-side and low-side FETs turn on correspondingly. The switching frequency variation for the different input and output voltages is shown in Figure 7. In this case the parameters of equation above are the following:  $R_{add}$  = 49.9 k $\Omega$ ,  $C_{add}$  = 1060 pF,  $T_{del1}$  = 240 ns,  $T_{del2}$  = 250 ns, Hyst = 0.5% of  $V_O$ . The lower-switching frequency at higher input voltages helps to keep low switching losses during the input voltage range.

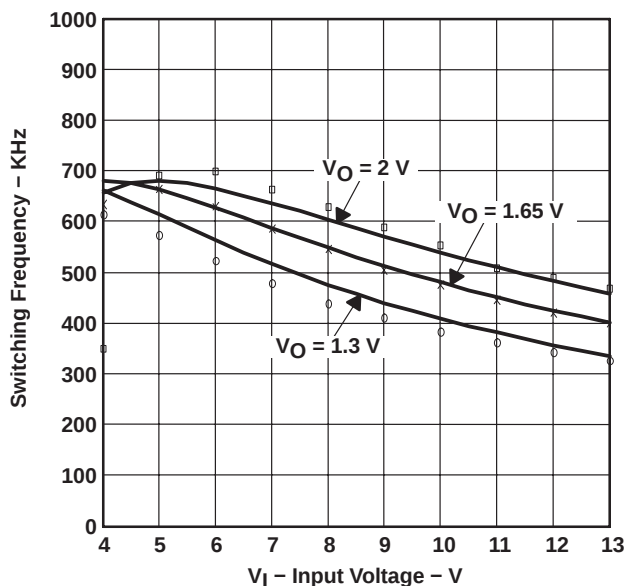


Figure 7. Theoretical (Solid) and Measured (Points) Switching Frequency

## output voltage

The output voltage with a dc decoupling capacitor (C13) is defined below:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where,  $R1$  = R13 and  $R2$  = R16 (see Figure 1)

## additional literature

*An Analytical Comparison of Alternative Control Techniques for Powering Next-Generation Microprocessors*, SEM-1400 TI/Unitrode Power Supply Design Seminar, Topic 1.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TPS5300DAP       | ACTIVE                | HTSSOP       | DAP             | 32   | 46          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-3-260C-168 HR          |                             |
| TPS5300DAPG4     | ACTIVE                | HTSSOP       | DAP             | 32   | 46          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-3-260C-168 HR          |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

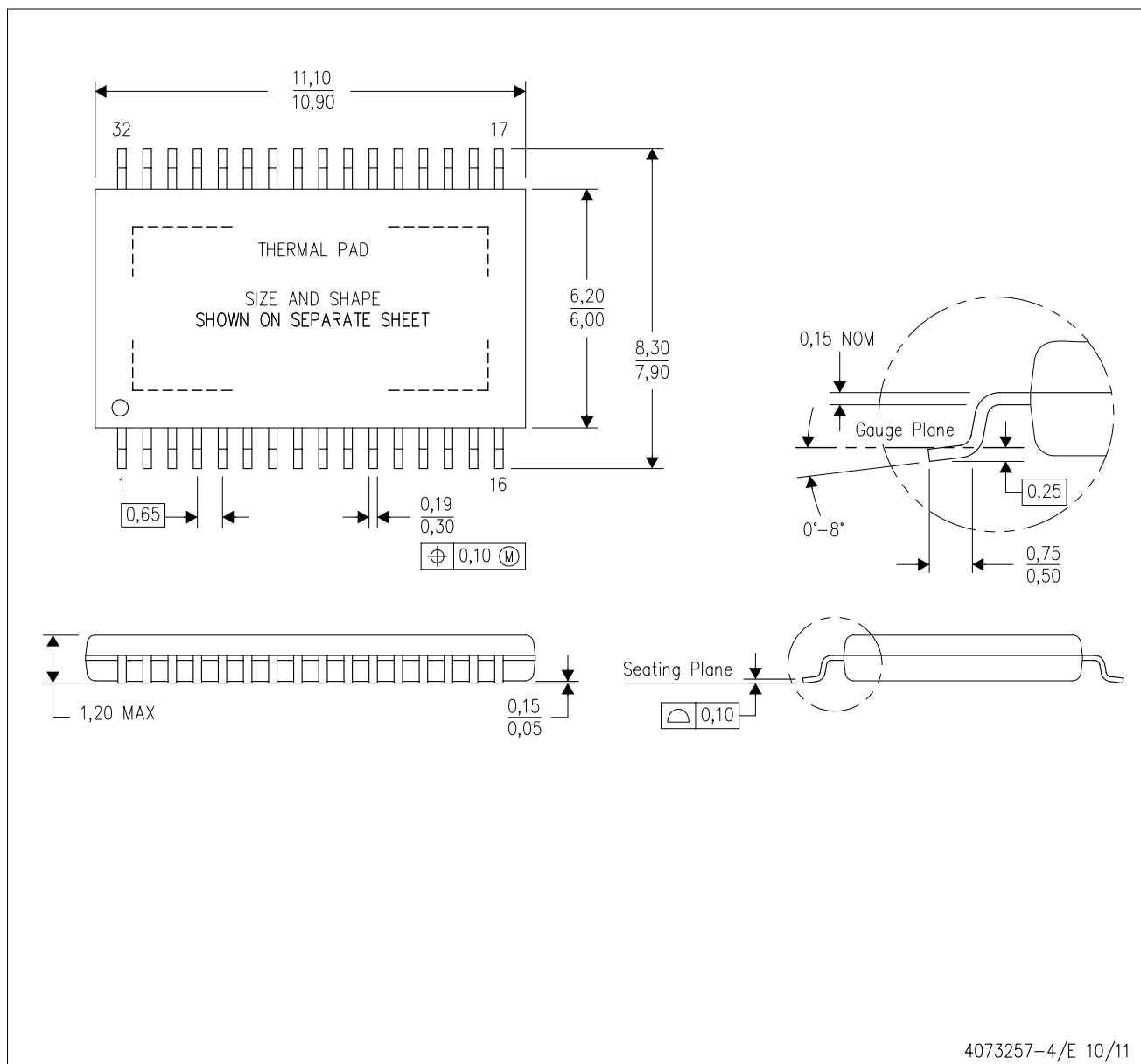
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
-  Falls within JEDEC MO-153 Variation DCT.

DAP (R-PDSO-G32)

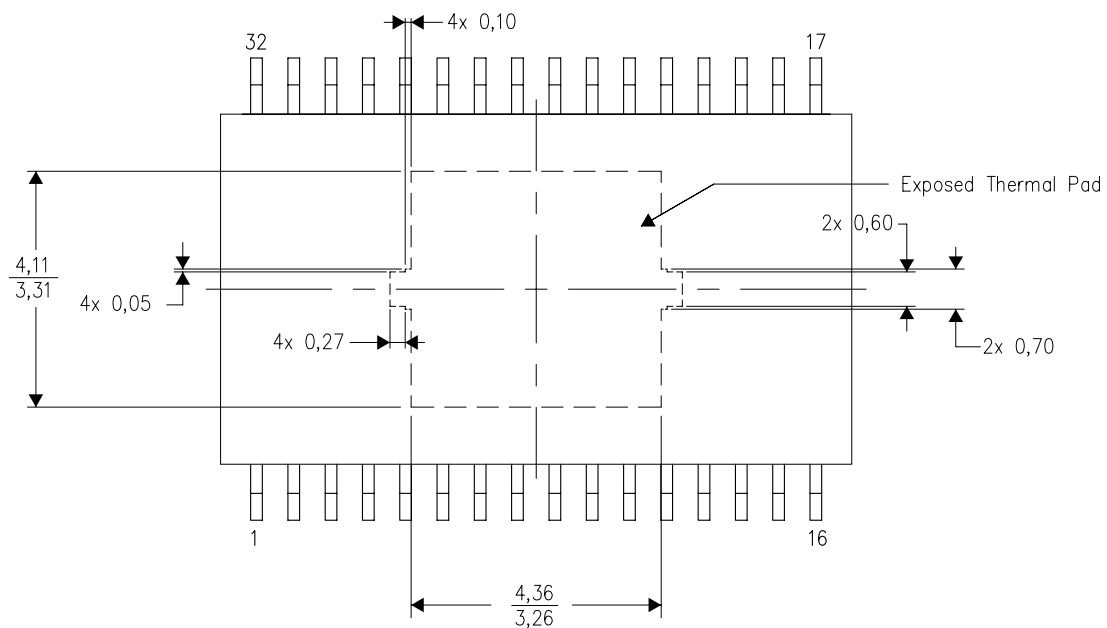
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

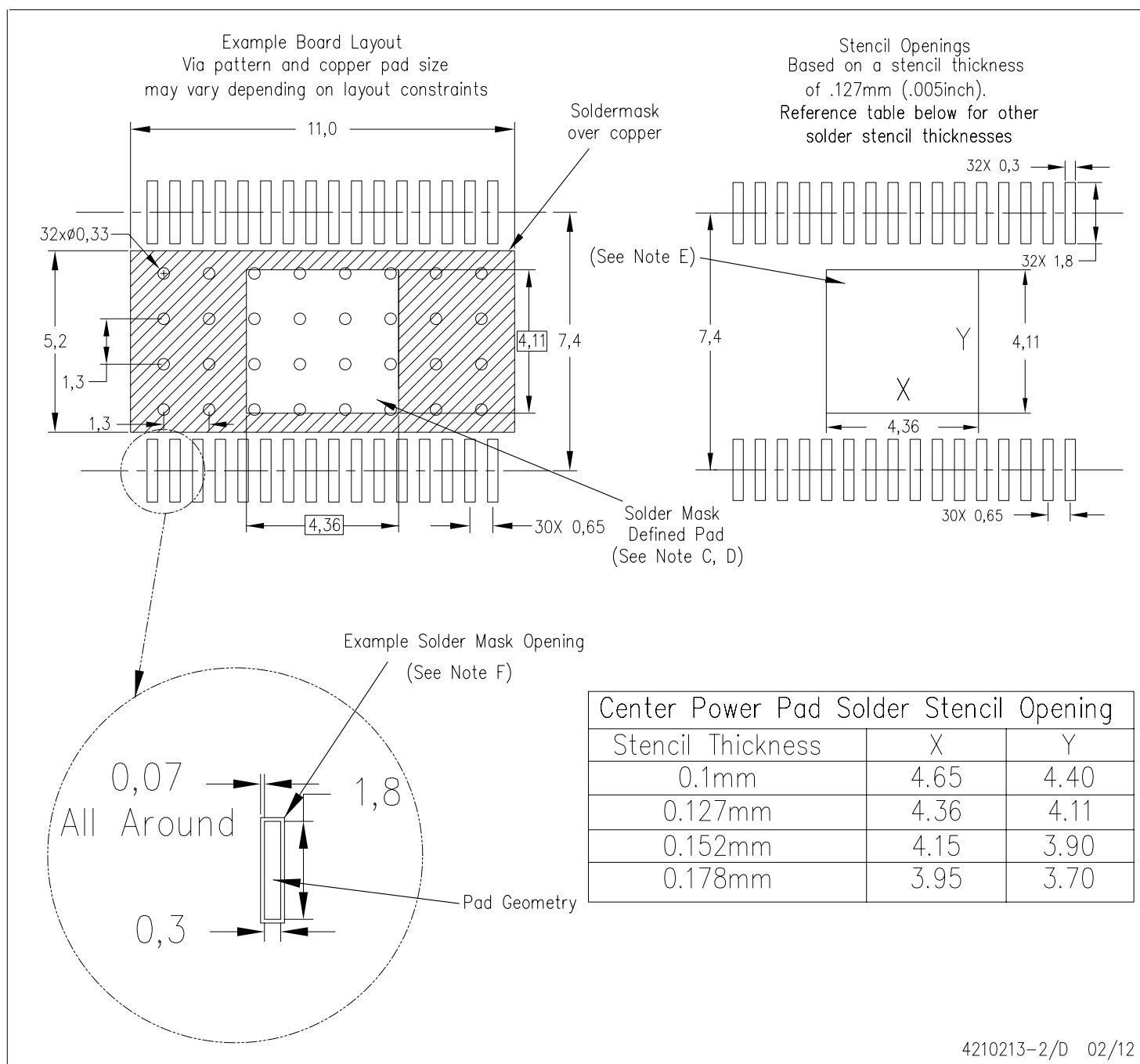


4206319-3/J 02/12

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

## DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Contact the board fabrication site for recommended soldermask tolerances.

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