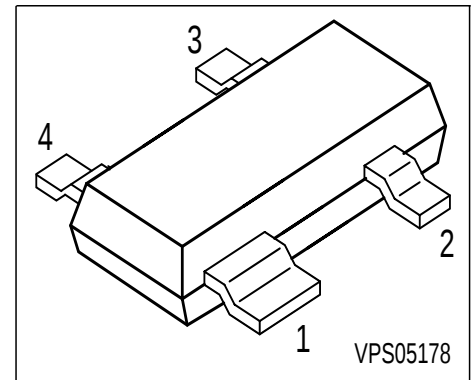
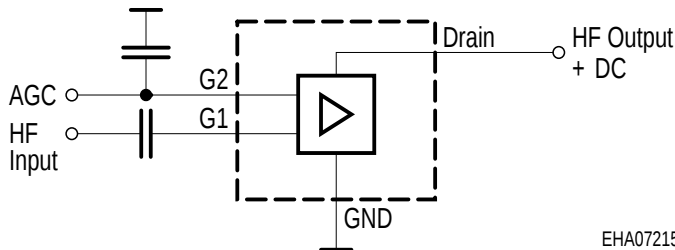


Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stages up to 1GHz
- Operating voltage 5V
- Integrated stabilized bias network



ESD: Electrostatic discharge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration				Package
BF1005	MZs	1 = S	2 = D	3 = G2	4 = G1	SOT143

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation, $T_S \leq 76^\circ\text{C}$	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	$^\circ\text{C}$
Channel temperature	T_{ch}	150	

Thermal Resistance

Channel - soldering point ¹⁾	R_{thchs}	≤ 370	K/W
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¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Note:

It is not recommended to apply external DC-voltage on Gate 1 in active mode.

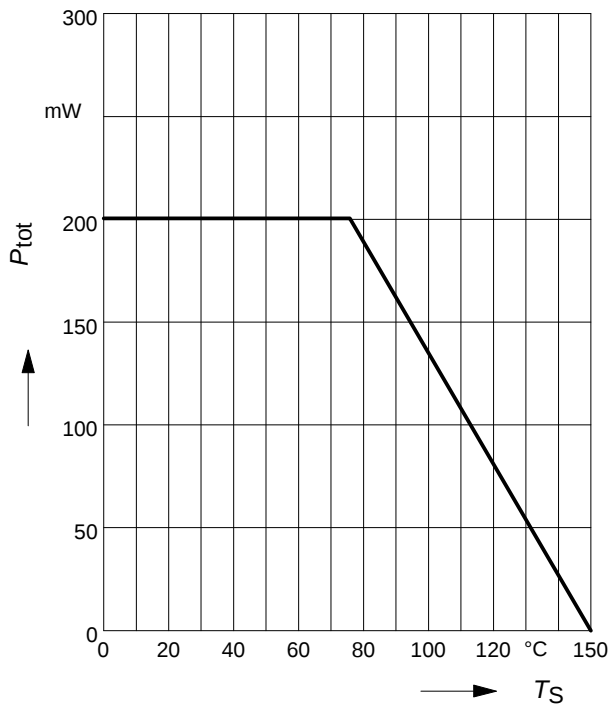
Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage $I_D = 650\ \mu\text{A}$, $V_{G1S} = 0\ \text{V}$, $V_{G2S} = 0\ \text{V}$	$V_{(\text{BR})\text{DS}}$	12	-	-	V
Gate 1 - source breakdown voltage $+I_{G1S} = 10\ \text{mA}$, $V_{G2S} = 0\ \text{V}$, $V_{\text{DS}} = 0\ \text{V}$	$+V_{(\text{BR})\text{G1SS}}$	8	-	12	
Gate 2 source breakdown voltage $\pm I_{G2S} = 10\ \text{mA}$, $V_{G1S} = 0\ \text{V}$, $V_{\text{DS}} = 0\ \text{V}$	$\pm V_{(\text{BR})\text{G2SS}}$	8	-	13	
Gate 1 source current $V_{G1S} = 6\ \text{V}$, $V_{G2S} = 0\ \text{V}$	$+I_{G1SS}$	-	100	-	μA
Gate 2 source leakage current $\pm V_{G2S} = 8\ \text{V}$, $V_{G1S} = 0\ \text{V}$, $V_{\text{DS}} = 0\ \text{V}$	$\pm I_{G2SS}$	-	-	50	nA
Drain current $V_{\text{DS}} = 5\ \text{V}$, $V_{G1S} = 0$, $V_{G2S} = 4.5\ \text{V}$	I_{DSS}	-	-	1.5	mA
Operating current (selfbiased) $V_{\text{DS}} = 5\ \text{V}$, $V_{G2S} = 4.5\ \text{V}$	I_{DSO}	8	10	-	
Gate 2-source pinch-off voltage $V_{\text{DS}} = 5\ \text{V}$, $I_D = 100\ \mu\text{A}$	$V_{\text{G2S(p)}}$	-	1	-	V

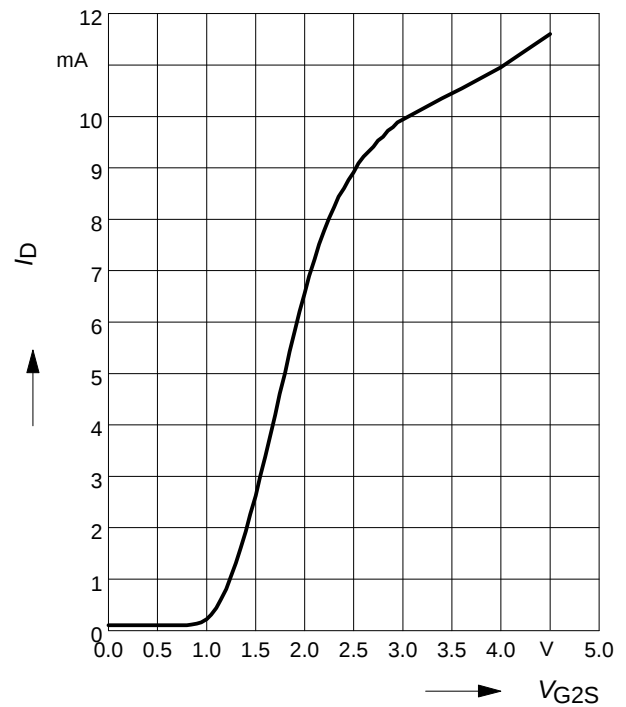
AC characteristics

Forward transconductance (self biased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4.5\ \text{V}$	g_{fs}	-	24	-	mS
Gate 1-input capacitance (self biased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $f = 1\ \text{MHz}$	C_{g1ss}	-	2.1	2.5	pF
Output capacitance (self biased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $f = 100\ \text{MHz}$	C_{dss}	-	1.3	-	
Power gain (self biased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $f = 800\ \text{MHz}$	G_{ps}	-	19	-	dB
Noise figure (self biased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $f = 800\ \text{MHz}$	F_{800}	-	1.4	-	
Gain control range (self biased) $V_{DS} = 5\ \text{V}$, $V_{G2S} = 4 \dots 0$, $f = 800\ \text{MHz}$	ΔG_{ps}	40	50	-	

Total power dissipation $P_{\text{tot}} = f(T_S)$

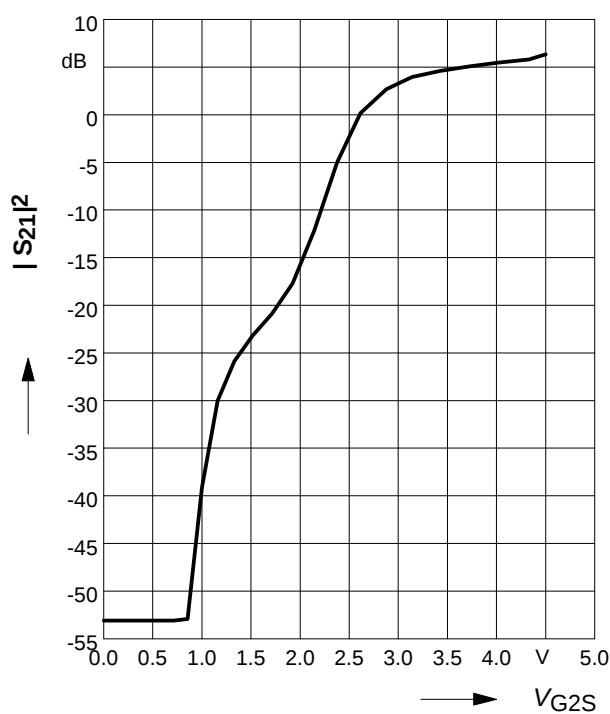


Drain current $I_D = f(V_{G2S})$



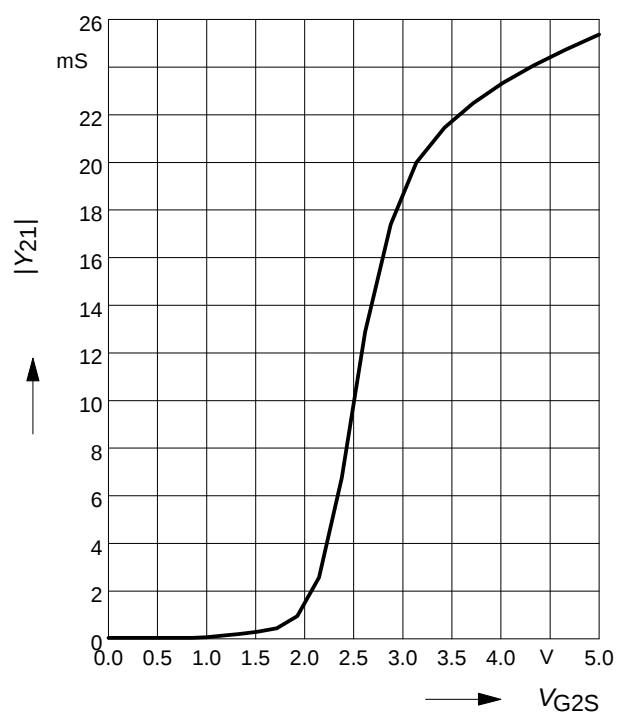
Insertion power gain

$|S_{21}|^2 = f(V_{G2S})$

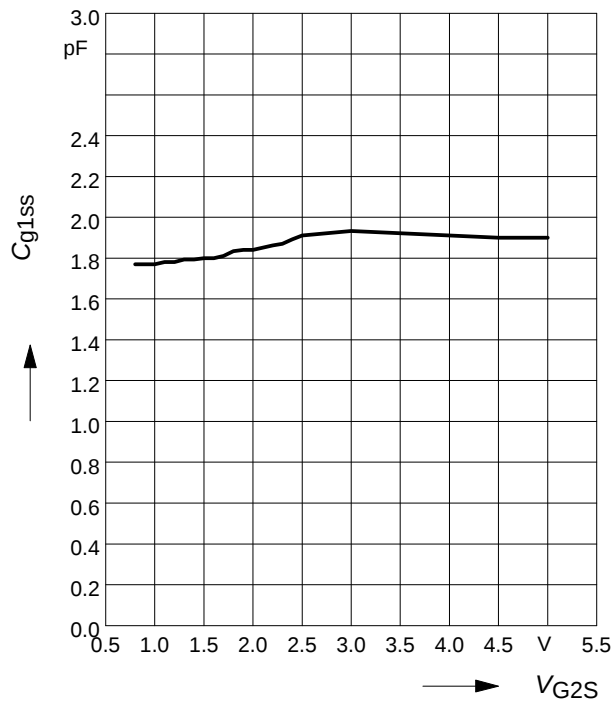


Forward transfer admittance

$|Y_{21}| = f(V_{G2S})$



Gate 1 input capacitance $C_{g1ss} = f(V_{G2S})$
 $f = 200\text{MHz}$



Output capacitance $C_{dss} = f(V_{G2S})$
 $f = 200\text{MHz}$

