

2N4351

N-CHANNEL MOSFET ENHANCEMENT MODE

FEATURES

DIRECT REPLACEMENT FOR INTERSIL 2N4351

HIGH DRAIN CURRENT $I_D = 100\text{mA}$

HIGH GAIN $g_{fs} = 1000\mu\text{S}$

ABSOLUTE MAXIMUM RATINGS¹

@ 25 °C (unless otherwise stated)

Maximum Temperatures

Storage Temperature -65 to +200 °C

Operating Junction Temperature -55 to +150 °C

Maximum Power Dissipation

Continuous Power Dissipation 375mW

Maximum Current

Drain to Source 100mA

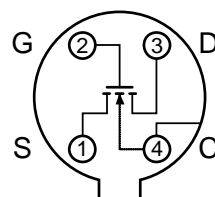
Maximum Voltages

Drain to Body 25V

Drain to Source 25V

Peak Gate to Source² $\pm 125\text{V}$

TO-72
BOTTOM VIEW



* Body tied to Case.

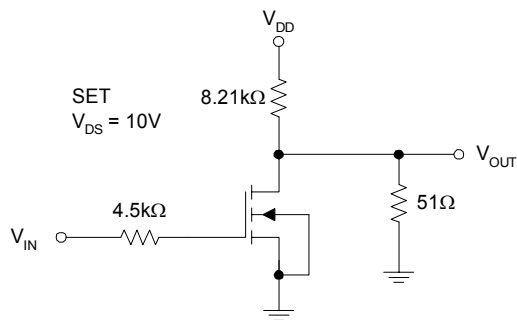
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated) ($V_{SB} = 0\text{V}$ unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	25			V	$I_D = 10\mu\text{A}$, $V_{GS} = 0\text{V}$
$V_{DS(on)}$	Drain to Source "On" Voltage			1		$I_D = 2\text{mA}$, $V_{GS} = 10\text{V}$
$V_{GS(th)}$	Gate to Source Threshold Voltage	1		5		$V_{DS} = 10\text{V}$, $I_D = 10\mu\text{A}$
I_{GSS}	Gate Leakage Current			10	pA	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$
I_{DSS}	Drain Leakage Current "Off"			10	nA	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$
$I_{D(on)}$	Drain Current "On"	3			mA	$V_{GS} = 10\text{V}$, $V_{DS} = 10\text{V}$
g_{fs}	Forward Transconductance	1000			μS	$V_{DS} = 10\text{V}$, $I_D = 2\text{mA}$, $f = 1\text{MHz}$
$r_{DS(on)}$	Drain to Source "On" Resistance			300	Ω	$V_{GS} = 10\text{V}$, $I_D = 0\text{A}$, $f = 1\text{kHz}$
C_{rss}	Reverse Transfer Capacitance			1.3	pF	$V_{DS} = 0\text{V}$, $V_{GS} = 0\text{V}$, $f = 140\text{kHz}$
C_{iss}	Input Capacitance			5.0		$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$, $f = 140\text{kHz}$
C_{db}	Drain to Body Capacitance			5.0		$V_{DB} = 10\text{V}$, $f = 140\text{kHz}$

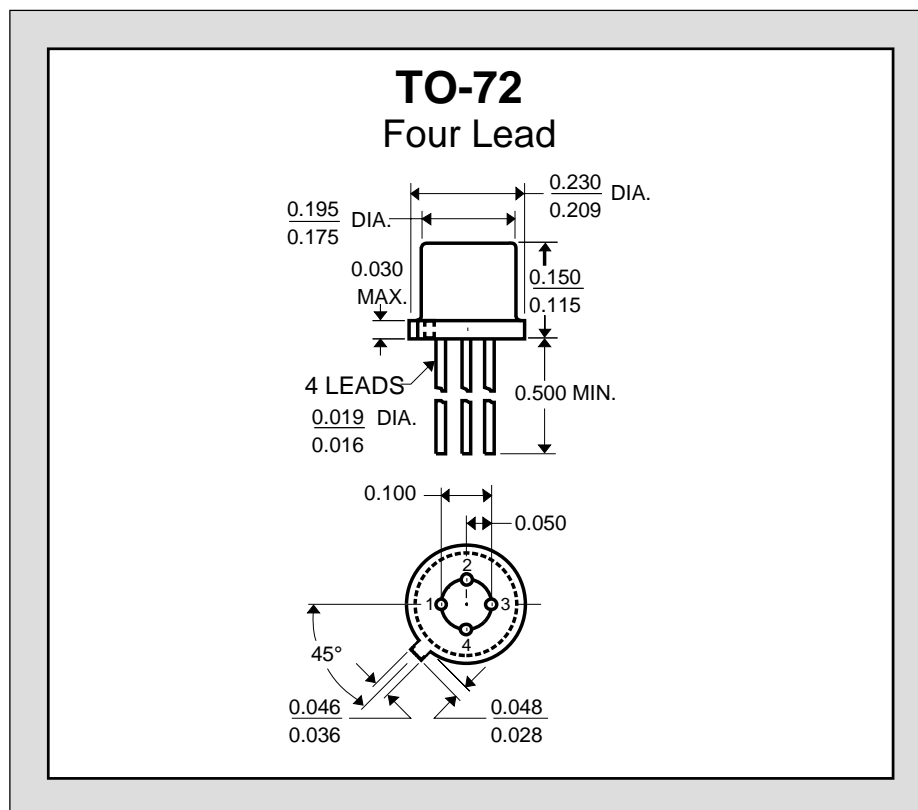
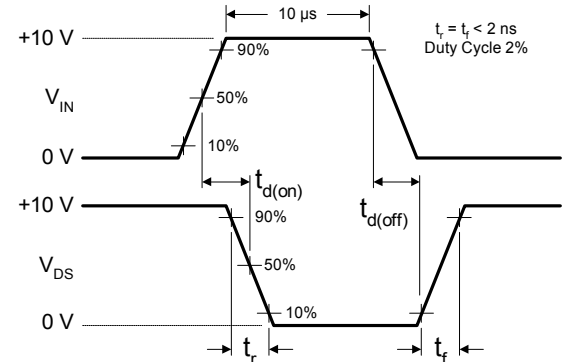
SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MAX	UNITS
$t_{d(on)}$	Turn On Delay Time	45	ns
t_r	Turn On Rise Time	65	
$t_{d(off)}$	Turn Off Delay Time	60	
t_f	Turn Off Fall Time	100	

SWITCHING TEST CIRCUIT



TIMING WAVEFORMS



1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Device must not be tested at $\pm 125V$ more than once or longer than 300ms.

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