14-BIT, 190 MSPS ADC WITH DDR LVDS/CMOS OUTPUTS

FEATURES

- **Maximum Sample Rate: 190 MSPS**
- **14-Bit Resolution**
- **No Missing Codes**
- **Total Power Dissipation 1.1 W**
- **Internal Sample and Hold**
- **73.2-dBFS SNR at 70-MHz IF**
- **84-dBc SFDR at 70-MHz IF**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Internal/External Reference Support**
- **Clock Duty Cycle Stabilizer**
- **Power Saving Modes at Lower Sample Rates**
- **3.3-V Analog and Digital Supply**
- **48-QFN Package (7 mm × 7 mm)**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**
- **Radar Systems**

DESCRIPTION

The ADS5546 is a high performance 14-bit 190 MSPS A/D converter. It offers state of the art functionality and performance while applying advanced techniques to minimize board space. Using an internal sample and hold and low jitter clock buffer, the ADC supports high SNR and high SFDR at high input frequencies. In a compact 48-pin QFN, the device offers unprecedented digital output flexibility with fully differential DDR (Double Data Rate) LVDS or parallel CMOS options. The ADS5546 also includes an internal reference, but the traditional reference pins have been eliminated, along with the need for external decoupling. Alternatively, the device can also be driven with an external reference. For applications where power is important, the ADS5546 offers innovative solutions, such as power down modes and the possibility of power scaling at lower sample rates. The device is specified over the -40°C to +85°C operating range.

PRODUCT PREVIEW

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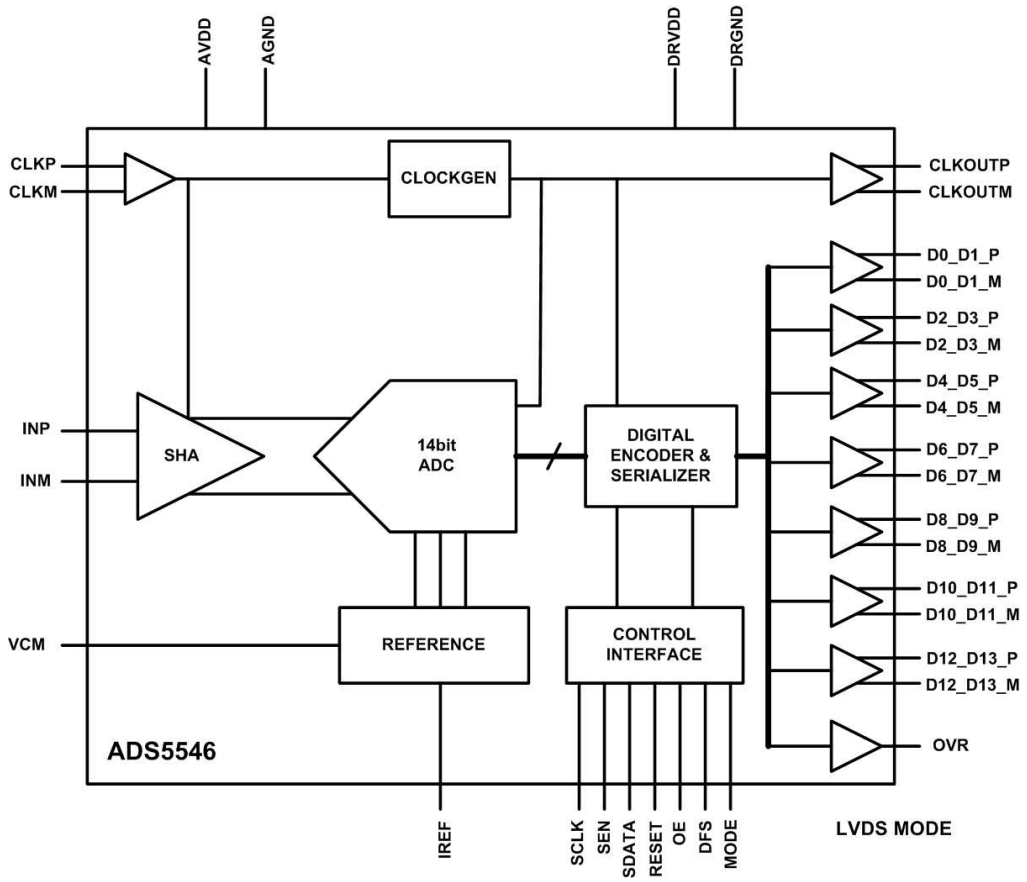

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5546	QFN-48	RGZ	–40°C to 85°C	ADS5546IRGZ	ADS5546IRGZ	

(1) θ_{JA} = TBD, θ_{JC} = TBD

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
AVDD	Supply voltage range	–0.3 V to 3.9	V
DRVDD	Supply voltage range	–0.3 V to 3.9	V
	Voltage between AGND and DRGND	-0.3 to 0.3	V
	Voltage between AVDD to DRVDD	-0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)	-0.3 to 1.8	V
	Voltage applied to analog input pins	–0.3 V to minimum (3.6, AVDD + 0.3 V)	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{STG}	Storage temperature range	–65 to 150	°C
	Lead temperature 1,6 mm (1/16") from the case for 10 seconds	220	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
SUPPLIES AND REFERENCES					
AVDD	Analog supply voltage	3	3.3	3.6	V
DRVDD	Digital supply voltage	3	3.3	3.6	V
ANALOG INPUTS					
	Differential input voltage range		2		Vpp
	Input common-mode voltage		1.5 ±0.1		V
	Voltage applied on VCM in external reference mode		1.5 ±0.05		V
CLOCK INPUT					
	Input clock sample rate	1		190	MSPS
	Input clock amplitude, differential	TBD	1.5		Vpp
	Input clock duty cycle		50%		
DIGITAL OUTPUTS					
C_L	Maximum external load capacitance from each output pin to DRGND (LVDS and CMOS modes)		5		pF
R_L	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
	Operating free-air temperature	–40		85	°C

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ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 190 MSPS, sine wave input clock, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				14		bits
ANALOG INPUT						
	Differential input voltage range			2		Vpp
	Differential input capacitance			7		pF
	Analog input bandwidth	–3 dB, source impedance 50 Ω		500		MHz
	Analog input common mode current (per input pin)			310		µA
REFERENCE VOLTAGES						
VREFB	Internal reference bottom voltage	Internal reference mode		0.5		V
VREFT	Internal reference top voltage	Internal reference mode		2.5		V
VCM	Common mode output voltage	Internal reference mode		1.5		V
	VCM output current capability	Internal reference mode		±4		mA
DC ACCURACY						
	No Missing Codes			Assured		
DNL	Differential non-linearity			0.5		LSB
INL	Integral non-linearity			± 3		LSB
	Offset error			±10		mV
	Offset temperature coefficient			TBD		ppm/°C
	Gain error			±1		%FS
	Gain temperature coefficient			TBD		Δ%/°C
DC PSRR	DC Power supply rejection ratio			TBD		mV/V
POWER SUPPLY						
IAVDD	Analog supply current			291		mA
IDRVDD	Digital supply current	LVDS mode, I_O = 3.5 mA, R_L = 100 Ω, C_L = 5 pF		51		mA
		CMOS mode, F_{IN} = 2.5 MHz, C_L = 5 pF		43		mA
I_{CC}	Total supply current	LVDS mode		342		mA
	Total power dissipation	LVDS mode		1.13		W
	Standby power	In STANDBY mode, clock running		100		mW

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ELECTRICAL CHARACTERISTICS (Continued)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 190 MSPS, sine wave input clock, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS						
SNR	Signal to noise ratio	F_{IN} = 10 MHz		73.8		dBFS
		F_{IN} = 40 MHz		73.6		
		F_{IN} = 70 MHz		73.2		
		F_{IN} = 100 MHz		72.8		
		F_{IN} = 150 MHz		71.9		
		F_{IN} = 225 MHz		70.3		
		F_{IN} = 300 MHz		68.9		
	RMS output noise	Inputs tied to common-mode		1.1		LSB
SFDR	Spurious free dynamic range	F_{IN} = 10 MHz		85		dBc
		F_{IN} = 40 MHz		85		
		F_{IN} = 70 MHz		84		
		F_{IN} = 100 MHz		79		
		F_{IN} = 150 MHz		80		
		F_{IN} = 225 MHz		77		
		F_{IN} = 300 MHz		72		
SINAD	Signal to noise and distortion ratio	F_{IN} = 10 MHz		73.1		dBFS
		F_{IN} = 40 MHz		72.9		
		F_{IN} = 70 MHz		72.5		
		F_{IN} = 100 MHz		71.1		
		F_{IN} = 150 MHz		70.8		
		F_{IN} = 225 MHz		68.8		
		F_{IN} = 300 MHz		67.4		
HD2	Second harmonic	F_{IN} = 10 MHz		89		dBc
		F_{IN} = 40 MHz		91		
		F_{IN} = 70 MHz		86		
		F_{IN} = 100 MHz		84		
		F_{IN} = 150 MHz		80		
		F_{IN} = 225 MHz		84		
		F_{IN} = 300 MHz		74		

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ELECTRICAL CHARACTERISTICS (Continued)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 190 MSPS, sine wave input clock, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	Third harmonic	F_{IN} = 10 MHz		87		dBc
		F_{IN} = 40 MHz		87		
		F_{IN} = 70 MHz		84		
		F_{IN} = 100 MHz		79		
		F_{IN} = 150 MHz		85		
		F_{IN} = 225 MHz		77		
		F_{IN} = 300 MHz		72		
	Worst harmonic (other than HD2, HD3)	F_{IN} = 10 MHz		93		dBc
		F_{IN} = 40 MHz		92		
		F_{IN} = 70 MHz		91		
		F_{IN} = 100 MHz		90		
		F_{IN} = 150 MHz		89		
		F_{IN} = 225 MHz		90		
		F_{IN} = 300 MHz		89		
THD	Total harmonic distortion	F_{IN} = 10 MHz		81.5		dBc
		F_{IN} = 40 MHz		82		
		F_{IN} = 70 MHz		81.8		
		F_{IN} = 100 MHz		77		
		F_{IN} = 150 MHz		78.5		
		F_{IN} = 225 MHz		76		
		F_{IN} = 300 MHz		71		
ENOB	Effective number of bits	F_{IN} = 10 MHz		11.8		bits
IMD	Two-tone intermodulation distortion			TBD		dBFS
				TBD		
AC PSRR	AC power supply rejection ratio			TBD		dB
	Voltage overload recovery time	Recovery to 1% for 6-dB overload		1		clock cycles

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DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = DRVDD = 3.3 V, I_O = 3.5 mA, R_L = 100 Ω(1)(2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µA
Low-level input current			–33		µA
Input capacitance			4		pF
DIGITAL OUTPUTS – CMOS MODE					
High-level output voltage			3.3		V
Low-level output voltage			0		V
Output capacitance (internal to device)			4		pF
DIGITAL OUTPUTS – LVDS MODE					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\|V_{OD}\|$			350		mV
V_{OS} Output offset voltage	Common-mode voltage of OUTP and OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		4		pF
Change in $\|V_{OD}\|$, $\|\Delta V_{OD}\|$			25		mV
Change in $\|V_{OS}\|$, $\|\Delta V_{OS}\|$			25		mV

(1) All LVDS and CMOS specifications are characterized, but not tested at production.
(2) I_O refers to the LVDS buffer current setting, R_L is the differential load resistance between the LVDS output pair.

TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling frequency = 190 MSPS, sine wave input clock, C_L = 5 pF(2) , no internal termination, I_O = 3.5 mA, R_L = 100 Ω(3), unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			1.2		ns
t_j	Aperture jitter			200		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		TBD		
		Time to valid data after stopping and restarting the input clock		TBD		
DDR LVDS MODE(4)						
	Latency			11		Clock cycles
	LVDS bit clock duty cycle			50%		
t_{su}	Data setup time(5)	Data valid(6) to zero-crossing of CLKOUTP rising edge		1000		ps
t_h	Data hold time(5)	Zero-crossing of CLKOUTP rising edge to data becoming invalid(6)		1150		ps

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_L is the effective external single-ended load capacitance between each output pin and ground.
(3) Io refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
(6) Data valid refers to logic high of +100 mV and logic low of -100 mV.

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TIMING CHARACTERISTICS – LVDS AND CMOS MODES (continued)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling frequency = 190 MSPS, sine wave input clock, C_L = 5 pF , no internal termination, I_O = 3.5 mA, R_L = 100 Ω, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over		1.95		ns
t_r	Data rise time	Rise time measured from –100 mV to 100 mV		160		ps
t_f	Data fall time	Fall time measured from –100 mV to 100 mV		160		ps
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		500		ns
PARALLEL CMOS MODE						
	Latency			11		Clock cycles
	CMOS output clock duty cycle			50%		
t_{su}	Data setup time	Data valid(7) to 50% of CLKOUT rising edge		2.8		ns
t_h	Data hold time	50% of CLKOUT rising edge to data becoming invalid(7)		0.3		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to 50% of CLKOUT rising edge		3.5		ns
t_{RISE}	Data rise time	Rise time measured from 20% to 80% of DRVDD		1.2		ns
t_{FALL}	Data fall time	Fall time measured from 80% to 20% of DRVDD		1.2		ns
t_{OE}	Output Enable (OE) to data delay	Time to valid data after OE becomes active		20		ns

(7) Data valid refers to logic high of 2 V and logic low of 0.8 V

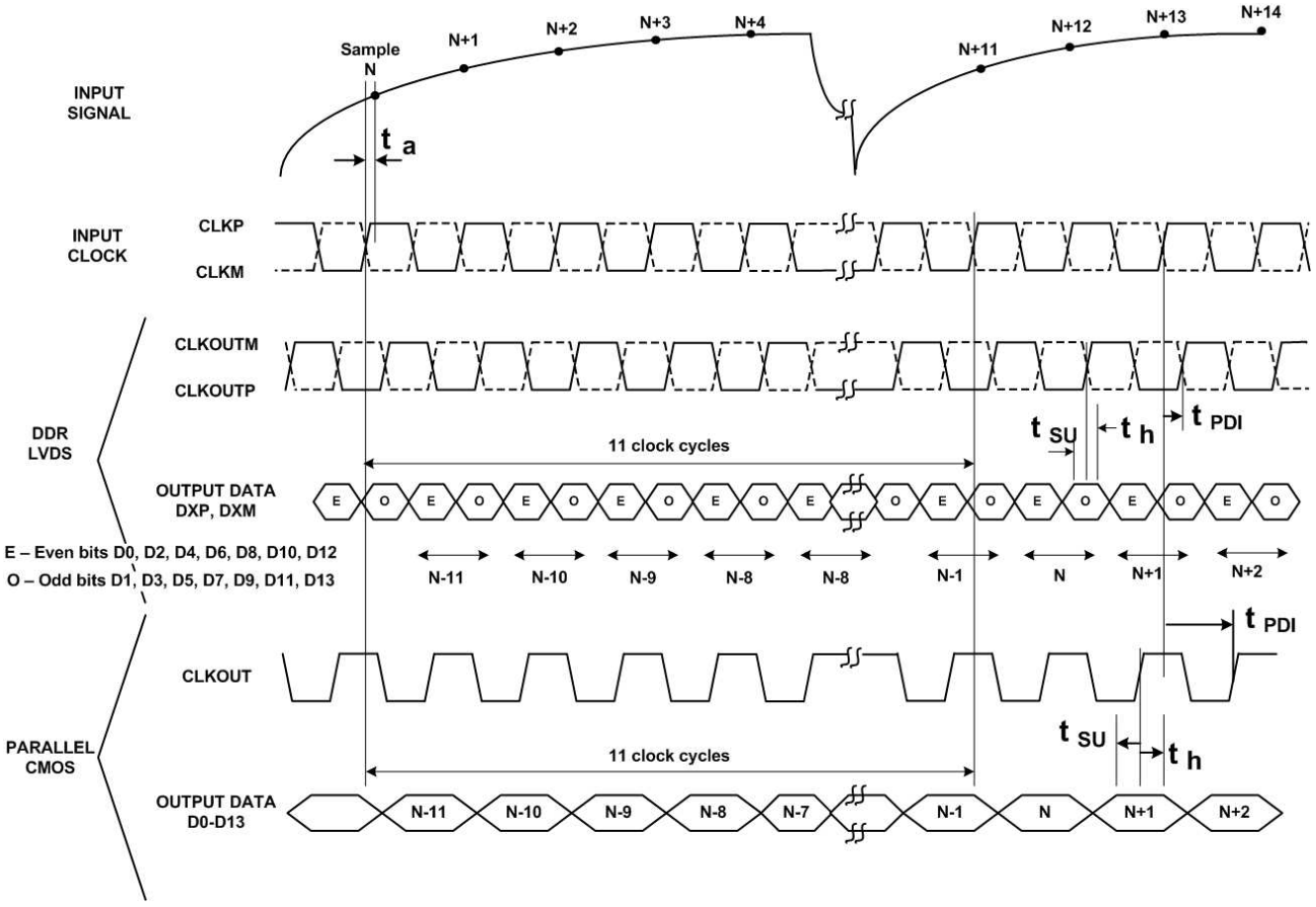

Figure 1. Latency

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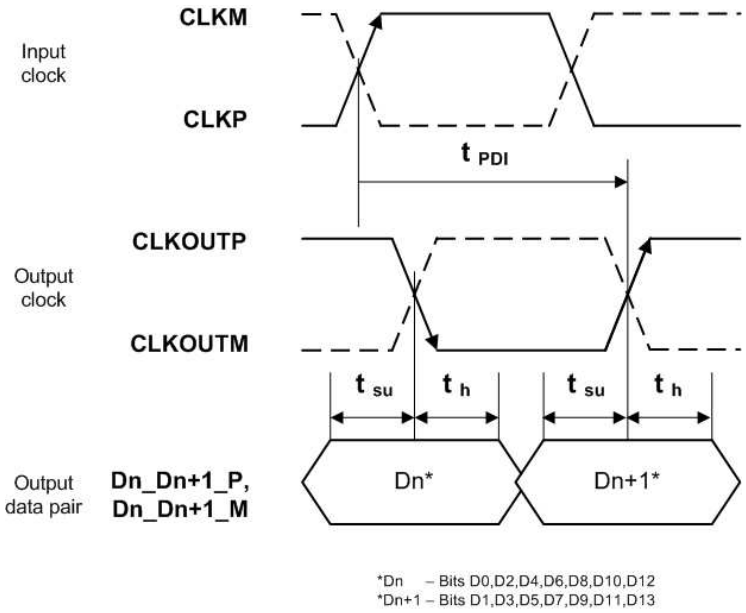

Figure 2. LVDS Mode Timing

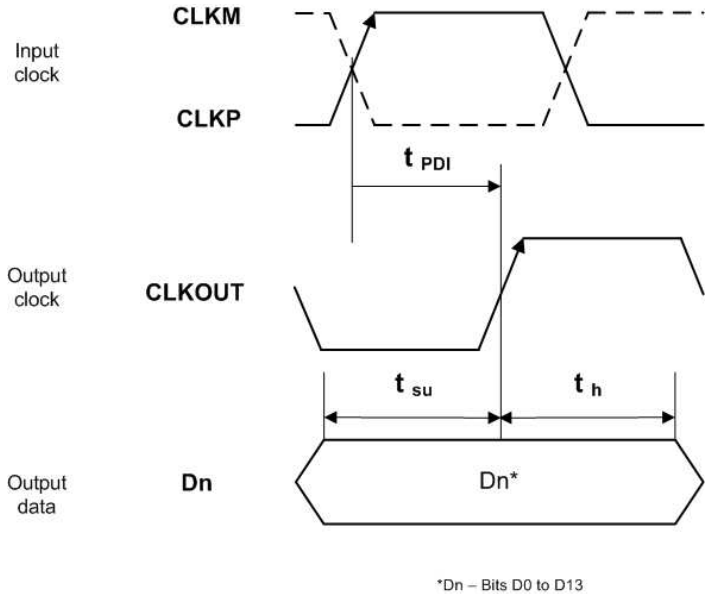

Figure 3. CMOS Mode Timing

DEVICE MODES CONFIGURATION

The ADS5546 offers great flexibility without increase in complexity. The device offers two methods to set its configuration: a parallel mode and a serial mode to access more advanced functions. The selection between one or the other is done by the use of RESET, pin 30.

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Tying RESET permanently to high (DRVDD) sets the device in parallel mode configuration. It is not required to pulse RESET after power up. In this mode, simply connecting the control pins (as described in the parallel pin control section) to the right levels will configure the device. Frequently used functions can be controlled in this mode - standby, selection between LVDS/CMOS output format, internal/external reference, two's complement/straight binary output format and position of the output clock edge.

For more advanced functions, the ADS5546 has a set of internal registers that can be accessed through the serial interface. This interface requires a pulse on RESET (which resets the internal registers to an initial state) and three control signals which enable serial access to the registers after their reset. The serial interface section describes this in more detail.

PARALLEL PIN CONTROL

The pins DFS, MODE, SEN and SDATA can be used to directly control certain modes of the ADC. Pins SEN and SDATA have dual functions as either serial or parallel interfaces, determined by the RESET pin. When RESET is high, the two pins function as parallel interface and when RESET is low, they act as serial interface lines. Pins DFS and MODE always function in parallel control mode, irrespective of RESET pin condition. There is no need for a reset pulse of any kind. Tying the RESET pin high (DRVDD) puts the device in this mode and the device configuration is set by the levels on the four control pins.

Table 1 has a brief description of the modes controlled by the four parallel pins.

Table 1. Parallel Pin Definition

PIN	CONTROL MODES
DFS	DATA FORMAT and the LVDS/CMOS output interface
MODE	Internal or external reference
SEN(1)	CLKOUT edge programmability
SDATA(1)	STANDBY mode – Global (ADC, internal references and output buffers are powered down)

(1) The CLKOUT edge and POWER DOWN modes are controlled by SEN and SDATA only when RESET is high. When RESET is low, these modes can be controlled from the serial interface registers.

A detailed description of the modes set by each parallel interface pin is given in Table 2 through Table 5.

Table 2. SDATA Control Pin

SDATA (Pin 28)	DESCRIPTION
0	Normal operation (Default)
DRVDD	STANDBY. This is a global power down, where ADC, internal references and the output buffers are powered down.

Table 3. SEN Control Pin

SEN (Pin 27)	DESCRIPTION
0	CMOS Mode: Rising and falling edge later by 5 Fs/36; LVDS mode: unused
DRVDD/3	CMOS Mode: Rising and falling edge later by Fs/12; LVDS mode: unused
2DRVDD/3	CMOS Mode: Rising and falling edge earlier by Fs/12; LVDS mode: Rising and falling edge later by Fs/12
DRVDD	Default CLKOUT position

Table 4. DFS Control Pin

DFS (Pin 6)	DESCRIPTION
0	2s complement data and DDR LVDS output (Default)
DRVDD/3	2s complement data and parallel CMOS output
2DRVDD/3	Offset binary data and parallel CMOS output
DRVDD	Offset binary data and DDR LVDS output

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Table 5. MODE Control Pin

MODE (Pin 23)	DESCRIPTION
0	Internal reference
AVDD/3	External reference
2AVDD/3	Externall reference
AVDD	Internal reference

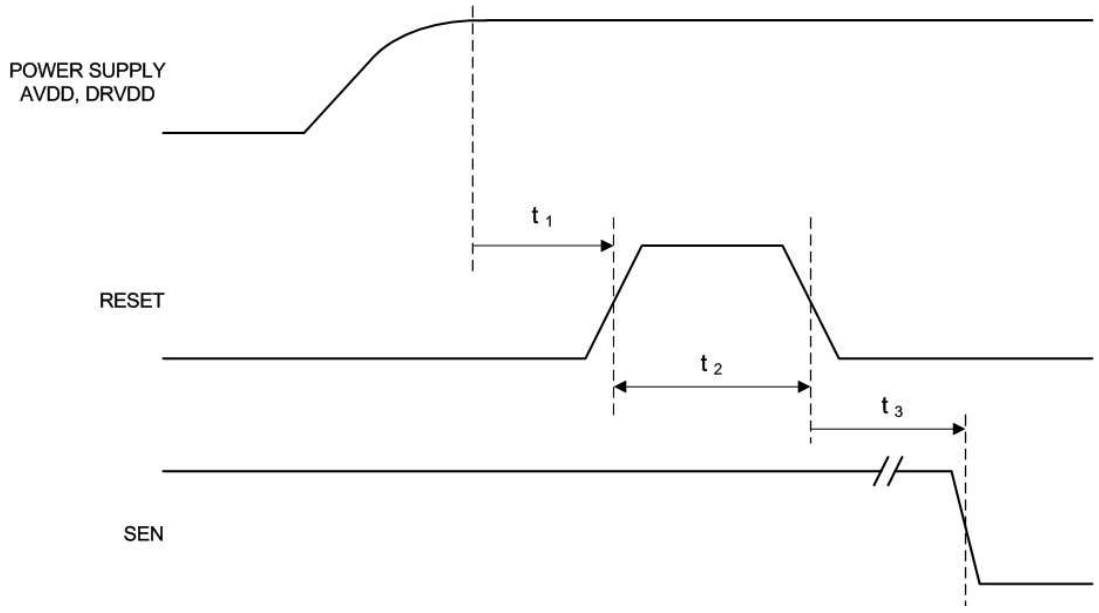
SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns).

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active		TBD		ns
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active		TBD		ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		6.5		ms



NOTE: A high-going pulse on RESET is required only in the serial interface mode. For parallel interface operation, RESET has to be tied high.

Figure 4. Reset Timing Diagram

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Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits form the register data.

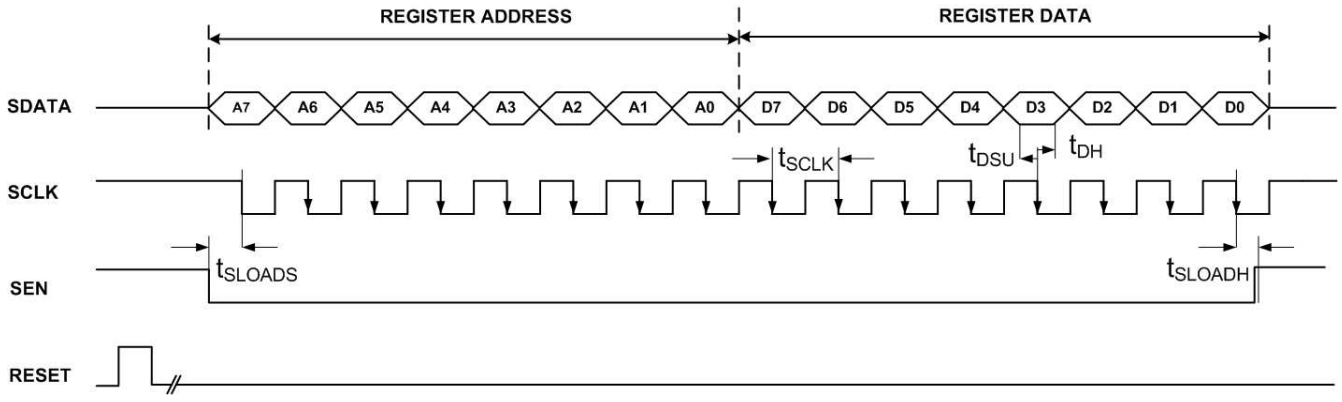

Figure 5. Serial Interface Timing Diagram

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SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK period	50			ns
	SCLK duty cycle		50%		
t_{SLOADS}	SEN to SCLK setup time		25		ns
t_{SLOADH}	SCLK to SEN hold time		25		ns
t_{DS}	SDATA setup time		25		ns
t_{DH}	SDATA hold time		25		ns

In serial interface mode (RESET is low), the pins MODE and DFS can still configure the device. To ensure that only the internal registers can configure the device, connect MODE and DFS to ground.

In the case where the user is required to configure the device through a combination of internal registers and the pins MODE and DFS, the priority in Table 6 applies.

Table 6. Priority Between Pin and Register Bits in Serial Interface Mode

Pin	Modes	Priority
MODE	Internal/External reference	When using the serial interface, the respective register bits control these modes, ONLY if the MODE pin is tied low.
DFS	DATA FORMAT	When using the serial interface, the respective register bits control these modes, ONLY if the DFS pin is tied low.
	LVDS/CMOS	When using the serial interface, the respective register bits override the DFS pin condition.

Table 7 gives a summary of all the modes that can be programmed through the serial interface.

Table 7. Serial Interface Register Map

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<STBY> – Global Power Down																
0	1	1	0	0	0	1	1	**0**	0	0	0	0	0	0	0	NORMAL converter operation
0	1	1	0	0	0	1	1	**1**	0	0	0	0	0	0	0	STANDBY
<DF> – Output Data Format																
0	1	1	0	0	0	1	1	0	0	0	0	**0**	0	0	0	2s complement output format
0	1	1	0	0	0	1	1	0	0	0	0	**1**	0	0	0	Straight binary output format
<ODI> – Output Data Interface																
0	1	1	0	1	1	0	0	0	0	0	**0**	**1**	0	0	0	DDR LVDS outputs
0	1	1	0	1	1	0	0	0	0	0	**1**	**1**	0	0	0	Parallel CMOS outputs
<REF> –Internal/External reference mode																
0	1	1	0	1	1	0	1	0	0	0	**0**	0	0	0	0	Internal reference
0	1	1	0	1	1	0	1	0	0	0	**1**	0	0	0	0	External reference – Force voltage on VCM pin
<TEST PATTERN> – Output test pattern on data outputs																
0	1	1	0	0	1	0	1	**0**	**0**	**0**	0	0	0	0	0	Normal operation
0	1	1	0	0	1	0	1	**0**	**0**	**1**	0	0	0	0	0	All zeros
0	1	1	0	0	1	0	1	**0**	**1**	**0**	0	0	0	0	0	All ones
0	1	1	0	0	1	0	1	**0**	**1**	**1**	0	0	0	0	0	Toggle pattern Alternate 1s and 0s on each data output and across the data outputs.
0	1	1	0	0	1	0	1	**1**	**0**	**0**	0	0	0	0	0	Ramp pattern – Output data ramps from 0x0000 to 0x3FFF every clock cycle
0	1	1	0	0	1	0	1	**1**	**0**	**1**	0	0	0	0	0	Custom pattern. Write the custom pattern in CUSTOM PATTERN registers A and B.
0	1	1	0	0	1	0	1	**X**	**X**	**X**	0	0	0	0	0	NOT USED
<CUSTOM PATTERN> – Output custom pattern on data outputs																
0	1	1	0	1	0	0	1	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	CUSTOM PATTERN D7-D0
0	1	1	0	1	0	1	0	0	0	**D13**	**D12**	**D11**	**D10**	**D9**	**D9**	CUSTOM PATTERN D13-D8
<CLK GAIN> – Clock Buffer gain programmablity, Gain Decreases monotonically from Gain 5 to Gain 0																
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**1**	**0**	Gain 5 Maximum gain
0	1	1	0	1	0	1	1	0	0	**1**	**1**	**0**	**0**	**1**	**0**	Gain 4
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	Gain 3
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**1**	**1**	**0**	Gain 2
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**0**	**0**	Gain 1 Default gain
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**1**	**1**	Gain 0 Minimum gain
<POWER SCALING> Power vs sampling frequency scaling																
0	1	1	0	1	1	0	1	**0**	**0**	**1**	0	0	0	0	0	Deafult Fs > 150 MSPS
0	1	1	0	1	1	0	1	**1**	**0**	**1**	0	0	0	0	0	Power Mode 1 – 125 < Fs ≤ 150 MSPS
0	1	1	0	1	1	0	1	**0**	**1**	**1**	0	0	0	0	0	Power Mode 2 – 65 < Fs ≤ 125 MSPS
0	1	1	0	1	1	0	1	**1**	**1**	**1**	0	0	0	0	0	Power Mode 3 – Fs ≤ 65 MSPS
<LVDS CURRENT> – Output data and clock buffers nominal current programmability																
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**0**	Deafult 3.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**1**	2.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**0**	4.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**1**	1.75 mA

PRODUCT PREVIEW

Table 7. Serial Interface Register Map (continued)

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<CURRENT DOUBLE> – Output data and clock buffer current double programmability																
0	1	1	1	1	1	1	1	**0**	**0**	0	0	0	0	0	0	Default, value specified by <LVDS CURRENT>
0	1	1	1	1	1	1	1	**0**	**1**	0	0	0	0	0	0	2x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**0**	0	0	0	0	0	0	1x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**1**	0	0	0	0	0	0	2x data, 4x clock currents
<DATA TERM> – Output data internal termination programmability																
0	1	1	1	1	1	1	1	**0**	**0**	**0**	0	0	0	0	0	No termination
0	1	1	1	1	1	1	1	**0**	**0**	**1**	0	0	0	0	0	325 Ω
0	1	1	1	1	1	1	1	**0**	**1**	**0**	0	0	0	0	0	200 Ω
0	1	1	1	1	1	1	1	**0**	**1**	**1**	0	0	0	0	0	125 Ω
0	1	1	1	1	1	1	1	**1**	**0**	**0**	0	0	0	0	0	170 Ω
0	1	1	1	1	1	1	1	**1**	**0**	**1**	0	0	0	0	0	120 Ω
0	1	1	1	1	1	1	1	**1**	**1**	**0**	0	0	0	0	0	100 Ω
0	1	1	1	1	1	1	1	**1**	**1**	**1**	0	0	0	0	0	75 Ω
<CLK TERM> – Output clock internal termination programmability																
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**0**	0	0	No termination
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**1**	0	0	325 Ω
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**0**	0	0	200 Ω
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**1**	0	0	125 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**0**	0	0	170 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**1**	0	0	120 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**0**	0	0	100 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**1**	0	0	75 Ω
<CLKOUT POSN CMOS> – Output clock rising edge programmability in CMOS mode																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	Rising edge earlier by Fs/12
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**0**	**1**	Rising edge later by Fs/12
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**1**	**1**	Rising edge earlier by 5Fs/36
<CLKOUT POSN CMOS> – Output clock falling edge programmability in CMOS mode																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	1	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	1	Falling edge earlier by Fs/12
0	1	1	0	0	0	1	0	0	0	0	**1**	**0**	0	0	1	Falling edge later by Fs/12
0	1	1	0	0	0	1	0	0	0	0	**1**	**1**	0	0	1	Falling edge later by 5Fs/36
<CLKOUT POSN LVDS> – Output clock rising edge programmability in LVDS mode																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	Rising edge later by Fs/12
<CLKOUT POSN LVDS> – Output clock falling edge programmability in LVDS mode																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	**1**	Falling edge later by Fs/12

PRODUCT PREVIEW

PIN CONFIGURATION (LVDS MODE)

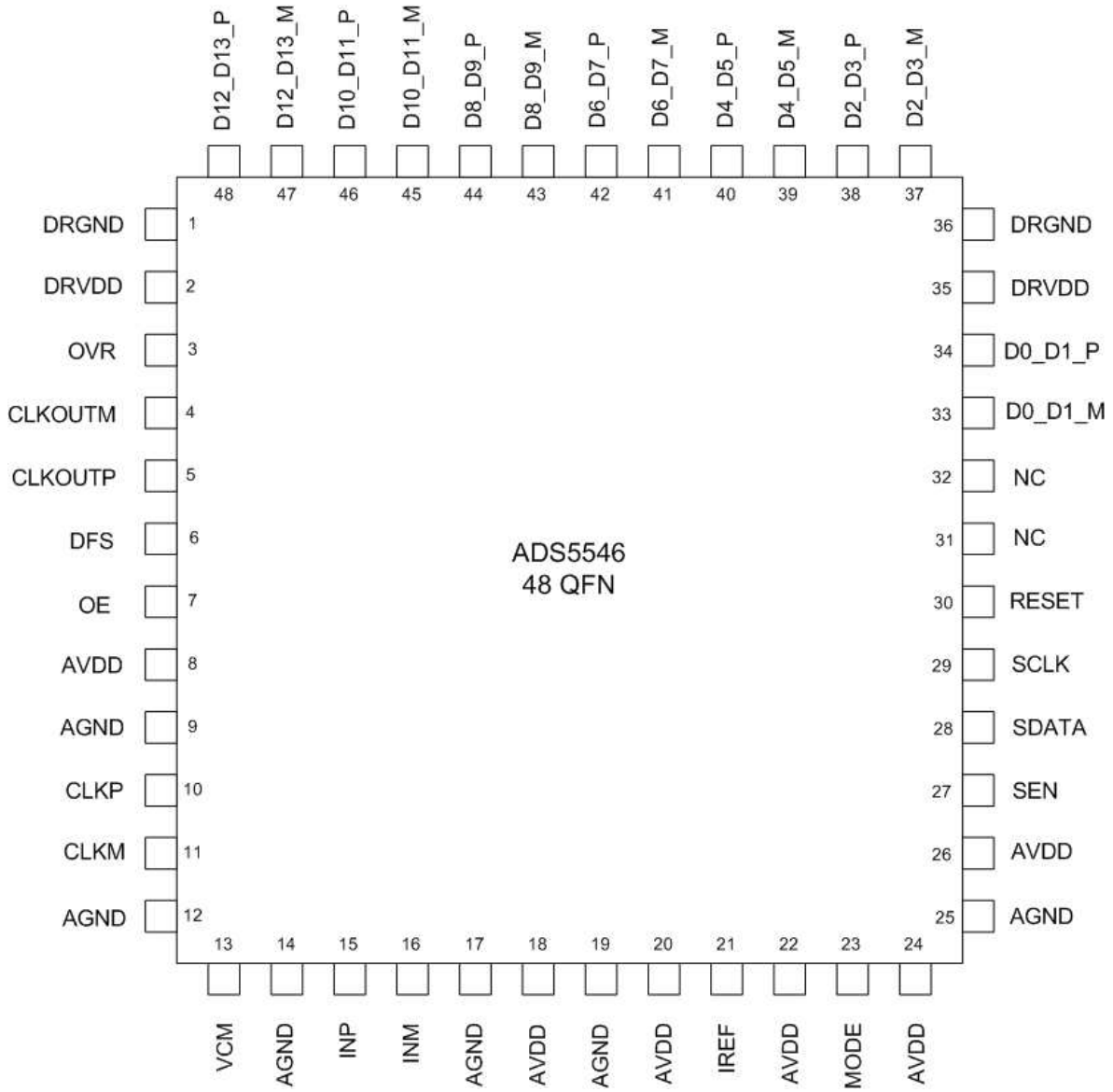

Figure 6. LVDS Mode Pinout

PIN ASSIGNMENTS – LVDS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
IREF	Current-set resistor, 56.2-kΩ resistor to ground.	I	21	1

PRODUCT PREVIEW

PIN ASSIGNMENTS – LVDS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
RESET	Serial interface reset input. When using the serial interface, the user should apply a high-going pulse on this pin to reset the internal registers. When the serial interface is not used, the user should tie RESET permanently high. (SDATA and SEN can be used as parallel pin controls). The pin has an internal 100-kΩ pull-down resistor.	I	30	1
SCLK	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.	I	29	1
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 2 for detailed information. The pin has an internal 100 kΩ pull-down resistor to DRVDD.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 3 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 4 for detailed information.	I	6	1
MODE	Mode select input. This pin selects the Internal or External reference mode. See Table 5 for detailed information.	I	23	1
CLKOUTP	Differential output clock, true	O	5	1
CLKOUTM	Differential output clock, complement	O	4	1
D0_D1_P	Differential output data D0 and D1 multiplexed, true	O	34	1
D0_D1_M	Differential output data D0 and D1 multiplexed, complement.	O	33	1
D2_D3_P	Differential output data D2 and D3 multiplexed, true	O	38	1
D2_D3_M	Differential output data D2 and D3 multiplexed, complement	O	37	1
D4_D5_P	Differential output data D4 and D5 multiplexed, true	O	40	1
D4_D5_M	Differential output data D4 and D5 multiplexed, complement	O	39	1
D6_D7_P	Differential output data D6 and D7 multiplexed, true	O	42	1
D6_D7_M	Differential output data D6 and D7 multiplexed, complement	O	41	1
D8_D9_P	Differential output data D8 and D9 multiplexed, true	O	44	1
D8_D9_M	Differential output data D8 and D9 multiplexed, complement	O	43	1
D10_D11_P	Differential output data D10 and D11 multiplexed, true	O	46	1
D10_D11_M	Differential output data D10 and D11 multiplexed, complement	O	45	1
D12_D13_P	Differential output data D12 and D13 multiplexed, true	O	48	1
D12_D13_M	Differential output data D12 and D13 multiplexed, complement	O	47	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
NC	Do not connect		31, 32	2

PRODUCT PREVIEW

PIN CONFIGURATION (CMOS MODE)

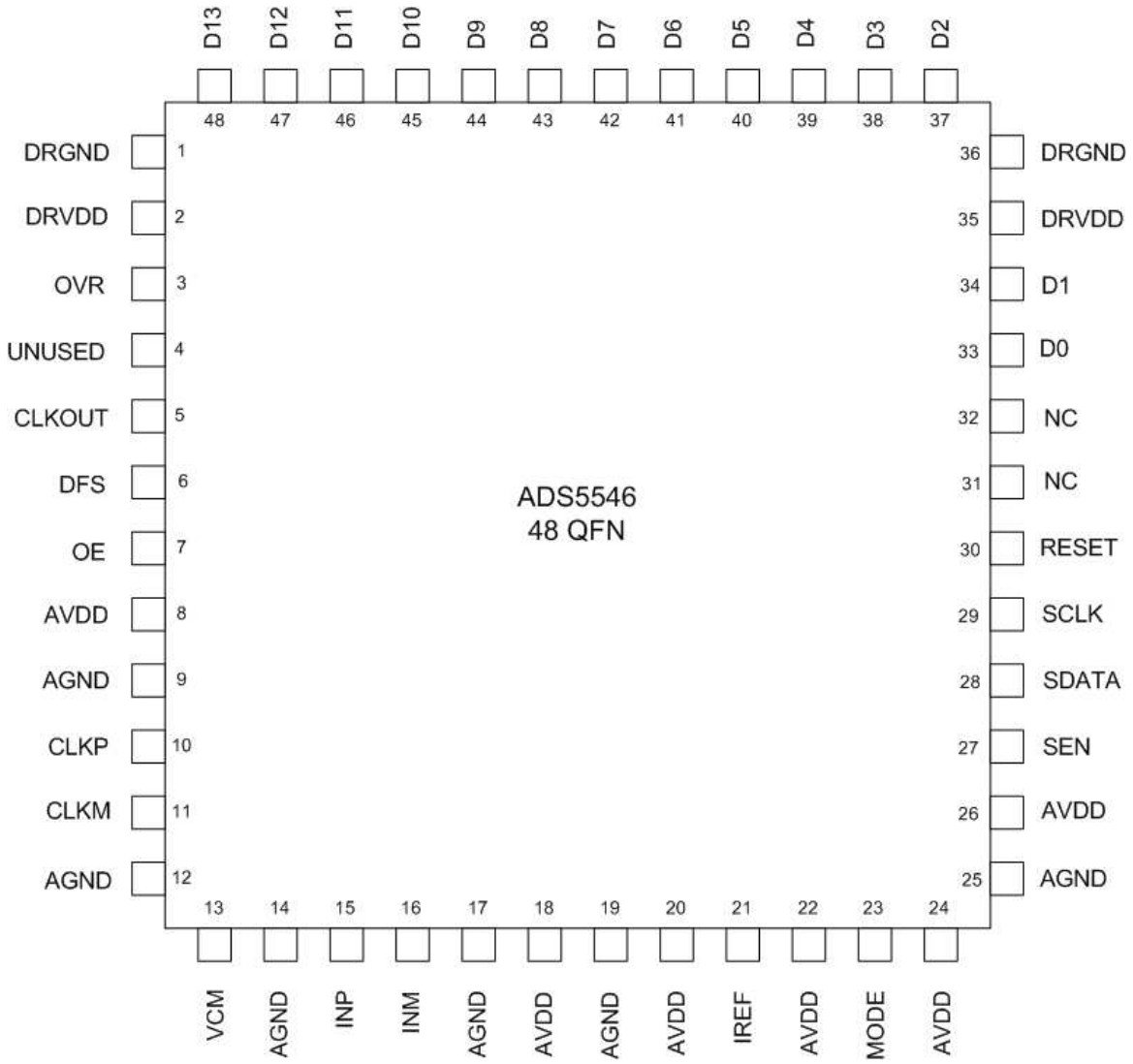

Figure 7. CMOS Mode Pinout

PIN ASSIGNMENTS – CMOS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
IREF	Current-set resistor, 56.2-kΩ resistor to ground.	I	21	1
RESET	Serial interface reset input. When using the serial interface, the user should apply a high-going pulse on this pin to reset the internal registers.	I	30	1

PRODUCT PREVIEW

PIN ASSIGNMENTS – CMOS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
	When the serial interface is not used, the user should tie RESET permanently high. (SDATA and SEN can be used as parallel pin controls). The pin has an internal 100-kΩ pull-down resistor.			
SCLK	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.	I	29	1
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 2 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 3 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 4 for detailed information.	I	6	1
MODE	Mode select input. This pin selects the internal or external reference mode. See Table 5 for detailed information.	I	23	1
CLKOUT	CMOS output clock	O	5	1
D0	CMOS output data D0	O	33	1
D0	CMOS output data D1	O	34	1
D2	CMOS output data D2	O	37	1
D2	CMOS output data D3	O	38	1
D4	CMOS output data D4	O	39	1
D4	CMOS output data D5	O	40	1
D6	CMOS output data D6	O	41	1
D7	CMOS output data D7	O	42	1
D8	CMOS output data D8	O	43	1
D9	CMOS output data D9	O	44	1
D10	CMOS output data D10	O	45	1
D11	CMOS output data D11	O	46	1
D12	CMOS output data D12	O	47	1
D13	CMOS output data D13	O	48	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
UNUSED	Unused pin in CMOS mode		4	1
NC	Do not connect		31, 32	2

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 190 MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, DDR LVDS data output (unless otherwise noted)

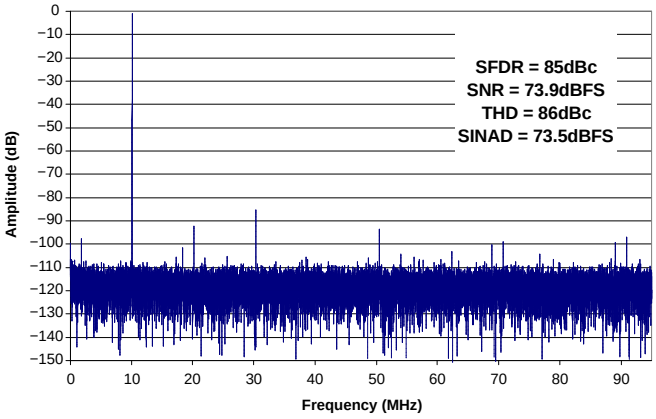

Figure 8.

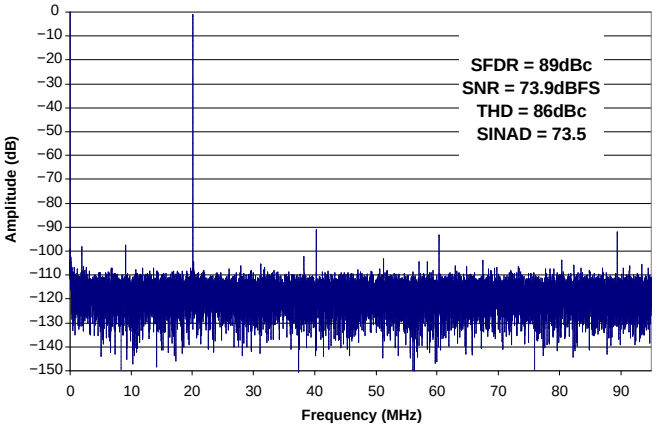

Figure 9.

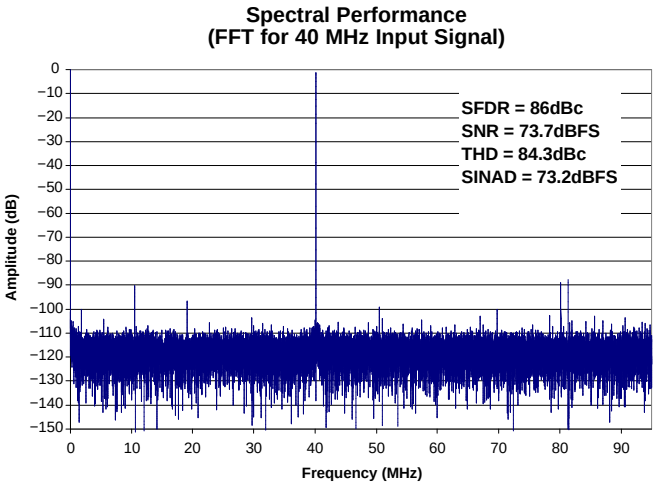

Figure 10.

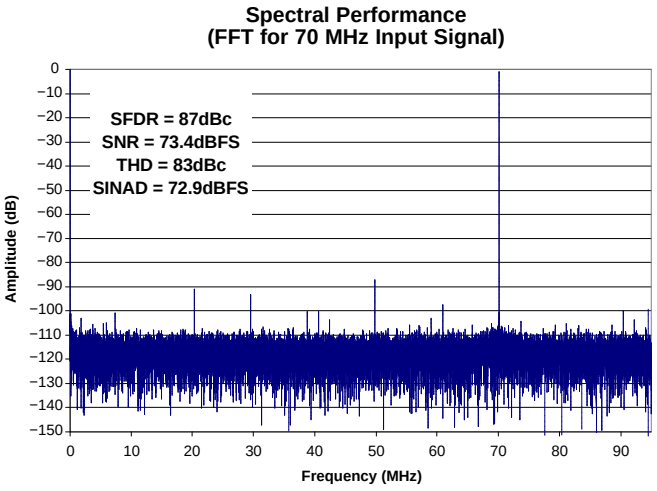

Figure 11.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 190 MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, DDR LVDS data output (unless otherwise noted)

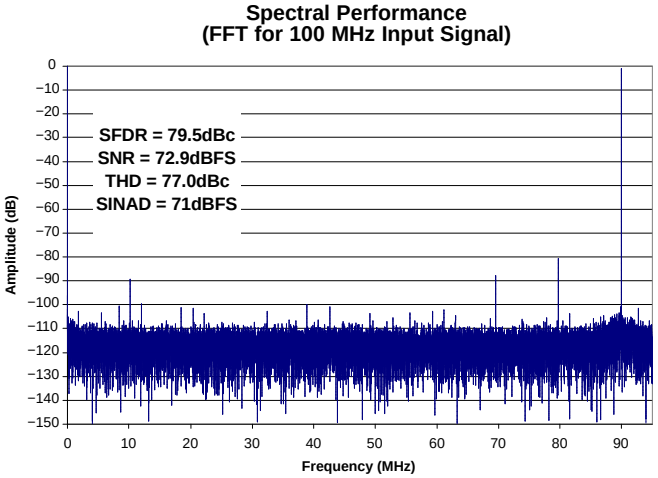

Figure 12.

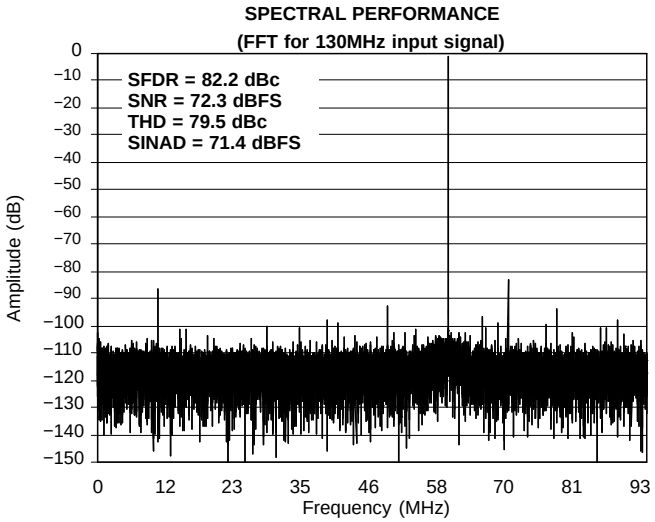

Figure 13.

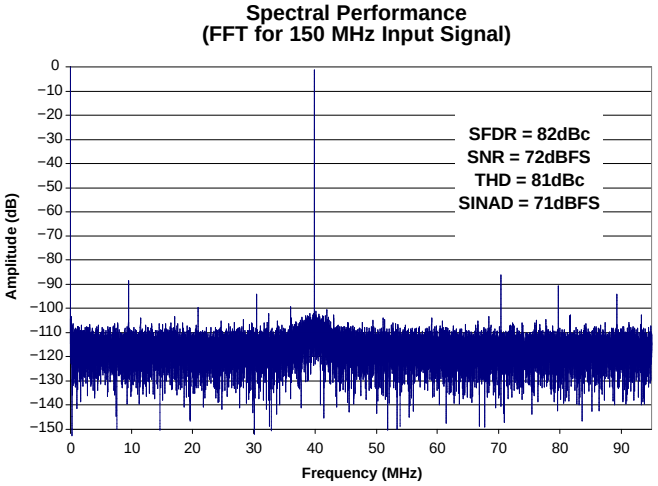

Figure 14.

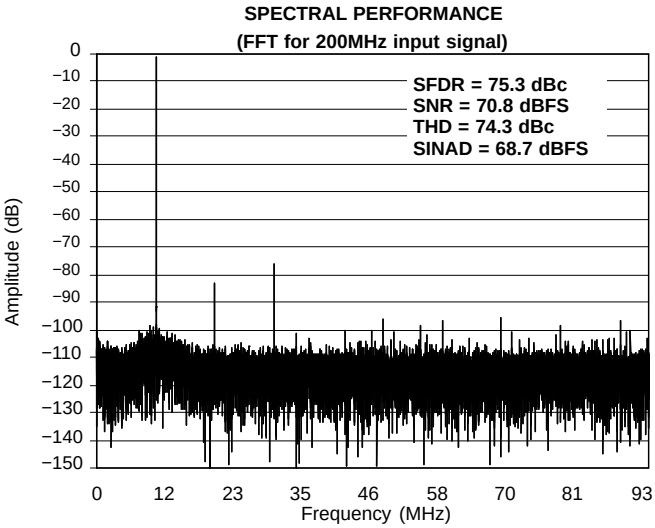

Figure 15.

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TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 190 MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, DDR LVDS data output (unless otherwise noted)

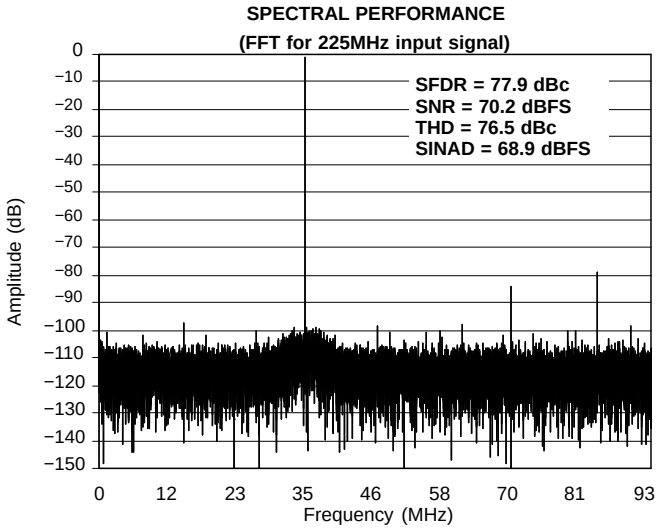

Figure 16.

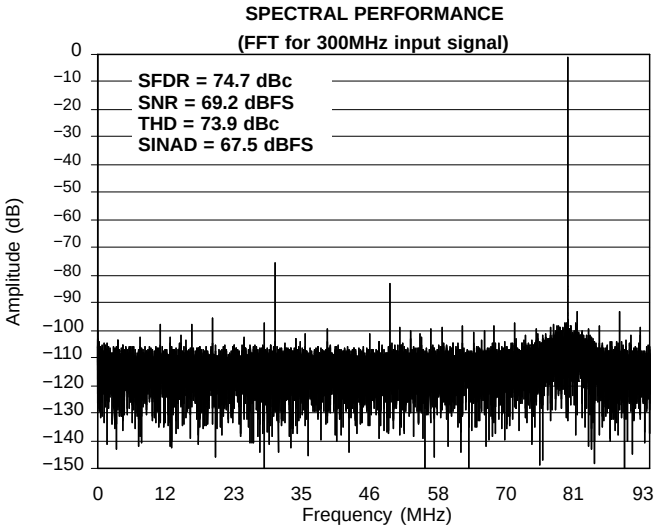

Figure 17.

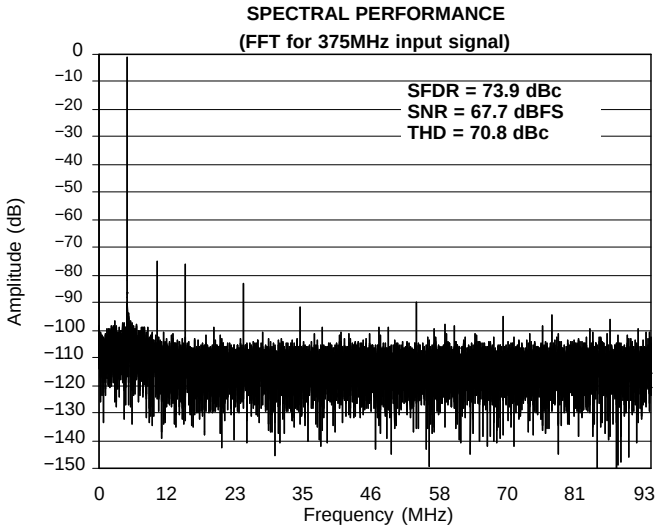

Figure 18.

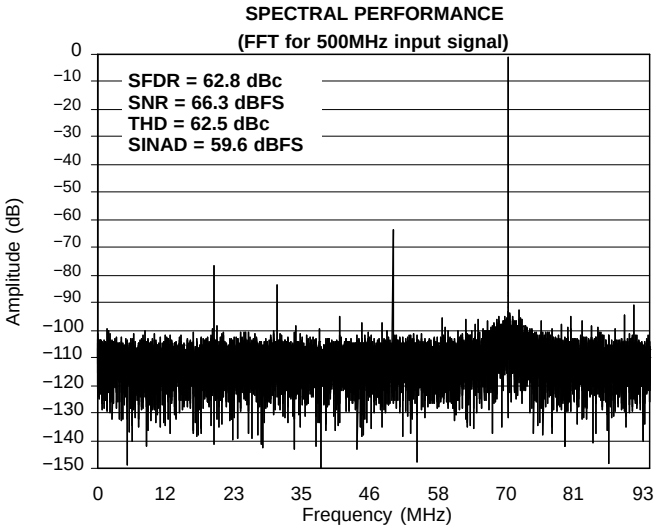

Figure 19.

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APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5546 is a low power 14-bit 190 MSPS pipeline ADC in a CMOS process. The ADS5546 is based on switched capacitor technology and runs off a single 3.3-V supply. The conversion process is initiated by a rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 11 clock cycles. The output is available as 14-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2's complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 20.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-Vpp differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).

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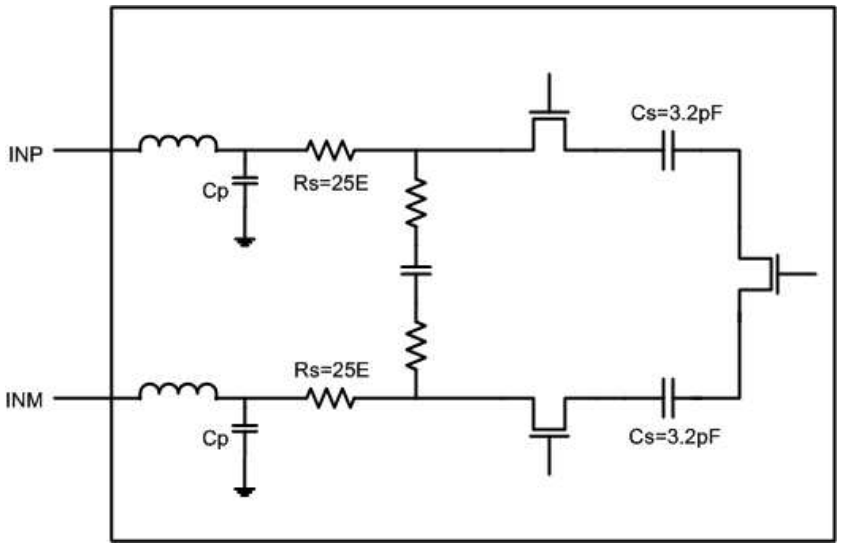

Figure 20. Input Stage

Driving Circuit

For optimum performance, the analog inputs have to be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. Input configurations using RF transformers suitable for low and high input frequencies are shown in Figure 21 and Figure 22. The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated by 50-Ω on the secondary side. Putting the termination on the secondary side helps to shield the kicks caused by the input sampling capacitors from the RF transformer's leakage inductances. The termination is accomplished by two 25 Ω connected in series, with the center point connected to the 1.5-V common-mode (VCM pin 13). The 4.7-Ω resistor in series with each input pin is required to damp the ringing caused by the device package parasitics (shown in Figure 20).

APPLICATION INFORMATION (continued)

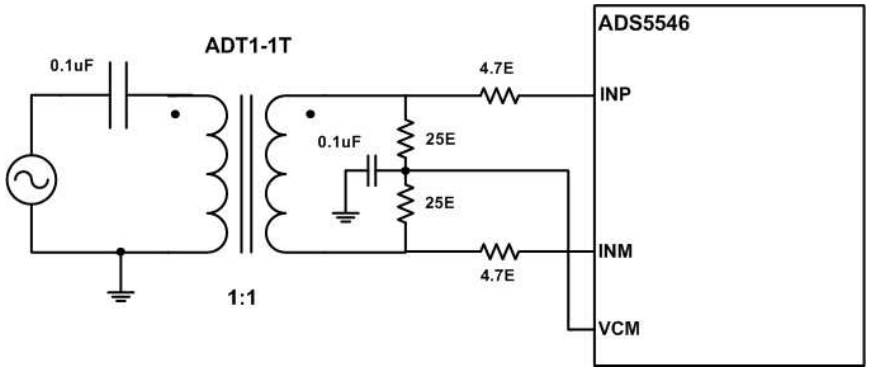

Figure 21. Drive Circuit at Low Input Frequencies

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair is required between the two transformers as shown in the Figure 22. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to get an overall 50 Ω (in the case of 50-Ω source impedance).

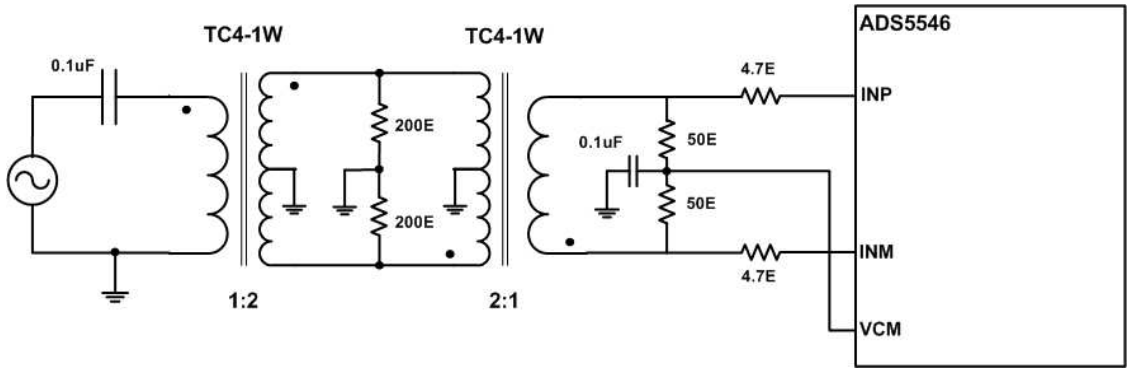

Figure 22. Drive Circuit at High Input Frequencies

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 310 µA (at 190 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{310\mu A \times Fs}{170MSPS} \quad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

Reference

The ADS5546 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by controlling the MODE pin 23 (see Table 5 for details) or by programming the serial interface register bit **<REF>**.

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

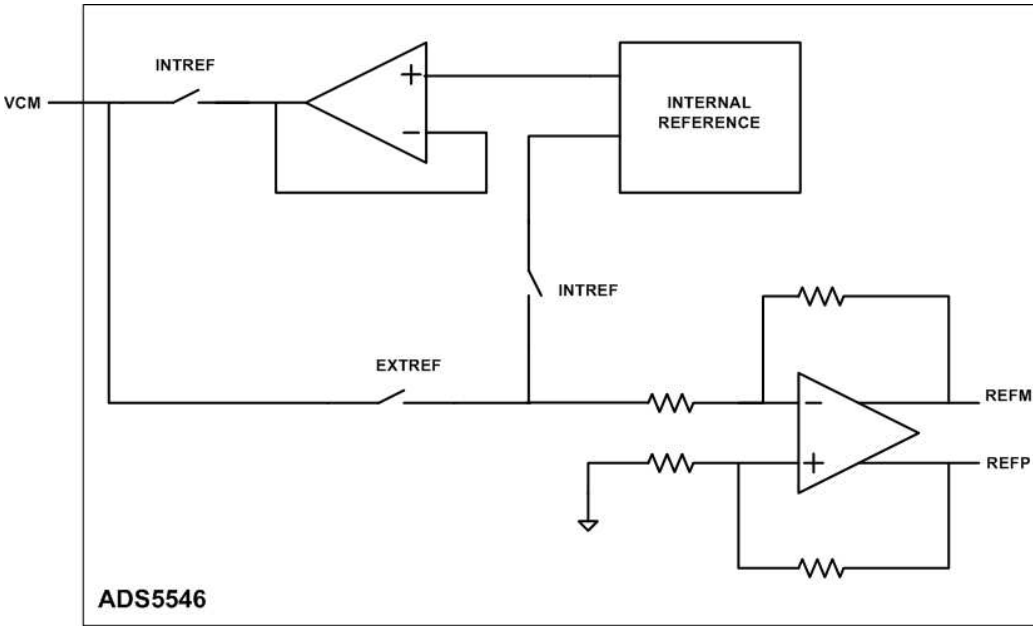

Figure 23. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

$$\text{Full–scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

CLOCK INPUT

The ADS5546 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors that connect CLKP (pin 10) and CLKM (pin 11) to VCM (pin 13), as shown in Figure 24.

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

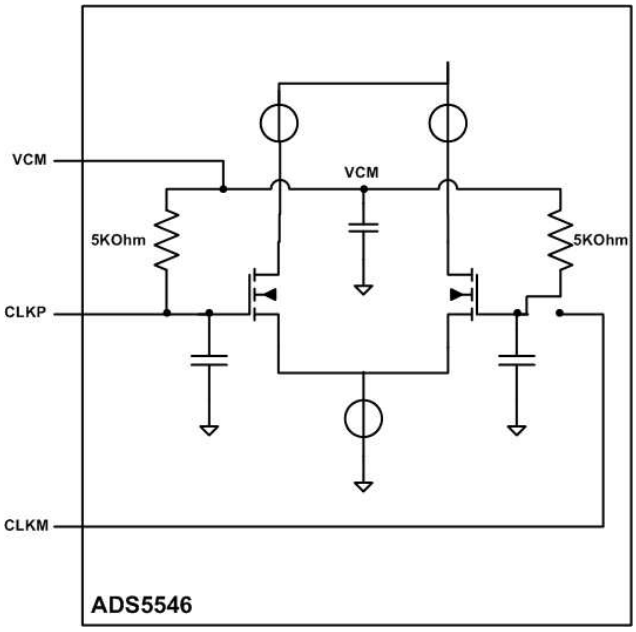

Figure 24. Clock Inputs

For the best performance, it is recommended to drive the clock inputs differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.1-µF capacitors, as shown in Figure 25.

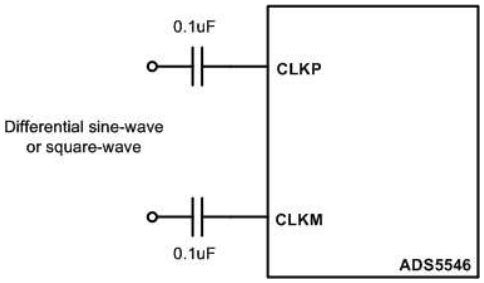

Figure 25. Differential Clock Drive

When driven with a single-ended CMOS clock input, connect CLKM (pin 11) to ground with a 0.1-µF capacitor and CLKP with a 0.1-µF capacitor to the clock source, as shown in Figure 26.

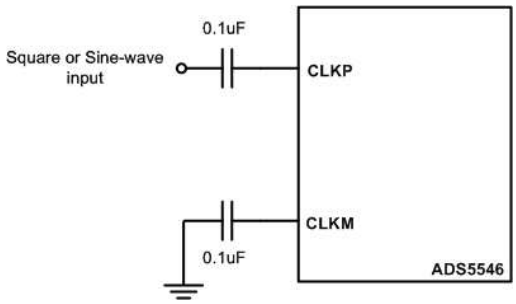

Figure 26. Single-Ended Clock Drive

PRODUCT PREVIEW

APPLICATION INFORMATION (continued)

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is little change in performance with a non-50% duty cycle clock input.

Clock Buffer Gain

When using a sinusoidal clock input, the noise contributed by clock jitter improves as the clock amplitude is increased. In addition, the clock buffer has a programmable gain option to amplify the input clock. For clock inputs with low slew rates , the jitter component of SNR improved with higher clock buffer gain settings. The clock buffer gain can be set by programming the register bits **<CLK GAIN>**. The clock buffer gain decreases monotonically from Gain5 to Gain4 settings.

Table 8. Clock Buffer Gain Programming

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<CLK GAIN> – Clock buffer gain programmability, Gain decreases monotonically from Gain 5 to Gain 0																
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**1**	**0**	Gain 5 Maximum gain
0	1	1	0	1	0	1	1	0	0	**1**	**1**	**0**	**0**	**1**	**0**	Gain 4
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	Gain 3
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**1**	**1**	**0**	Gain 2
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**0**	**0**	Gain 1 Default gain
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**1**	**1**	Gain 0 Minimum gain

Power Down

The ADS5546 has three power-down modes – global STANDBY, output buffer disabled, and input clock stopped.

Global STANDBY

This mode can be initiated by setting the register bit **<STBY>** through the serial interface. In this mode, the A/D converter, reference block and the output buffers are powered down resulting in reduced power dissipation of about 100 mW. The wake-up time from the global power down to normal mode is typically 20 µs.

Output Buffer Disable

The output buffers can be disabled using OE pin 7 in both the LVDS and CMOS modes, reducing the total power by about 100 mW. With the buffers disabled, the outputs are in high impedance state. The wake-up time from this mode to normal mode is typically 500 ns in LVDS mode and 20 ns in CMOS mode.

Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 100 mW and the wake-up time from this mode data becoming valid in normal mode is typically 35 µs.

Power Scaling Modes

The ADS5546 has a power scaling mode in which the device can be operated at reduced power levels at lower sampling frequencies with no difference in performance. There are four power scaling modes for different sampling clock frequency ranges, using the serial interface register bits **<POWER SCALING>**. Only the AVDD power is scaled, leaving the DRVDD power unchanged.

Table 9. Power Scaling vs Sampling Speed

Sampling Frequency, MSPS	Power Scaling Mode(1)	Analog Power Typical, mW	Analog Power in Default Mode, mW
> 150	Default	291 at 170 MSPS	
125 to 150	Power scale 1	255 at 150 MSPS	278 at 150 MSPS

(1) The performance in the power scaling modes is from characterization and not tested in production.

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Table 9. Power Scaling vs Sampling Speed (continued)

Sampling Frequency, MSPS	Power Scaling Mode(1)	Analog Power Typical, mW	Analog Power in Default Mode, mW
65 to 125	Power scale 2	223 at 125 MSPS	268 at 125 MSPS
< 65	Power scale 3	177 at 65 MSPS	245 at 65 MSPS

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<POWER SCALING>																
0	1	1	0	1	1	0	1	**0**	**0**	**1**	0	0	0	0	0	Default Fs> 150 MSPS
0	1	1	0	1	1	0	1	**1**	**0**	**1**	0	0	0	0	0	Power Mode1 125 < Fs ≤ 150 MSPS
0	1	1	0	1	1	0	1	**0**	**1**	**1**	0	0	0	0	0	Power Mode2 65 < Fs ≤ 125 MSPS
0	1	1	0	1	1	0	1	**1**	**1**	**1**	0	0	0	0	0	Power Mode3 Fs ≤ 6 5 MSPS

Power Supply

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

Output Information

The ADS5546 provides 14-bit data, an output clock synchronized with the data and an out-of-range indicator that goes high when the output reaches the full-scale limits. In addition, output enable control (OE pin 7) is provided to power down the output buffers and put the outputs in high-impedance state.

Output Interface

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the DFS (pin 6) or the serial interface register bit **<ODI>** (see Table 4).

DDR LVDS Outputs

In this mode, the 14 data bits and the output clock are put out using LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair as shown in Figure 27. So, there are 7 LVDS output pairs for the 14 data bits and 1 LVDS output pair for the output clock.

PRODUCT PREVIEW

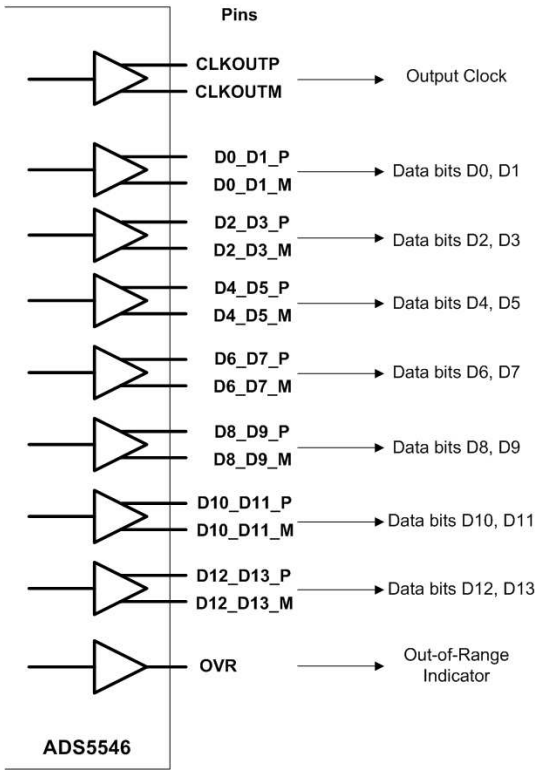

Figure 27. DDR LVDS Outputs

Even data bits D0, D2, D4, D6, D8, D10, and D12 are output at the falling edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9, D11, and D13 are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the 14 data bits (see Figure 28).

PRODUCT PREVIEW

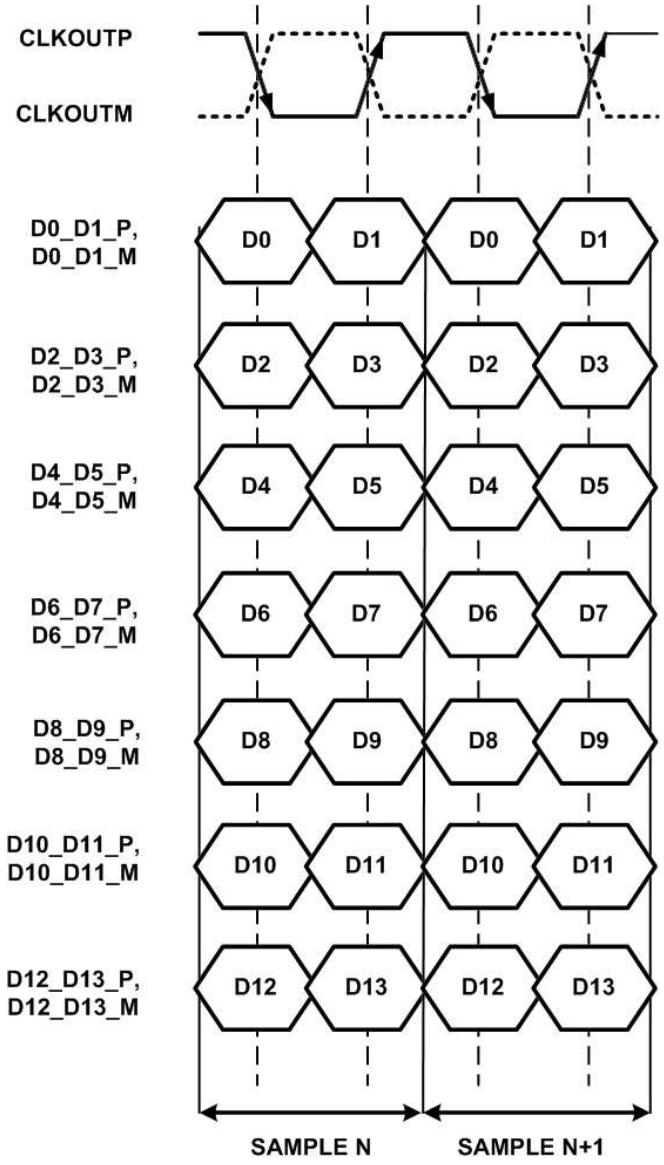

Figure 28. DDR LVDS Interface

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-mVp-p differential swing). The LVDS buffer currents can also be nominal programmed to 2.5 mA, 4 mA, and 4.5 mA using the serial interface. In addition, there exists a current double mode, where this current is doubled for the data and output clock buffers separately.

Both the buffer current programming and the current double mode can be done separately for the data buffers and the output clock buffer.

Table 10. LVDS Buffer Currents Programming

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<LVDS CURRENT> – Output data and clock buffers current programmability																
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**0**	Default 3.5 mA

PRODUCT PREVIEW

Table 10. LVDS Buffer Currents Programming (continued)

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**1**	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**0**	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**1**	
<CURRENT DOUBLE> – Output data and clock buffer current double																
0	1	1	1	1	1	1	1	**0**	**0**	0	0	0	0	0	0	Default, value specified by <LVDS CURRENT>.
0	1	1	1	1	1	1	1	**0**	**1**	0	0	0	0	0	0	2x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**0**	0	0	0	0	0	0	1x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**1**	0	0	0	0	0	0	2x data, 4x clock currents

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are terminated inside the device. Five values of termination resistance are available – 166, 200, 250, 333, and 500 Ω (nominal with ±20% variation). Any combination of these five terminations can be programmed; the effective termination will be the parallel combination of the selected resistances.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100-Ω internal and 100-Ω external termination, the voltage swing at the receiver end will be halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current doube mode (see Table 11).

Table 11. Programming Internal Termination for LVDS Data and Clock

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
R/W	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<DATA TERM> – Output data internal termination programmability																
0	1	1	1	1	1	1	**0**	**0**	**0**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**0**	**0**	**1**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**0**	**1**	**0**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**0**	**1**	**1**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**1**	**0**	**0**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**1**	**0**	**1**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**1**	**1**	**0**	0	0	0	0	0	0	
0	1	1	1	1	1	1	**1**	**1**	**1**	0	0	0	0	0	0	
<CLK TERM> – Output clock internal termination programmability																
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**0**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**1**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**0**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**1**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**0**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**1**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**0**	0	0	
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**1**	0	0	

Parallel CMOS

In this mode, the 14 data outputs and the output clock are put out as 3.3-V CMOS voltage levels. Each data bit and the output clock is available on a separate pin in parallel. By default, the data outputs are valid during the rising edge of the output clock. The output clock is CLKOUT (pin 5).

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Output Clock Position Programmability

In both the LVDS and CMOS modes, the output clock can be moved around its default position. This can be done using SEN pin 27 (as described in Table 5) or using the serial interface register bits **<CLKOUT POSN>**. In CMOS mode there is an option to increase either the set-up or hold times by 1/(12 × Fs) from the default value. In LVDS mode there is an option to only increase the setup time by 1/(12 × Fs) and 1/12 × Fs).

Table 12. CLKOUT Position Programing

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<CLKOUT POSN CMOS> – Output clock rising edge programmability in CMOS mode																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	Rising edge earlier by Fs/12
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**0**	**1**	Rising edge later by Fs/12
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**1**	**1**	Rising edge earlier by 5Fs/36
<CLKOUT POSN CMOS> – Output clock falling edge programmability in CMOS mode																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	1	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	1	Falling edge earlier by Fs/12
0	1	1	0	0	0	1	0	0	0	0	**1**	**0**	0	0	1	Falling edge later by Fs/12
0	1	1	0	0	0	1	0	0	0	0	**1**	**1**	0	0	1	Falling edge later by 5Fs/36
<CLKOUT POSN LVDS> – Output clock rising edge programmability in LVDS mode																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	Rising edge later by Fs/12
<CLKOUT POSN LVDS> – Output clock falling edge programmability in LVDS mode																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	**1**	Falling edge later by Fs/12

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the DFS (pin 6) or the serial interface register bit **<DFS>** (see Table 7). In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.

PRODUCT PREVIEW

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

DEFINITION OF SPECIFICATIONS (continued)

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

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Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (3)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (4)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

DEFINITION OF SPECIFICATIONS (continued)

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (5)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS5546IRGZ	PREVIEW	QFN	RGZ	48		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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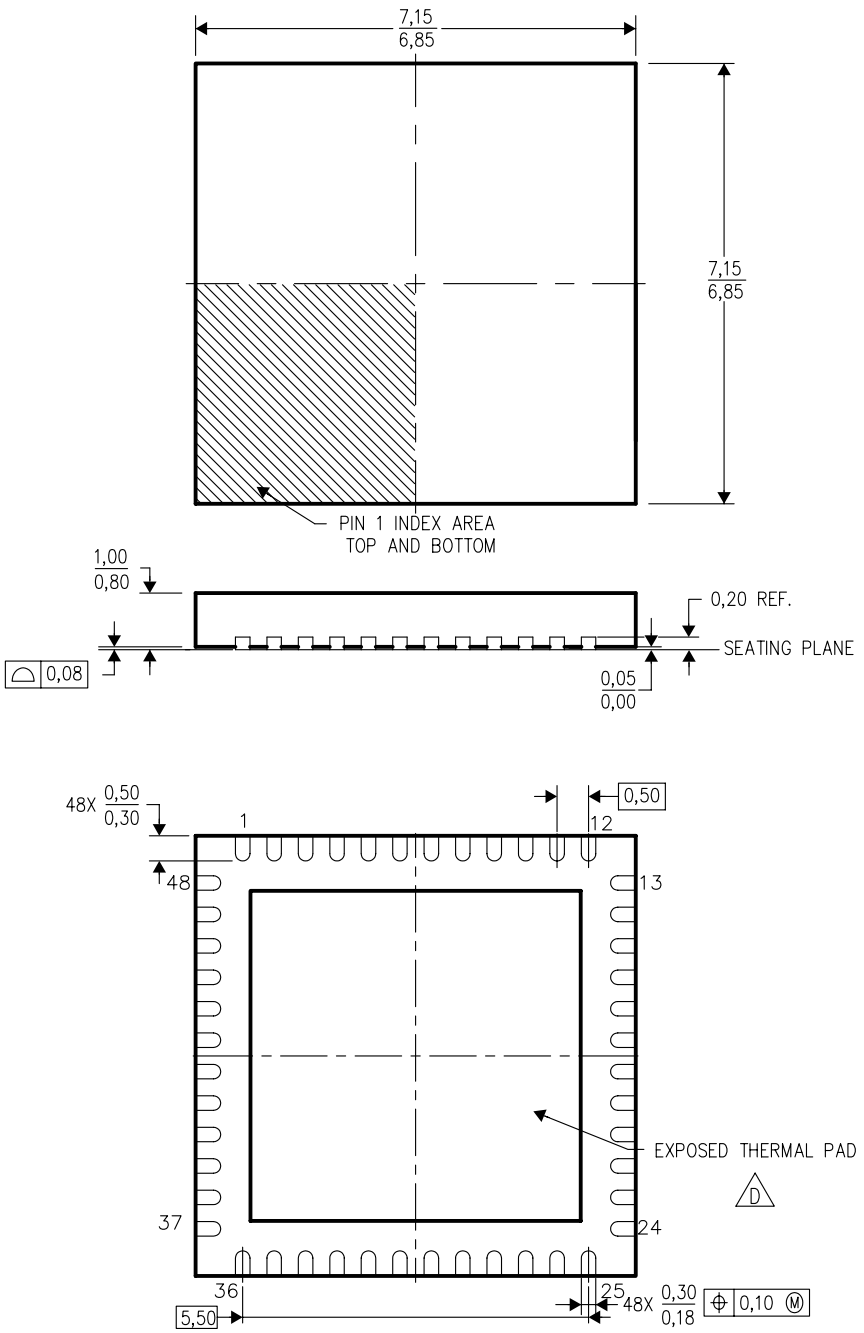
RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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