

NL3S22S

USB 2.0 + Audio Switch

The NL3S22S is a double-pole/double-throw (DPDT) analog switch for routing high speed differential data and audio. The high-speed data path is compliant with High Speed USB 2.0, Full Speed USB 1.1, Low Speed USB 1.0 and any generic UART protocol. The multi-purpose audio path is capable of passing signals with negative voltages as low as 2 V below ground and features shunt resistors to reduce Pop and Click noise in the audio system.

Features

- V_{CC} Range: 2.7 V to 5.5 V
- Control Pins Compatible with 1.8 V Interfaces
- I_{CC} : 23 μ A (Typ)
- ESD Performance: 4 kV HBM
- Available in 1.4 mm x 1.8 mm UQFN10
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

High Speed Data Path

- Input Signal Range: 0 V to 3.7 V
- $R_{DS(on)}$: 5 Ω (Typ)
- C_{ON} : 4.5 pF (Typ)
- Data Rate: USB 2.0-Compliant – up to 480 Mbps

Audio Path

- Input Signal Range: -2.0 V to 2.0 V
- $R_{DS(on)}$: 3 Ω (Typ)
- $R_{ON(FLAT)}$: 0.002 Ω (Typ)
- THD: 0.002% ($R_L = 16 \Omega$ / $V_{IS} = 0.4 V_{RMS}$)

Applications

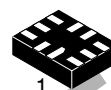
- Smartphones
- Tablets
- USB 2.0 Hosts/Peripherals
- Audio / High-Speeds Data Switching



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MARKING DIAGRAM



UQFN10
CASE 488AT

AW M ■

AW = Device Code
M = Date Code
■ = Pb-Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NL3S22SMUTAG	UQFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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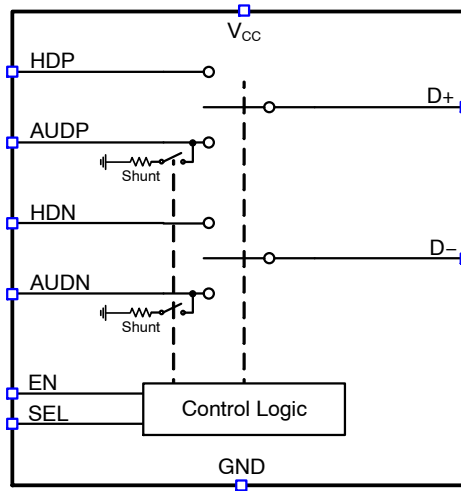


Figure 1. Block Diagram

FUNCTION TABLE

EN	SEL	Shunt Status	D+/D- Function
0	X	ON	No Connect
1	0	OFF	AUDP/AUDN
1	1	ON	HDP/HDN

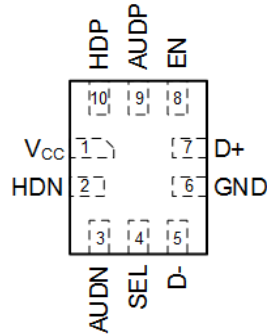


Figure 2. UQFN10 – Top Through View

PIN DESCRIPTION

Pin Name	Pin	Description
V _{CC}	1	Power Supply
HDN	2	High Speed Differential Data (-)
AUDN	3	Audio Signal (-)
SEL	4	Function Select
D-	5	Audio/Data Common I/O (-)
GND	6	Ground
D+	7	Audio/Data Common I/O (+)
EN	8	Chip Enable
AUDP	9	Audio Signal (+)
HDP	10	High Speed Differential Data (+)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V _{CC}	Positive DC Supply Voltage	−0.3 to +6	V
V _{IS}	Analog Input/Output Voltage HDP, HDN	−0.3 to +5.5	V
	AUDP, AUDN	−2.5 to V _{CC} + 0.3	
	D+, D−	−2.5 to +5.5	
V _{IN}	Digital Control Pin Voltage on EN, SEL	−0.3 to V _{CC} + 0.3	V
T _s	Storage Temperature	−55 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C
T _J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity (Note 1)	Level 1	
I _{LU}	Latchup Current (Note 2)	±100	mA
ESD	ESD Protection (Note 3) Human Body Model	4000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.
2. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
3. This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) ±4.0 kV per JEDEC standard: JESD22-A114 for all pins.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CCEN}	Positive DC Supply Voltage	2.7	5.5	V
V _{IS}	Switch Input / Output Voltage (Note 4) HDP, HDN	0	3.7	V
	AUDP, AUDN	−2.0	2.0	
	D+, D−	−2.0	3.7	
V _{IN}	Digital Control Input Voltage	GND	V _{CC}	V
T _A	Operating Temperature Range	−40	+85	°C

4. If the audio channel is not in use, it is recommended that no signals are applied on the audio inputs AUDN and AUDP.

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DC ELECTRICAL CHARACTERISTICS (Typical values are at $V_{CC} = +3.6\text{ V}$ and $T_A = +25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test Conditions	V_{CC} (V)	-40 °C to 85 °C			Unit
				Min	Typ	Max	

POWER SUPPLY

I_{CC}	Supply Current	$I_{IS} = 0\text{ mA}$	4.2	–	23	105	μA
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Control Logic (EN, SEL)

V_{IH}	Input High Voltage		4.2	1.5	–	–	V
			3.6	1.4	–	–	
			2.7	1.3	–	–	
V_{IL}	Input Low Voltage		4.2	–	–	0.4	V
			3.6	–	–	0.4	
			2.7	–	–	0.4	
V_{IHYS}	Input Hysteresis		2.7 – 5.5	–	250	–	mV
I_{IN}	Leakage Current		2.7 – 5.5	–	–	± 150	nA

AUDIO SWITCH (AUDP/AUDN $\leftrightarrow$ D+/D–)

R_{ON}	ON-Resistance	$V_{IS} = -2.0\text{ V to } 2.0\text{ V}, I_{IS} = 50\text{ mA}$	3.0	–	3	5	Ω
ΔR_{ON}	ON-Resistance Matching Between Channels	$V_{IS} = -2.0\text{ V to } 2.0\text{ V}, I_{IS} = 50\text{ mA}$	3.0	–	0.05	–	Ω
$R_{FLAT(ON)}$	ON Resistance Flatness	$V_{IS} = -2.0\text{ V to } 2.0\text{ V}, I_{IS} = 50\text{ mA}$	3.0	–	0.002	–	Ω
R_{SH}	Shunt Resistance		3.6	–	125	200	Ω

DATA SWITCH (HDP/HDN $\leftrightarrow$ D+/D–)

R_{ON}	ON-Resistance	$V_{IS} = 0\text{ V to } 1.7\text{ V}, I_{IS} = 15\text{ mA}$	3.0	–	5	7.5	Ω
ΔR_{ON}	ON-Resistance Matching Between Channels	$V_{IS} = 0\text{ V to } 1.7\text{ V}, I_{IS} = 15\text{ mA}$	3.0	–	0.02	–	Ω
$R_{FLAT(ON)}$	ON Resistance Flatness	$V_{IS} = 0\text{ V to } 1.7\text{ V}, I_{IS} = 15\text{ mA}$	3.0	–	0.003	–	Ω
$I_{SW(OFF)}$	OFF-State Leakage	$V_{IS} = 0\text{ V to } 3.6$	3.6	–	–	200	nA
$I_{SW(ON)}$	ON-State Leakage	$V_{IS} = 0\text{ V to } 3.6$	3.6	–	–	± 200	nA

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AC ELECTRICAL CHARACTERISTICS (Typical values are at $V_{CC} = +3.6\text{ V}$ and $T_A = +25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test Conditions	V _{CC} (V)	–40 °C to 85 °C			Unit
				Min	Typ	Max	
AUDIO SWITCH (AUDP/AUDN ↔ D+/D–)							
THD	Audio THD	f = 20 Hz to 20 kHz, V _{IS} = 0.4 V _{RMS} , DC Bias = 0 V, R _L = 16 Ω	2.7 – 5.5	–	0.002	–	%
PSRR	Power Supply Ripple Rejection	From V _{CC} unto AUDP/AUDN, f = 217 Hz, R _L = 16 Ω	2.7 – 5.5	–	118	–	dB
DATA SWITCH (HDP/HDN ↔ D+/D–)							
C _{ON}	Equivalent ON–Capacitance	Switch ON, f = 1 MHz	3.6	–	4.84	–	pF
C _{OFF}	Equivalent OFF–Capacitance	Switch OFF, f = 1 MHz	3.6	–	2.06	–	pF
D _{IL}	Differential Insertion Loss	f = 10 MHz	2.7 – 5.5	–	–0.42	–	dB
		f = 800 MHz	2.7 – 5.5	–	–1.89	–	
		f = 1.1 GHz	2.7 – 5.5	–	–3.01	–	
D _{ISO}	Differential Off–Isolation	f = 10 MHz	2.7 – 5.5	–	–60	–	dB
		f = 800 MHz	2.7 – 5.5	–	–15	–	
		f = 1.1 GHz	2.7 – 5.5	–	–15	–	
D _{CTK}	Differential Crosstalk	f = 10 MHz	2.7 – 5.5	–	–67	–	dB
		f = 800 MHz	2.7 – 5.5	–	–23	–	
		f = 1.1 GHz	2.7 – 5.5	–	–19	–	
PSRR	Power Supply Ripple Rejection	From V _{CC} unto D+/D–, f = 217 Hz, R _L = 50 Ω	2.7 – 5.5	–	108	–	dB
DYNAMIC TIMING							
t _{PD}	Propagation Delay (Notes 5 and 6)	V _{NOH} or V _{NOL} = 0V, R _L = 50 Ω,	2.7 – 5.5	–	0.25	–	ns
t _{ON}	Turn–On Time	V _{IS} = 1 V, R _L = 50 Ω, C _L = 7 pF (fix- ture only)	2.7 – 5.5				μs
		EN or SEL to AUDP/AUDN		–	2.2	–	
		EN or SEL to HDP/HDN		–	6.2	–	
t _{OFF}	Turn–Off Time	V _{IS} = 1 V, R _L = 50 Ω, C _L = 7 pF (fix- ture only)	2.7 – 5.5				ns
		EN or SEL to AUDP/AUDN		–	67	–	
		EN or SEL to HDP/HDN		–	1200	–	
t _{sk(b–b)}	Bit to bit skew	Within the same differential channel	2.7 – 5.5	–	5	–	ps
t _{sk(ch–ch)}	Channel to channel skew	Maximum skew between all chan- nels	2.7 – 5.5	–	5	–	ps

5. Guaranteed by design.

6. No other delays than the RC network formed by the load resistance and the load capacitance of the switch are added on the bus. For a 10 pF load, this delay is 5 ns which is much smaller than rise and fall time of typical driving systems. Propagation delays on the bus are determined by the driving circuit on the driving side and its interactions with the load of the driven side.

PARAMETER MEASUREMENT INFORMATION

VNA Source
Balanced Port 1

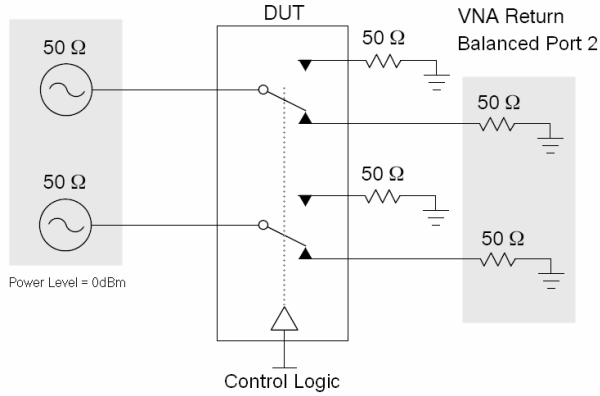


Figure 3. Differential Insertion Loss (S_{DD21})

VNA Source
Balanced Port 1

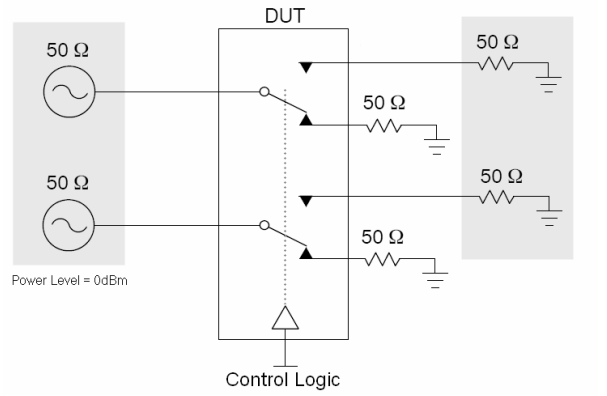


Figure 4. Differential Off Isolation (S_{DD21})

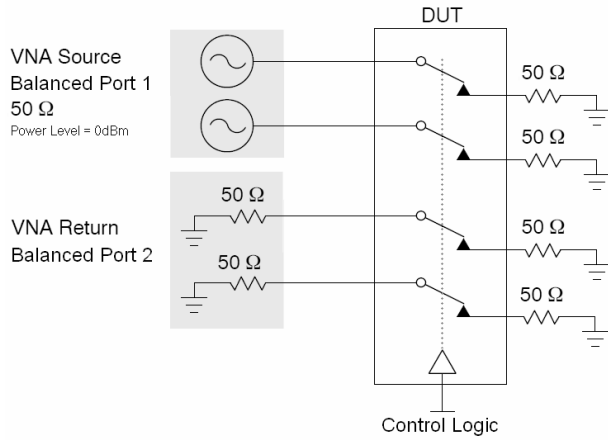


Figure 5. Differential Crosstalk (S_{DD21})

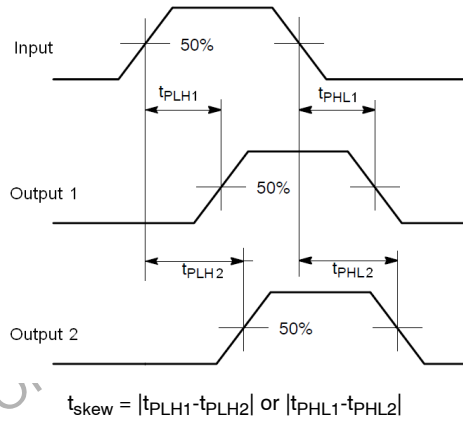


Figure 6. Bit-to-Bit and Channel-to-Channel Skew

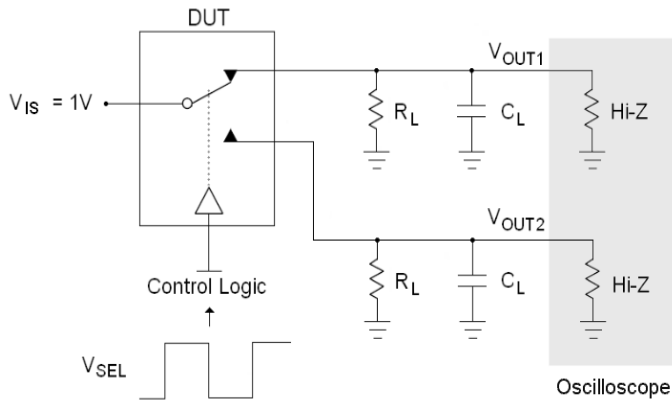


Figure 7. t_{ON} and t_{OFF}

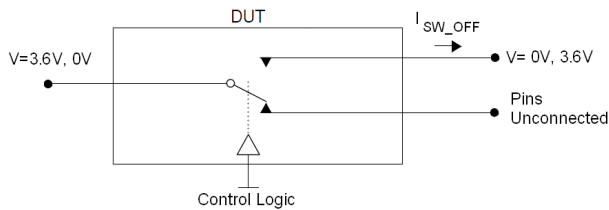
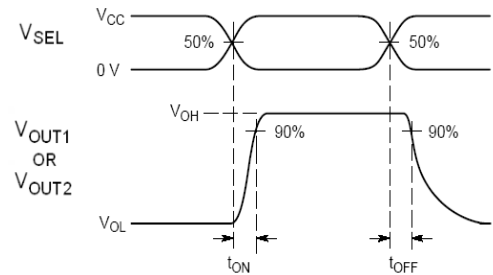


Figure 8. Off State Leakage

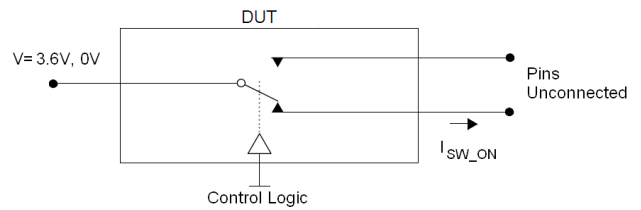


Figure 9. On State Leakage

TYPICAL OPERATING CHARACTERISTICS

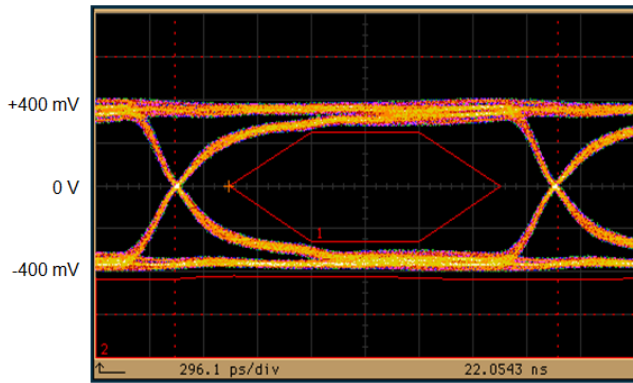


Figure 10. USB 2.0 High Speed Eye Diagram

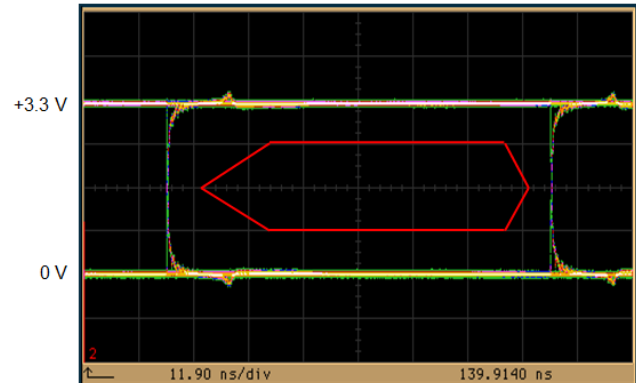


Figure 11. USB 1.1 Full Speed Eye Diagram

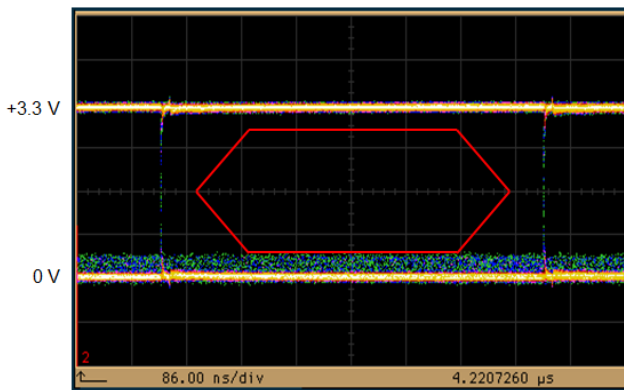


Figure 12. USB 1.0 Low Speed Eye Diagram

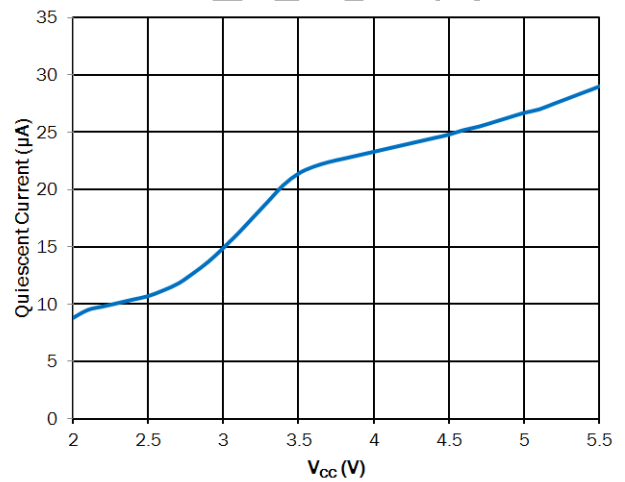


Figure 13. Product Supply Current

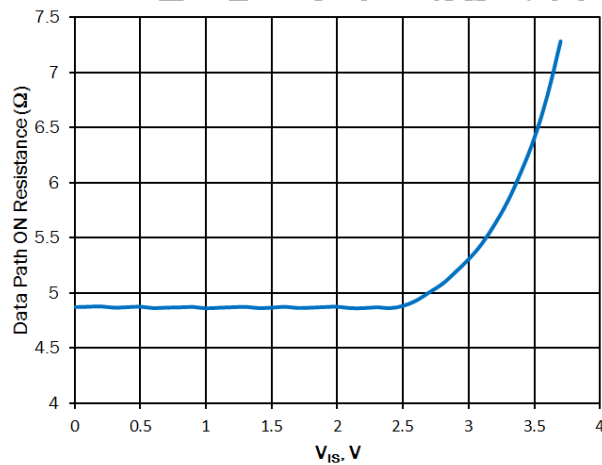


Figure 14. Data Path On Resistance

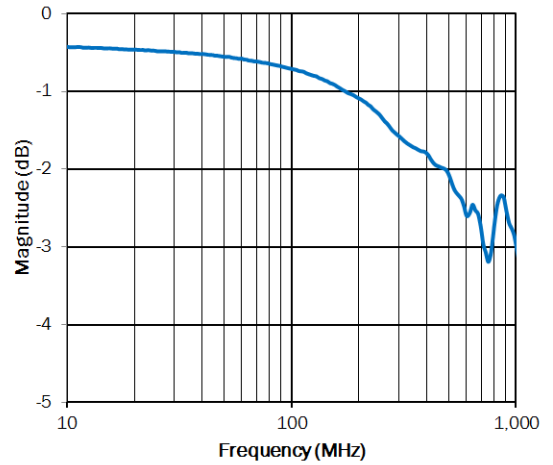


Figure 15. Data Switch Differential Insertion Loss

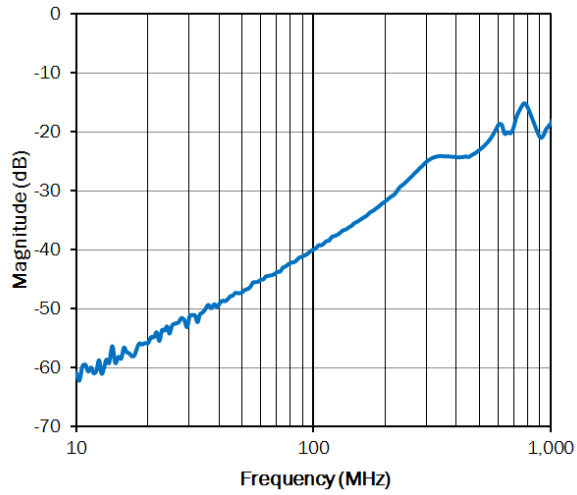


Figure 16. Data Switch Differential Off-Isolation

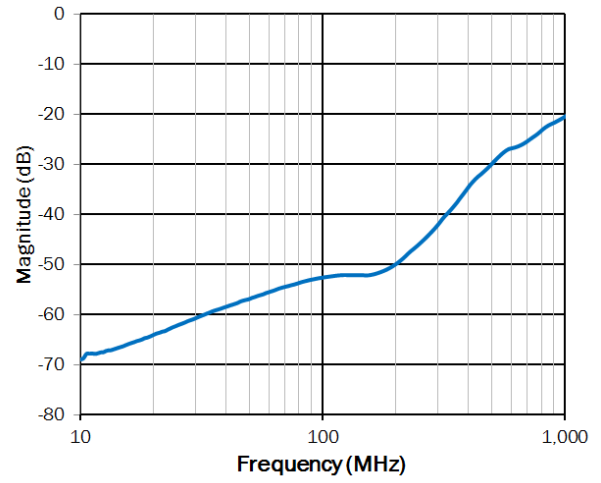


Figure 17. Data Switch Differential Crosstalk

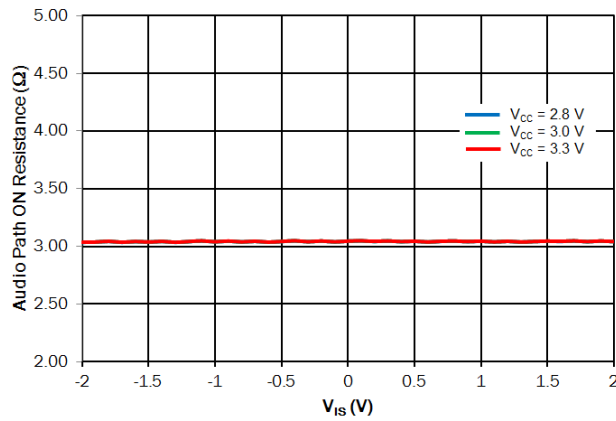


Figure 18. Audio Path On Resistance

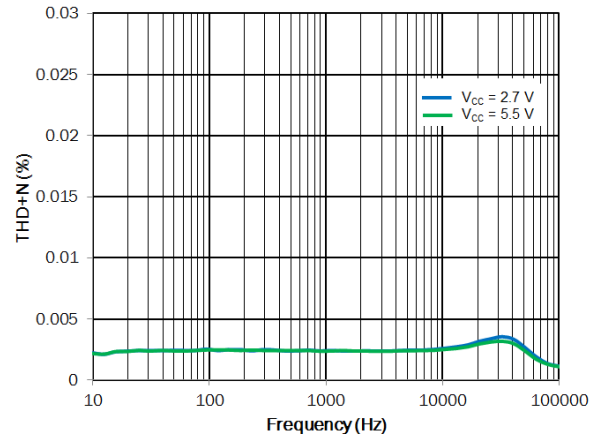
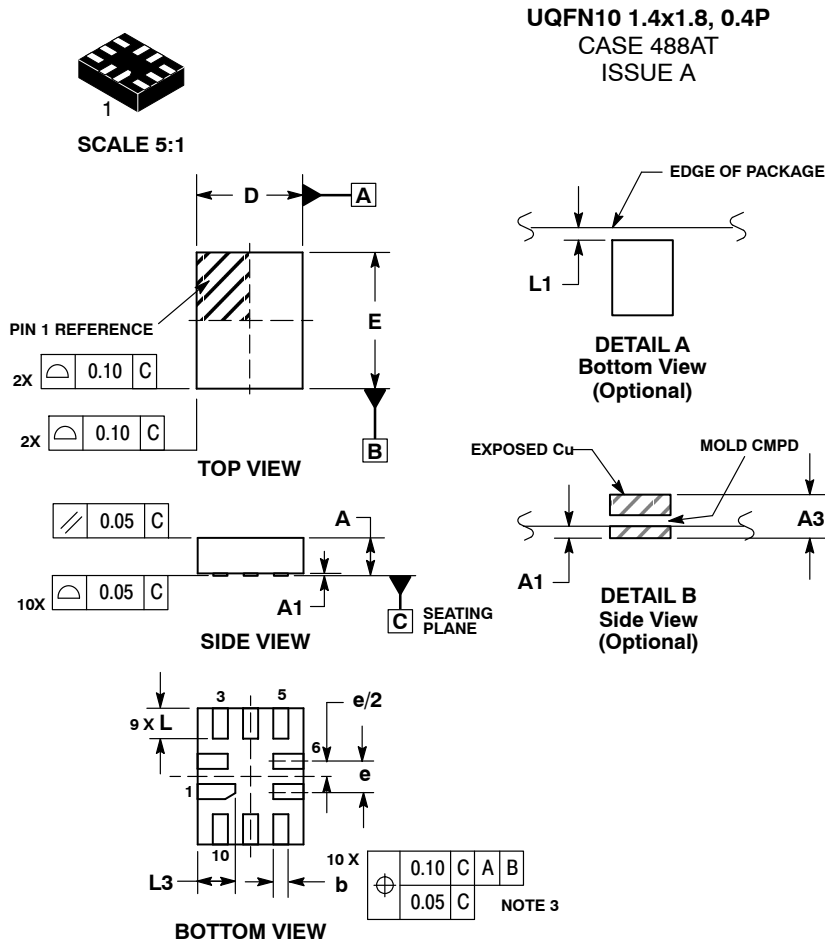
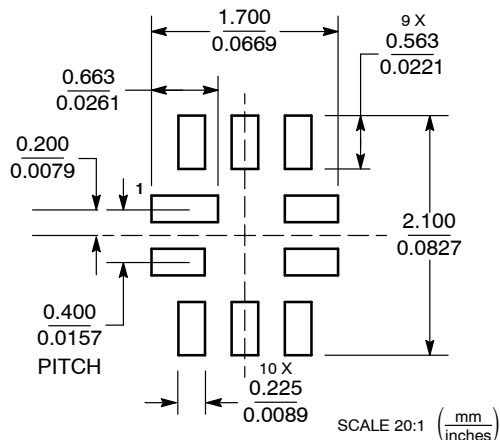


Figure 19. Audio THD



MOUNTING FOOTPRINT



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DESCRIPTION:	10 PIN UQFN, 1.4 X 1.8, 0.4P	PAGE 1 OF 1

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