Single Chip 12-Bit Data Acquisition System

FEATURES

- Software Programmable Features
  - Unipolar/Bipolar Conversion
  - Differential/Single Ended Inputs
  - MSB-First or MSB/LSB Data Sequence
  - Power Shutdown
- Built-In Sample and Hold
- Single Supply 5V or ±5V Operation
- Direct 4-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 46.5kHz Maximum Throughput Rate
- System Shutdown Output (LTC1296)

KEY SPECIFICATIONS

- Resolution: 12 Bits
- Fast Conversion Time: 12µs Max Over Temp
- Low Supply Current: 6.0mA

DESCRIPTION

The LTC1293/4/6 is a family of data acquisition systems which contain a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform either 12-bit unipolar, or 11-bit plus sign bipolar A/D conversions. The input multiplexer can be configured for either single ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single ended input channels. When the LTC1293/4/6 is idle it can be powered down in applications where low power consumption is desired. The LTC1296 includes a System Shutdown Output pin which can be used to power down external circuitry, such as signal conditioning circuitry prior to the input mux.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing up to eight channels of data to be transmitted over as few as three wires.

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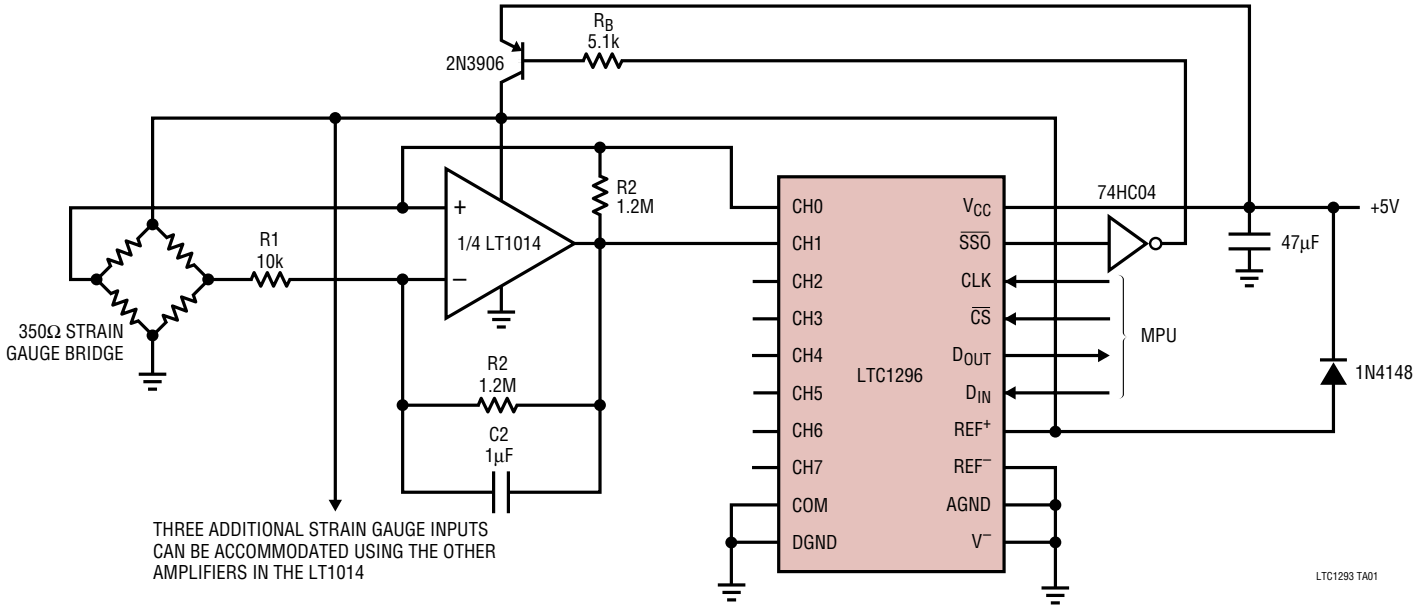
TYPICAL APPLICATION

12-Bit Data Acquisition System with Power Shutdown

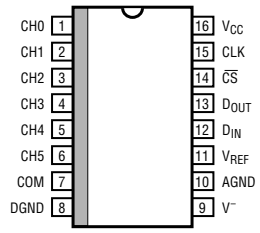


ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Negative Supply Voltage (V^-) ..... –6V to GND
Voltage
  Analog and Reference
    Inputs ..... (V^-) –0.3V to V_{CC} + 0.3V
  Digital Inputs .....–0.3V to 12V
  Digital Outputs ..... –0.3V to V_{CC} + 0.3V

Power Dissipation 500mW
Operating Temperature Range
  LTC1293/4/6BC, LTC1293/4/6CC,
  LTC1293/4/6DC ..... 0°C to 70°C
  LTC1296BI, LTC1296CI, LTC1296DI ... –40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

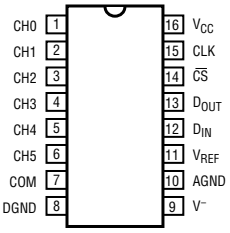
PACKAGE/ORDER INFORMATION (Top Views) Consult factory for Industrial and Military grades.



SW PACKAGE, 16-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

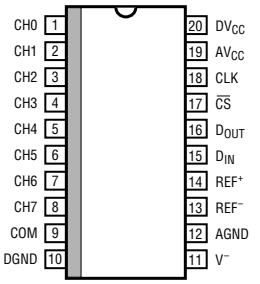
LTC1293BCSW
LTC1293CCSW
LTC1293DCSW



N PACKAGE, 16-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)

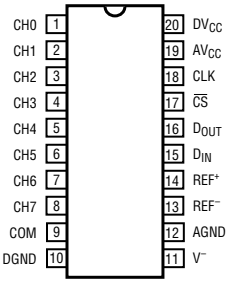
ORDER PART NUMBER

LTC1293BCN
LTC1293CCN
LTC1293DCN



SW PACKAGE, 20-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 150°C/W

LTC1294BCSW
LTC1294CCSW
LTC1294DCSW

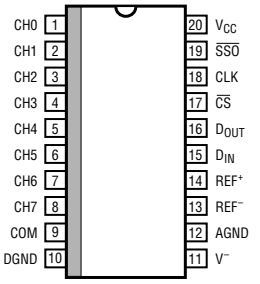


N PACKAGE, 20-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)

LTC1294BCN
LTC1294CCN
LTC1294DCN

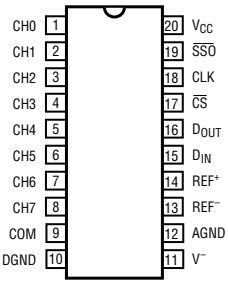
J PACKAGE, 20-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (J)
OBSOLETE PACKAGE
Consider the N Package for Alternate Source

LTC1294BCJ
LTC1294CCJ
LTC1294DCJ



SW PACKAGE, 20-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 150°C/W

LTC1296BCSW
LTC1296CCSW
LTC1296DCSW
LTC1296BISW
LTC1296CISW
LTC1296DISW



N PACKAGE, 20-LEAD PDIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W (N)

LTC1296BIN
LTC1296CIN
LTC1296DIN
LTC1296BCN
LTC1296CCN
LTC1296DCN

J PACKAGE, 20-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (J)
OBSOLETE PACKAGE
Consider the N Package for Alternate Source

LTC1296BCJ
LTC1296CCJ
LTC1296DCJ

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1293/4/6B MIN	LTC1293/4/6B TYP	LTC1293/4/6B MAX	LTC1293/4/6C MIN	LTC1293/4/6C TYP	LTC1293/4/6C MAX	LTC1293/4/6D MIN	LTC1293/4/6D TYP	LTC1293/4/6D MAX	UNITS
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Notes 4, 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±0.5			±1.0			±4.0	LSB
Minimum Resolution for which No Missing Codes are Guaranteed		●			12			12			12	Bits
Analog and REF Input Range	(Note 7)				(V^-)–0.05V to V_{CC} + 0.05V							V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1293/4/6B LTC1293/4/6C LTC1293/4/6D MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		0.1		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			2.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		21 CLK +500ns			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDI}	Hold Time, D_{IN} after CLK↑	V_{CC} = 5V (Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid After CLK↓				130		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)		300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)		400			ns
t_{suDI}	Set-up Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{su\overline{CS}}$	Set-up Time, $\overline{CS}$↓ before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{wH\overline{CS}}$	CS High Time During Conversion	V_{CC} = 5V (Note 6)		500			ns
$t_{wL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)		21			CLK Cycles
$t_{en\overline{SSO}}$	Delay Time, CLK↓ to $\overline{SSO}$↓	See Test Circuits	●		750	1500	ns
$t_{dis\overline{SSO}}$	Delay Time, $\overline{CS}$↓ to $\overline{SSO}$↑	See Test Circuits	●		250	500	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS			LTC1293/4/6B LTC1293/4/6C LTC1293/4/6D MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V		●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V		●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$		●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V		●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10mA I_O = 360µA		 ●	 2.4	4.7 4.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA		●			0.4	V
I_{OZ}	High Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High		● ●			3 –3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				–20		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$				20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High		●		6	12	mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High, Power Shutdown	LTC1294BC, LTC1294CC, LTC1294DC, LTC1294BI, LTC1294CI, LTC1294DI,	●		5	10	µA
		CLK Off	LTC1294BM, LTC1294CM, LTC1294DM	●		5	15	µA
I_{REF}	Reference Current	$\overline{CS}$ High		●		10	50	µA
I^-	Negative Supply Current	$\overline{CS}$ High		●		1	50	µA
$I_{SOURCEs}$	$\overline{SSO}$ Source Current	$V_{\overline{SSO}}$ = 0V		●	0.8	1.5		mA
I_{SINKs}	$\overline{SSO}$ Sink Current	$V_{\overline{SSO}} = V_{CC}$		●	0.5	1.0		mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to DGND, AGND and REF^- wired together (unless otherwise noted).

Note 3: V_{CC} = 5V, V_{REF+} = 5V, V_{REF-} = 0V, V^- = 0V for unipolar mode and –5V for bipolar mode, CLK = 1.0MHz unless otherwise specified. The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 4096. For example, when V_{REF} = 5V, 1LSB (bipolar) = 2 (5V)/4096 = 2.44mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

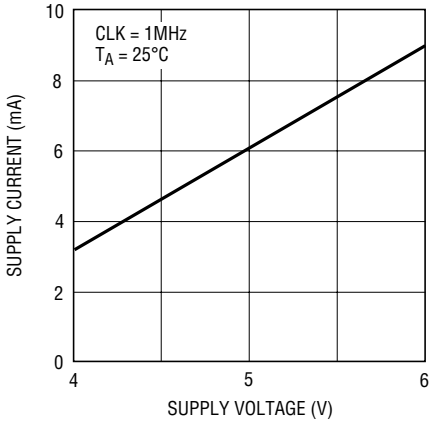
Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

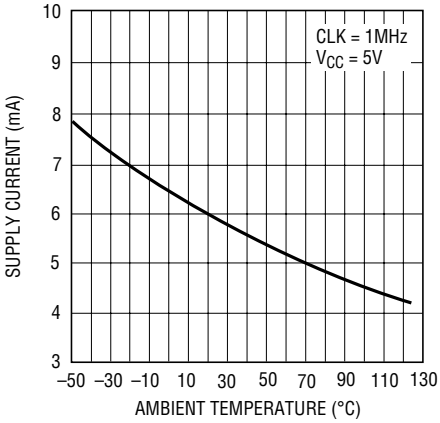
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



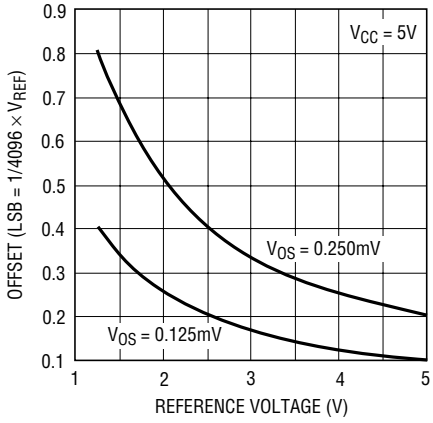
LTC1293 G01

Supply Current vs Temperature



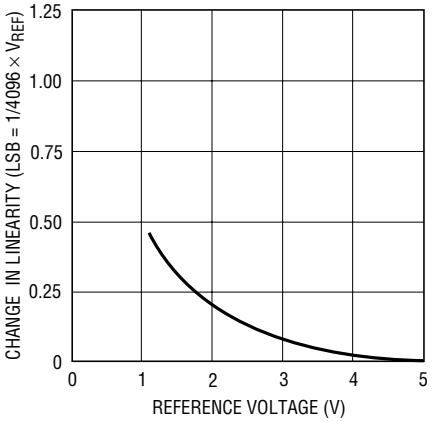
LTC1293 G02

Unadjusted Offset Voltage vs Reference Voltage



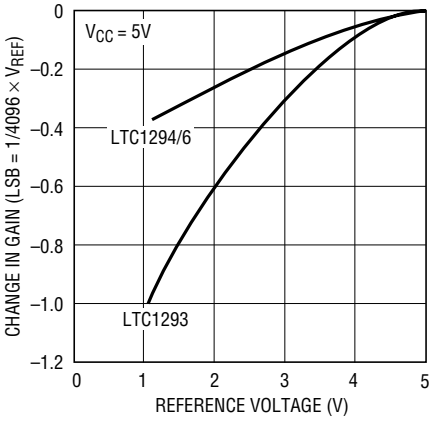
LTC1293 G03

Change in Linearity vs Reference Voltage



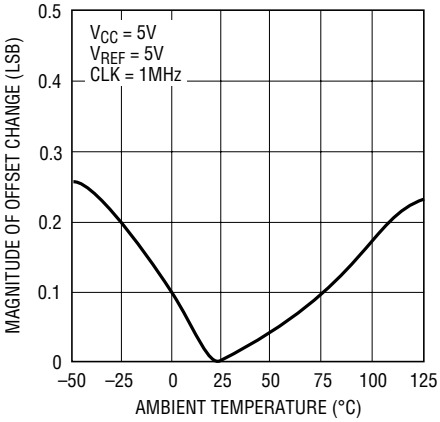
LTC1293 G04

Change in Gain vs Reference Voltage



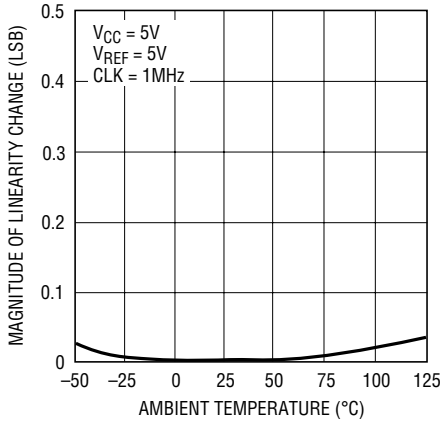
LTC1293 G05

Change in Offset vs Temperature



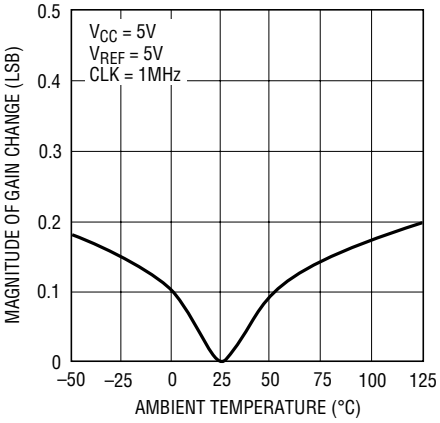
LTC1293 G06

Change in Linearity vs Temperature



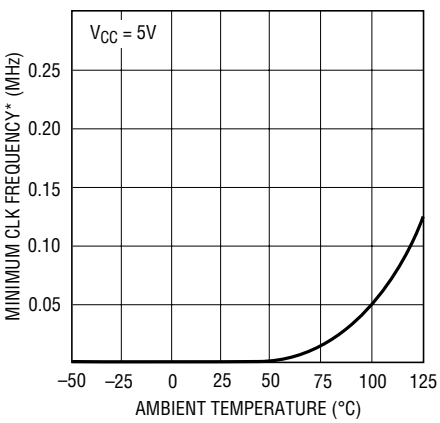
LTC1293 G07

Change in Gain vs Temperature



LTC1293 G08

Minimum Clock Rate for 0.1LSB Error

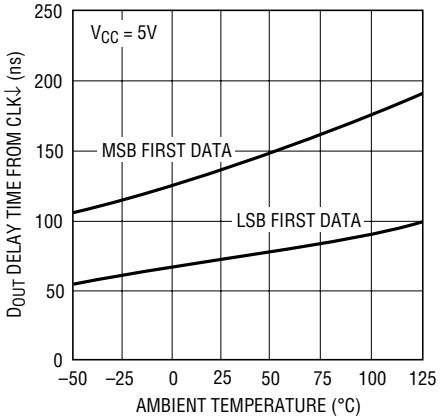


LTC1293 G09

* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

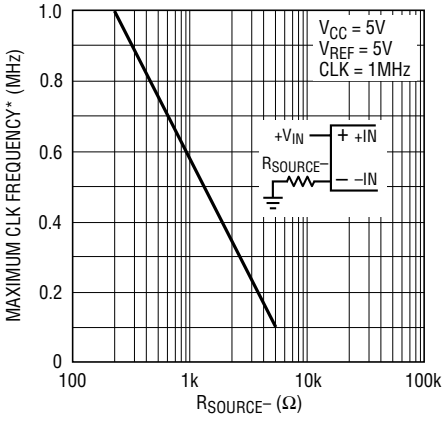
TYPICAL PERFORMANCE CHARACTERISTICS

D_{OUT} Delay Time vs Temperature



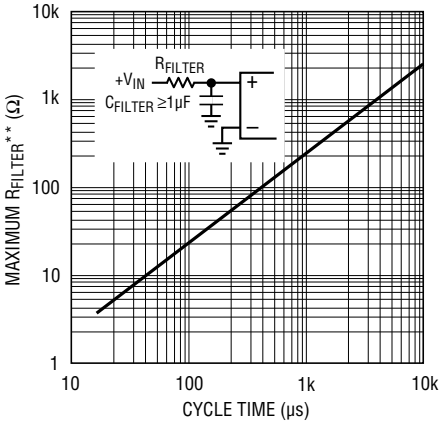
LTC1293 G10

Maximum Clock Rate vs Source Resistance



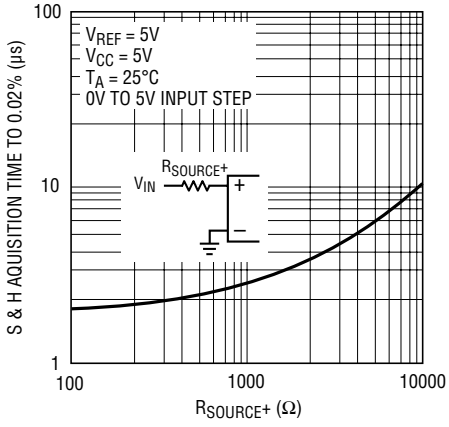
LTC1293 G11

Maximum Filter Resistor vs Cycle Time



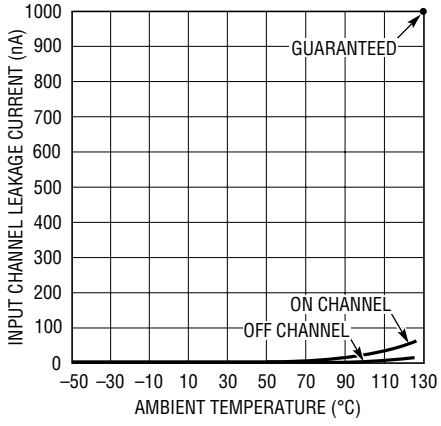
LTC1293 G12

Sample and Hold Acquisition Time vs Source Resistance



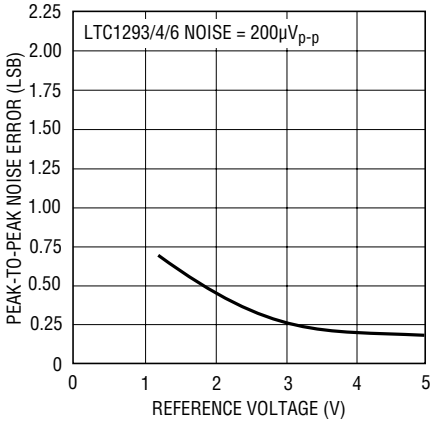
LTC1292 G13

Input Channel leakage Current vs Temperature



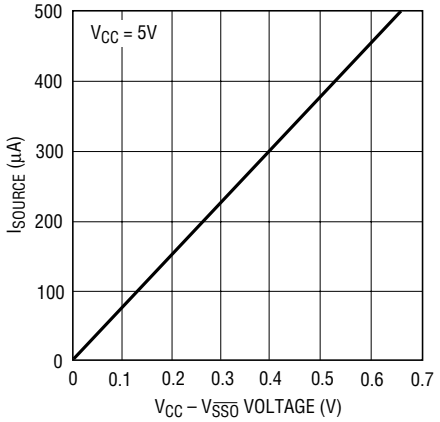
LTC1293 G14

Noise Error vs Reference Voltage



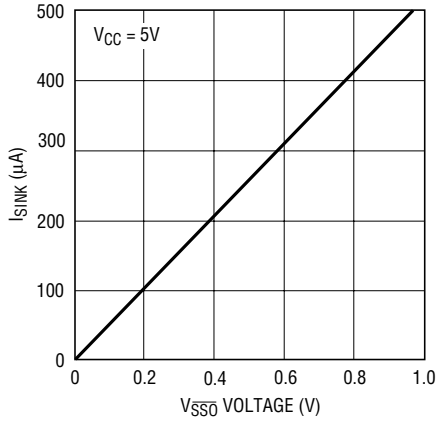
LTC1293 G15

LTC1296 $\overline{SSO}$ Source Current vs $V_{CC} - V_{\overline{SSO}}$



LTC1293 G16

LTC1296 $\overline{SSO}$ Sink Current vs $V_{\overline{SSO}}$



LTC1293 G17

* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT $R_{FILTER} = 0\Omega$ IS FIRST DETECTED.

PIN FUNCTIONS

LTC1293

#	PIN	FUNCTION	DESCRIPTION
1 – 6	CH0 – CH5	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
7	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
8	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
9	V^-	Negative Supply	Tie V^- to most negative potential in the circuit (Ground in single supply applications).
10	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
11	V_{REF}	Ref. Input	The reference inputs must be kept free of noise with respect to AGND.
12	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
13	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
14	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
15	CLK	Clock	This clock synchronizes the serial data transfer and controls A/D conversion rate.
16	V_{CC}	Positive supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

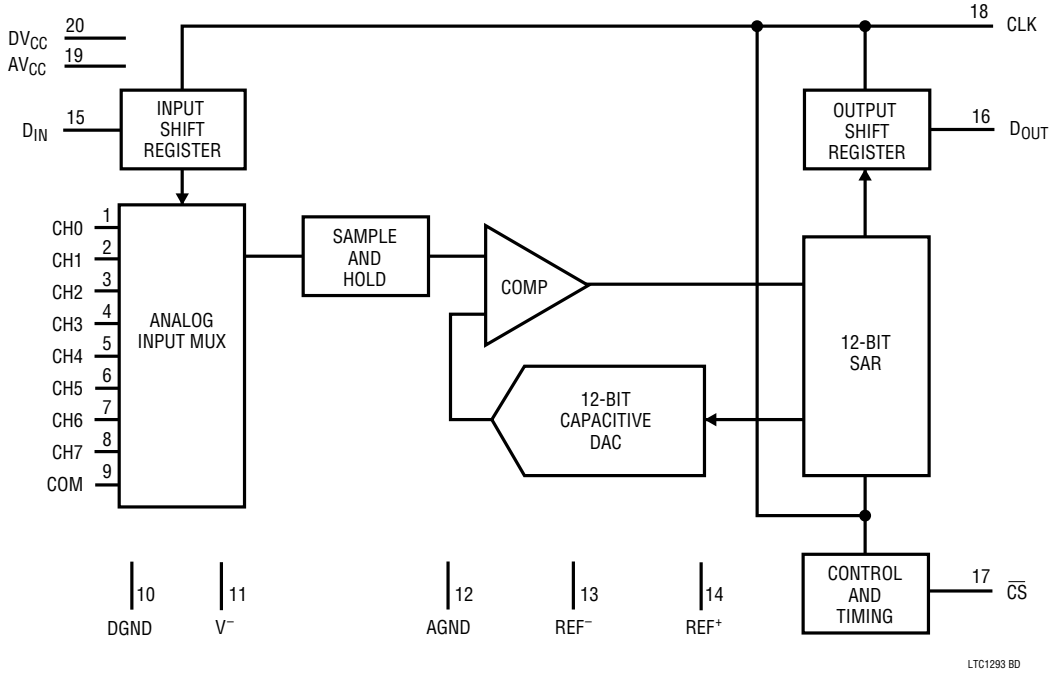
LTC1294

#	PIN	FUNCTION	DESCRIPTION
1 –8	CH0 – CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	V^-	Negative Supply	Tie V^- to most negative potential in the circuit (Ground in single supply applications).
12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
13, 14	REF^-, REF^+	Ref. Inputs	The reference inputs must be kept free of noise with respect to AGND. The A/D sees a reference voltage equal to the difference between REF^+ and REF^-.
15	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
18	CLK	Clock	This clock synchronizes the serial data transfer and controls A/D converion rate.
19, 20	AV_{CC}, DV_{CC}	Positive Supplies	These supplies must be kept free of noise and ripple by bypassing directly to the analog ground plane. AV_{CC} and DV_{CC} must be tied together.

LTC1296

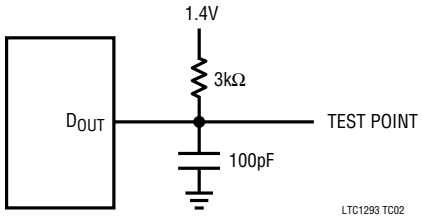
#	PIN	FUNCTION	DESCRIPTION
1 –8	CH0 – CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	V^-	Negative Supply	Tie V^- to most negative potential in the circuit (Ground in single supply applications).
12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
13, 14	REF^-, REF^+	Ref. Inputs	The reference inputs must be kept free of noise with respect to AGND. The A/D sees a reference voltage equal to the difference between REF^+ and REF^-.
15	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
18	CLK	Clock	This clock synchronizes the serial data transfer and controls A/D conversion rate.
19	$\overline{SSO}$	System Shutdown Output	System Shutdown Output pin will go low when power shutdown is requested.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM (Pin numbers refer to LTC1294)

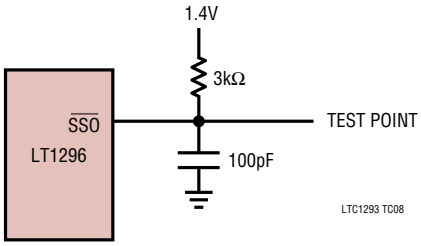


TEST CIRCUITS

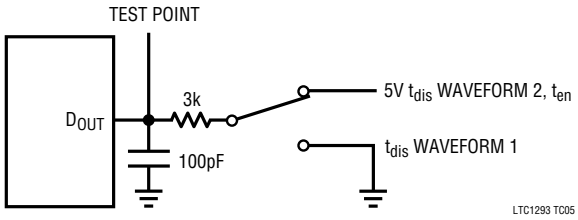
Load Circuit for t_{dDO}, t_r and t_f



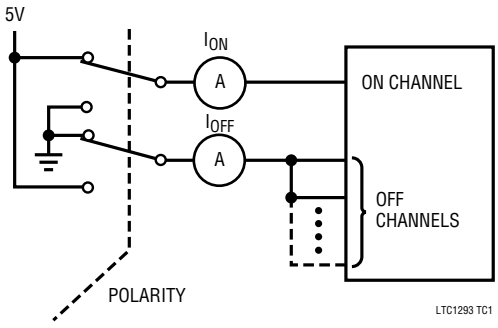
Load Circuit for t_{enSSO} and $t_{dis\overline{SSO}}$



Load Circuit for t_{dis} and t_{en}

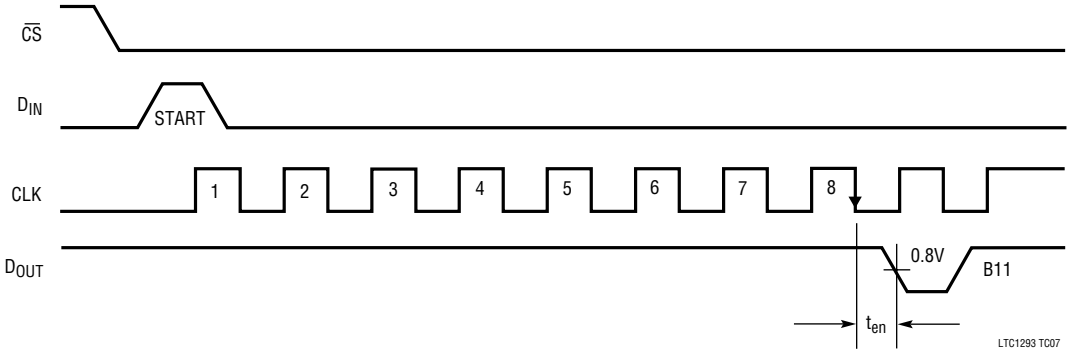


On and Off Channel Leakage Current

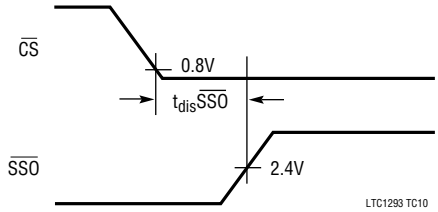


TEST CIRCUITS

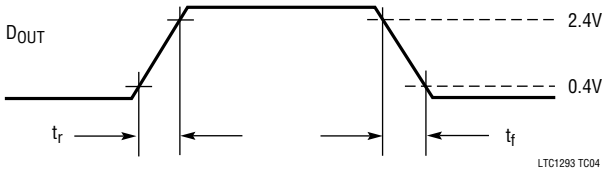
Voltage Waveforms for t_{en}



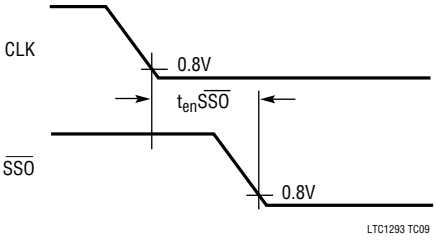
Voltage Waveform for $t_{dis\overline{SSO}}$



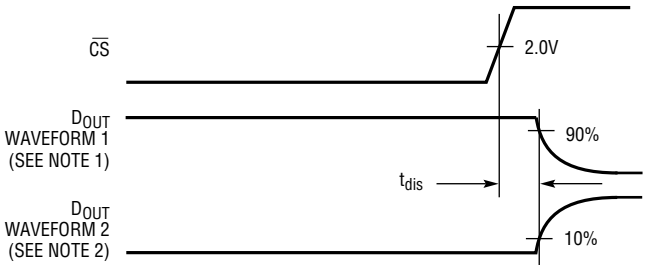
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveform for for $t_{en\overline{SSO}}$



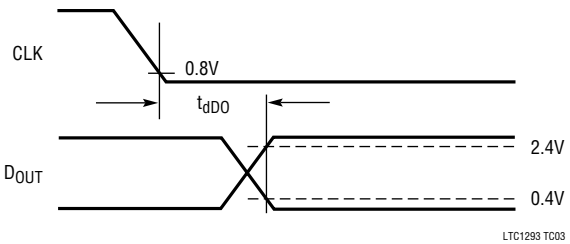
Voltage Waveform for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1293 TC06

Voltage Waveform for D_{OUT} Delay Time, t_{dDO}



APPLICATIONS INFORMATION

The LTC 1293/4/6 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

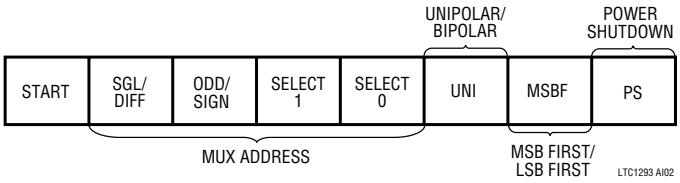
DIGITAL CONSIDERATIONS

Serial Interface

The LTC1293/4/6 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The input data is first received and then the A/D conversion result is transmitted (half duplex). Because of the half duplex operation D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wired: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}). Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1293/4/6 looks for a start bit. After the start bit is received a 7-bit input word is shifted into the D_{IN} input which configures the LTC1293/4/6 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. With the half duplex serial interface the D_{OUT} data is from the current conversion. After the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1293/4/6 in preparation for the next data exchange.

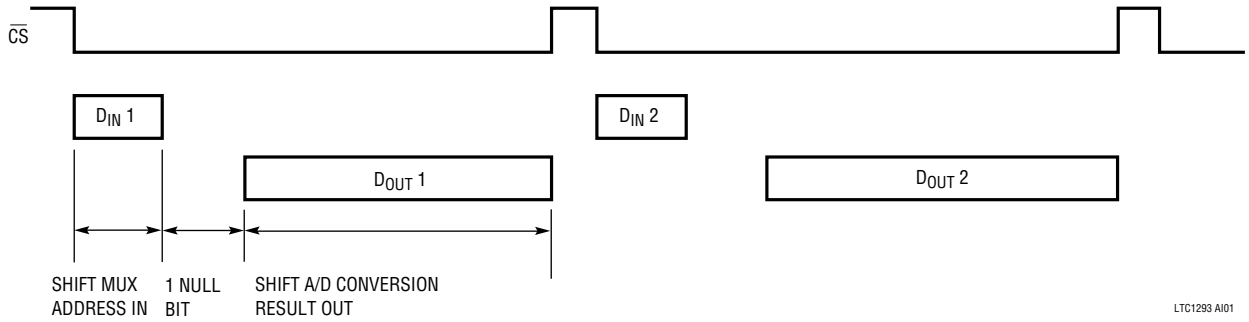
INPUT DATA WORD

The LTC1293/4/6 seven-bit data word is clocked into the D_{IN} input on the rising edge of the clock after chip select goes low and the start bit has been recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeroes which precede this logical one will be ignored. After the start bit is received the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.



MUX Address

The four bits of the input word following the START BIT assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following table. Note that in differential mode (SGL/DIFF = 0) measurements are limited to four adjacent input pairs with either polarity. In single ended mode, all input channels are measured with respect to COM. Only the +inputs have sample and holds. Signals applied at the –inputs must not change more than the required accuracy during the conversion.

APPLICATIONS INFORMATION

Table 1a. LTC1294/6 Multiplexer Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS			SINGLE-ENDED CHANNEL SELECTION							
SGL/ DIFF	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	SGL/ DIFF	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	COM
0	0	0 0	+	–							1	0	0 0	+								–
0	0	0 1			+	–					1	0	0 1			+						–
0	0	1 0					+	–			1	0	1 0					+				–
0	0	1 1							+	–	1	0	1 1							+		–
0	1	0 0	–	+							1	1	0 0		+							–
0	1	0 1			–	+					1	1	0 1				+					–
0	1	1 0					–	+			1	1	1 0						+			–
0	1	1 1							–	+	1	1	1 1								+	–

Table 1b. LTC1293 Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION						MUX ADDRESS			SINGLE-ENDED CHANNEL SELECTION						
SGL/ DIFF	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	SGL/ DIFF	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	COM
0	0	0 0	+	–					1	0	0 0	+						–
0	0	0 1			+	–			1	0	0 1			+				–
0	0	1 0					+	–	1	0	1 0					+		–
0	0	1 1	Not Used						1	0	1 1	Not Used						
0	1	0 0	–	+					1	1	0 0		+					–
0	1	0 1			–	+			1	1	0 1				+			–
0	1	1 0					–	+	1	1	1 0						+	–
0	1	1 1	Not Used						1	1	1 1	Not Used						

Unipolar/Bipolar (UNI)

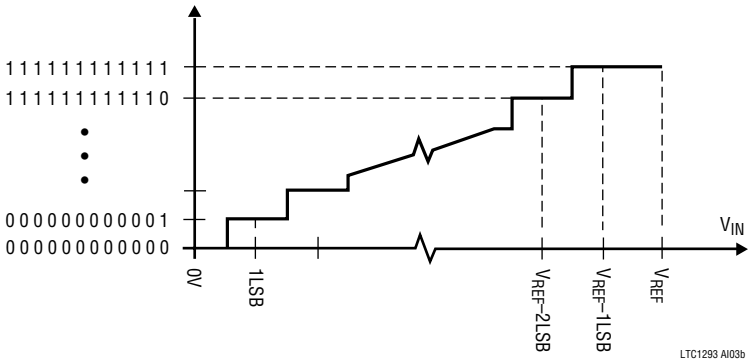
The UNI bit determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below:

Unipolar Transfer Curve (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (VREF = 5V)
1 1 1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	4.9988V
1 1 1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	4.9976V
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 0 0 1	1LSB	0.0012V
0 0 0 0 0 0 0 0 0 0 0 0	0V	0V

LTC1293 AI03a

Unipolar Output Code (UNI = 1)



LTC1293 AI03b

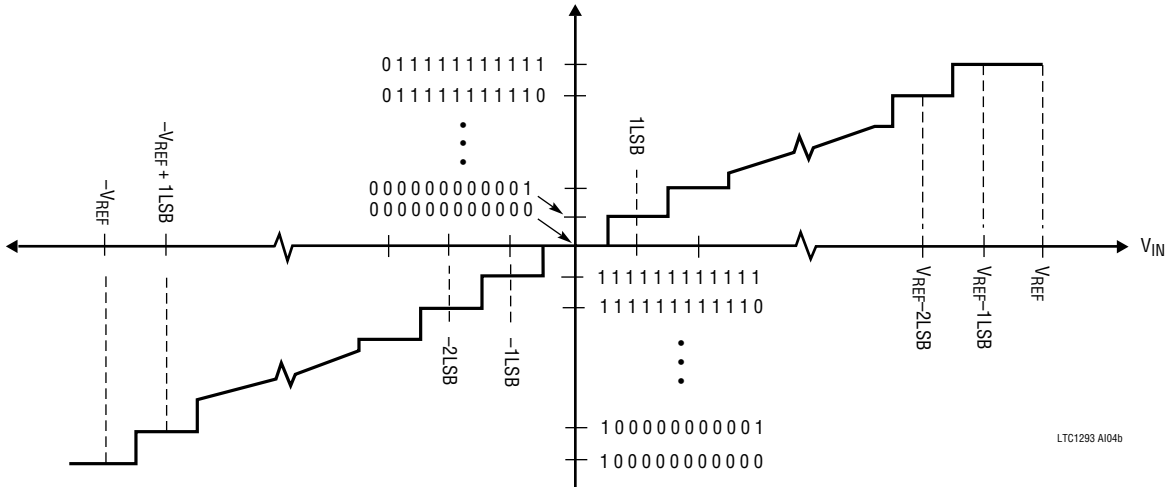
APPLICATIONS INFORMATION

Bipolar Transfer Curve (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)	OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
0 1 1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	4.9976V	1 1 1 1 1 1 1 1 1 1 1 1	–1LSB	–0.0024V
0 1 1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	4.9851V	1 1 1 1 1 1 1 1 1 1 1 0	–2LSB	–0.0048V
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
0 0 0 0 0 0 0 0 0 0 0 1	1LSB	0.0024V	1 0 0 0 0 0 0 0 0 0 0 1	$-(V_{REF})$ + 1LSB	–4.9976V
0 0 0 0 0 0 0 0 0 0 0 0	0V	0V	1 0 0 0 0 0 0 0 0 0 0 0	$-(V_{REF})$	–5.00000V

LTC1293 AI04a

Bipolar Output Code (UNI = 0)



The following discussion will demonstrate how the two reference pins are to be used in conjunction with the analog input multiplexer. In unipolar mode the input span of the A/D is set by the difference in voltage on the REF^+ pin and the REF^- pin. In the bipolar mode the input span is twice the difference in voltage on the REF^+ pin and the REF^- pin. In the unipolar mode the lower value of the input span is set by the voltage on the COM pin for single-ended inputs and by the voltage on the minus input pin for differential inputs. For the bipolar mode of operation the voltage on the COM pin or the minus input pin set the center of the input span.

The upper and lower value of the input span can now be summarized in the following table:

INPUT CONFIGURATION		UNIPOLAR MODE	BIPOLAR MODE
Single-Ended	Lower Value	COM	$-(REF^+ - REF^-) + COM$
	Upper Value	$(REF^+ - REF^-) + COM$	$(REF^+ - REF^-) + COM$
Differential	Lower Value	IN^-	$-(REF^+ - REF^-) + IN^-$
	Upper Value	$(REF^+ - REF^-) + IN^-$	$(REF^+ - REF^-) + IN^-$

The reference voltages REF^+ and REF^- can fall between V_{CC} and V^-, but the difference (REF^+ –REF^-) must be less than or equal to V_{CC}. The input voltages must be less than or equal to V_{CC} and greater than or equal to V^-. For the LTC1293 REF^- = 0V.

The following examples are for a single-ended input configuration.

Example 1: Let V_{CC} = 5V, V^- = 0V, REF^+ = 4V, REF^- = 1V and COM = 0V. Unipolar mode of operation. The resulting input span is $0V \le IN^+ \le 3V$.

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Example 2: The same conditions as Example 1 except COM = 1V. The resulting input span is $1V \le IN^+ \le 4V$. Note if $IN^+ \ge 4V$ the resulting D_{OUT} word is all 1's. If $IN^+ \le 1V$ then the resulting D_{OUT} word is all 0's.

Example 3: Let $V_{CC} = 5V$, $V^- = -5V$, $REF^+ = 4V$, $REF^- = 1V$ and COM = 1V. Bipolar mode of operation. The resulting input span is $-2V \le IN^+ \le 4V$.

For differential input configurations with the same conditions as in the above three examples the resulting input spans are as follows:

Example 1 (Diff.): $IN^- \le IN^+ \le IN^- + 3V$.
Example 2 (Diff.): $IN^- \le IN^+ \le IN^- + 3V$.
Example 3 (Diff.): $IN^- - 3V \le IN^+ \le IN^- + 3V$.

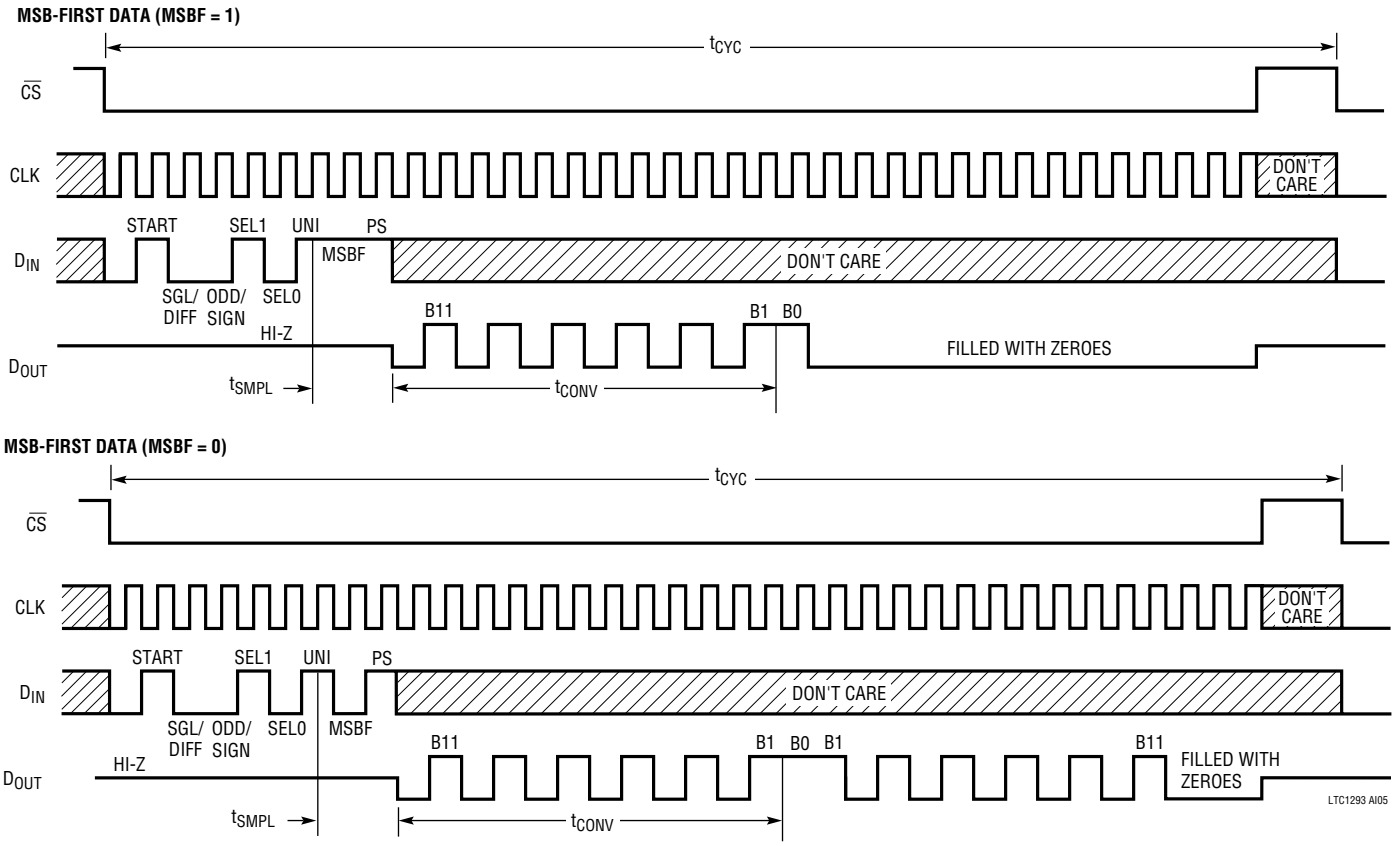
MSB-First/LSB-First (MSBF)

The output data of the LTC1293/4/6 is programmed for MSB-first or LSB-first sequence using the MSB bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeroes will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. In the bipolar mode the sign bit will fill in after the MSB bit for MSBF = 0 (see Operating Sequence).

Power Shutdowns (PS)

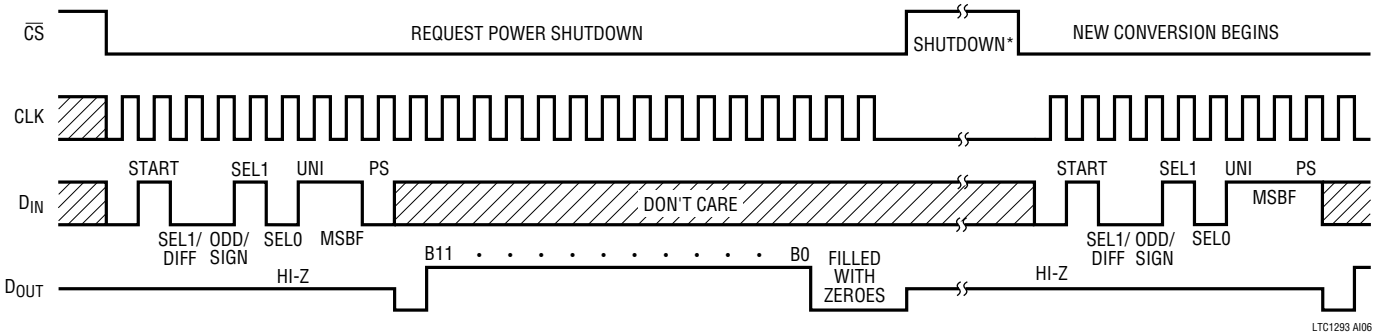
The power shutdown feature of the LTC1293/4/6 is activated by making the PS bit a logical zero. If $\overline{CS}$ remains low after the PS bit has been received, a 12-bit D_{OUT} word with

Operating Sequence
Example: Differential Inputs ($CH4^+$, $CH5^-$), Unipolar Mode



APPLICATIONS INFORMATION

Power Shutdown Operating Sequence
Example: Differential Inputs (CH4$^+$, CH5$^-$), Unipolar Mode and MSB-First Data



*STOPPING THE CLOCK WILL HELP REDUCE POWER CONSUMPTION.
$\overline{CS}$ CAN BE BROUGHT HIGH ONCE THE DIN WORD HAS BEEN CLOCKED IN.

all logical ones will be shifted out followed by logical zeroes till $\overline{CS}$ goes high. Then the D_{OUT} line will go into its high impedance state. The LTC 1293/4/6 will remain in the shutdown mode till the next $\overline{CS}$ cycle. There is no warm-up or wait period required after coming out of the power shutdown cycle so a conversion can commence after $\overline{CS}$ goes low (see Power Shutdown Operating Sequence). The LTC1296 has a System Shutdown Output pin ($\overline{SSO}$) which will go low when power shutdown is activated. The pin will stay low till next $\overline{CS}$ cycle.

Microprocessor Interfaces

The LTC1293/4/6 can interface directly (without external hardware) to most popular microprocessors (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1293/4/6. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Microprocessor Interfaces

The LTC1293/4/6 can interface directly (without external hardware) to most popular microprocessors (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1293/4/6.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1293/4/6**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

* Requires external hardware

** Contact factory for interface information for processors not on this list

† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

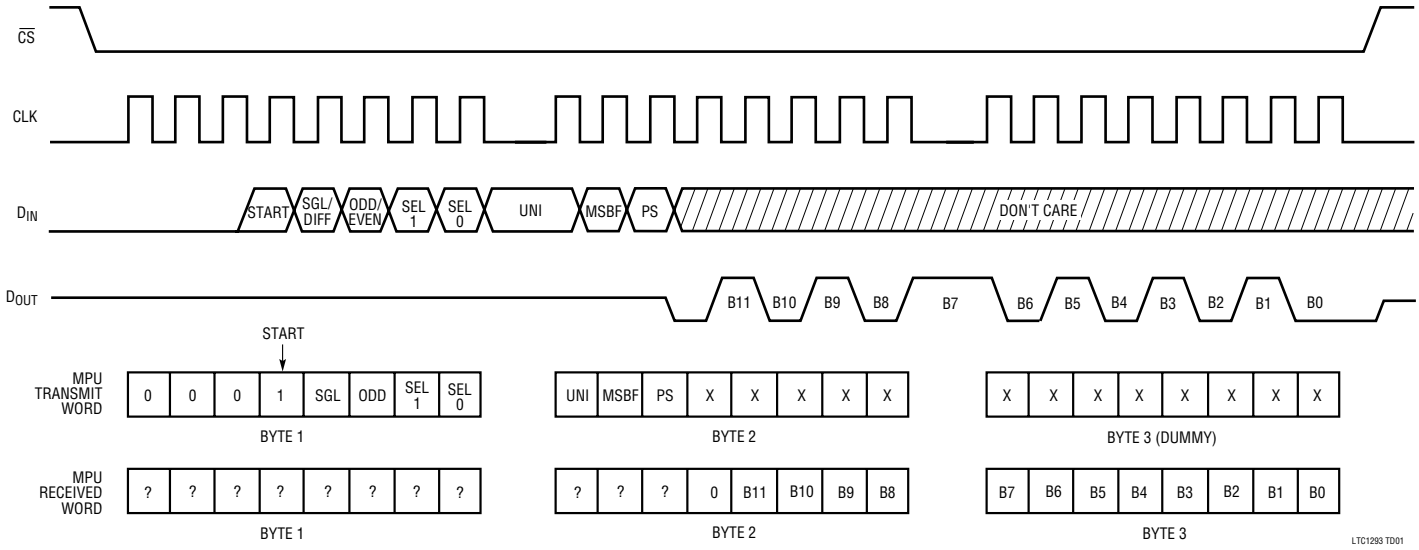
Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits B7 through B0 into the MPU. The data is right justified in the two memory locations. ANDing the second byte with $0D_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

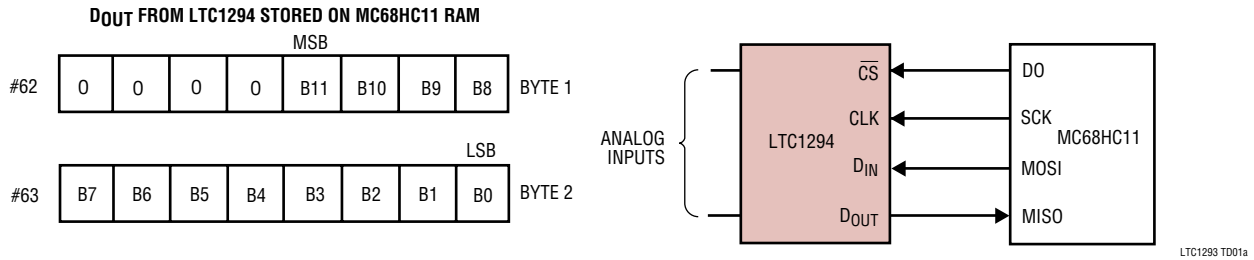
Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1293/4/6 and parallel port microprocessors. Usually the signals $\overline{CS}$, D_{IN} and CLK are generated on three port lines and the D_{OUT} signal is read on a fourth port line. This works very well. One can save a line by tying the D_{IN} and D_{OUT} lines together. The 8051 first sends the start bit and D_{IN} to the LTC1294 over the line connected to P1.2. Then P1.2 is reconfigured as an input and the 8051 reads back the 12-bit A/D result over the same data line.

Data Exchange Between LTC1294 and MC68HC11



Hardware and Software Interface to Motorola MC68HC11

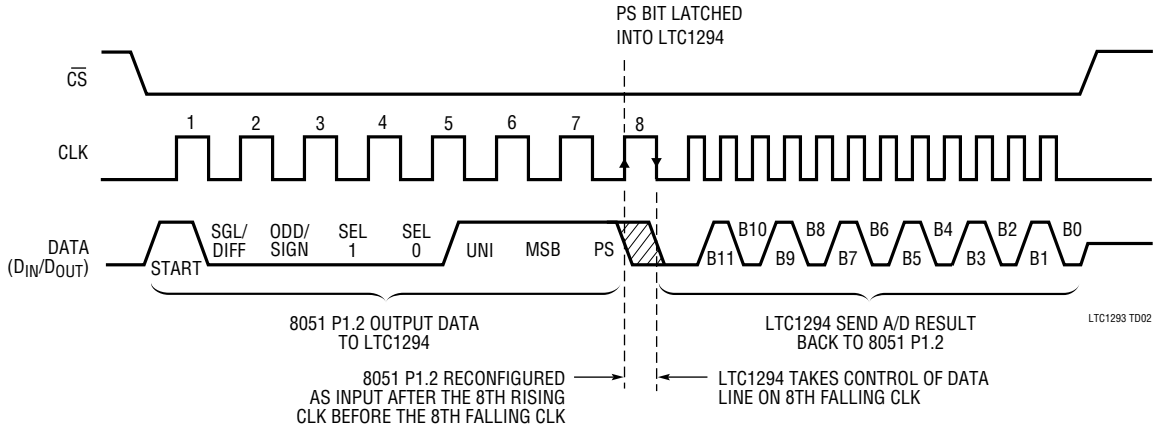


APPLICATIONS INFORMATION

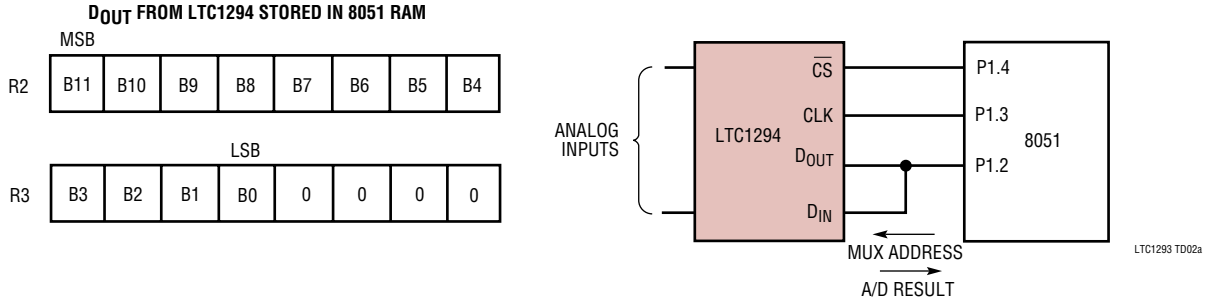
MC68HC11 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR		STAA	$102A	LOAD DIN INTO SPI, START SCK
	STAA	$1028	LOAD DATA INTO SPCR ($1028)	WAIT2	LDAA	$1029	CHECK SPI STATUS REG
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR		BPL	WAIT2	CHECK IF TRANSFER IS DONE
	STAA	$1009	LOAD DATA INTO PORT D DDR		LDAA	$102A	LOAD LTC1294 MSBs INTO ACC A
	LDAA	#$10	LOAD DIN WORD INTO ACC A		STAA	$62	STORE MSBs IN $62
	STAA	$50	LOAD DIN DATA INTO $50		LDAA	$52	LOAD DUMMY DIN INTO ACC A FROM $52
	LDAA	#$E0	LOAD DIN WORD INTO ACC A		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	STAA	$51	LOAD DIN DATA INTO $51				
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A	WAIT3	LDAA	$1029	CHECK SPI STATUS REG
	STAA	$52	LOAD DUMMY DIN DATA INTO $52		BPL	WAIT3	CHECK IF TRANSFER IS DONE
	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000		BSET	$08,X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
LOOP	BCLR	$08,X,$01	D0 GOES LOW ($\overline{CS}$ GOES LOW)		LDAA	$102A	LOAD LTC1294 LSBs IN ACC
	LDAA	$50	LOAD DIN INTO ACC A FROM $50		STAA	$63	STORE LSBs IN $63
	STAA	$102A	LOAD DIN INTO SPI, START SCK				
	LDAA	$1029	CHECK SPI STATUS REG		JMP	LOOP	START NEXT CONVERSION
WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE				
	LDAA	$51	LOAD DIN INTO ACC A FROM $51				

Hardware and Software Interface to Intel 8051



Hardware and Software Interface to Intel 8051



APPLICATIONS INFORMATION

8051 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	SETB	P1.4	$\overline{CS}$ GOES HIGH		CLR	P1.3	CLK GOES LOW
CONT	MOV	A,#87H	DIN WORD FOR LTC1294		CLR	A	CLEAR ACC
	CLR	P1.4	$\overline{CS}$ GOES LOW		RLC	A	ROTATE DATA BIT (B3) INTO ACC
	MOV	R4,#08H	LOAD COUNTER		MOV	C,P1.2	READ DATA BIT INTO CARRY
LOOP1	RLC	A	ROTATE DIN BIT INTO CARRY		RLC	A	ROTATE DATA BIT (B2) INTO ACC
	CLR	P1.3	CLK GOES LOW		SETB	P1.3	CLK GOES HIGH
	MOV	P1.2,C	OUTPUT DIN BIT TO LTC1294		CLR	P1.3	CLK GOES LOW
	SETB	P1.3	CLK GOES HIGH		MOV	C,P1.2	READ DATA BIT INTO CARRY
	DJNZ	R4,LOOP1	NEXT DIN BIT		RLC	A	ROTATE DATA BIT (B1) INTO ACC
	MOV	P1,#04H	P1.2 BECOMES AN INPUT		SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW		CLR	P1.3	CLK GOES LOW
	MOV	R4,#09H	LOAD COUNTER		MOV	C,P1.2	READ DATA BIT INTO CARRY
LOOP	MOV	C,P1.2	READ DATA BIT INTO CARRY		SETB	P1.4	$\overline{CS}$ GOES HIGH
	RLC	A	ROTATE DATA BIT (B3) INTO ACC		RRC	A	ROTATE DATA BIT (B0) INTO ACC
	SETB	P1.3	CLK GOES HIGH		RRC	A	ROTATE RIGHT INTO ACC
	CLR	P1.3	CLK GOES LOW		RRC	A	ROTATE RIGHT INTO ACC
	DJNZ	R4,LOOP	NEXT DOUT BIT		RRC	A	ROTATE RIGHT INTO ACC
	MOV	R2,A	STORE MSBs IN R2		MOV	R3,A	STORE LSBs IN R3
	MOV	C,P1.2	READ DATA BIT INTO CARRY		AJMP	CONT	START NEXT CONVERSION
	SETB	P1.3	CLK GOES HIGH				

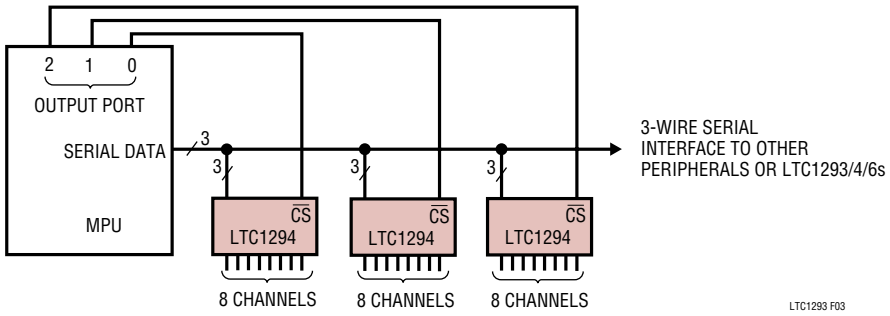


Figure 3. Several LTC1294 Sharing One 3-Wire Serial Interface

Sharing the Serial Interface

The LTC1293/4/6 can share the same 3-wire serial interface with other peripheral components or other LTC1293/4/6's (Figure 3). Now, the $\overline{CS}$ signals decide which LTC1293/4/6 is being addressed by the MPU.

ANALOG CONSIDERATIONS

Grounding

The LTC1293/4/6 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a PC board. The analog ground pin (AGND) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). The digital ground pin (DGND) also can be tied directly to this ground pin because minimal digital noise is generated within the chip itself. V_{CC} should be bypassed to the ground plane with a 22µF (minimum value) tantalum with leads as short as possible and as close as possible to the pin. A 0.1µF ceramic disk also should be placed in parallel with the 22µF and again with leads as short as possible and as close to V_{CC} as possible. AV_{CC} and DV_{CC} should be tied together on the

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LTC1294. Figure 4 shows an example of an ideal LTC1293/4/6 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

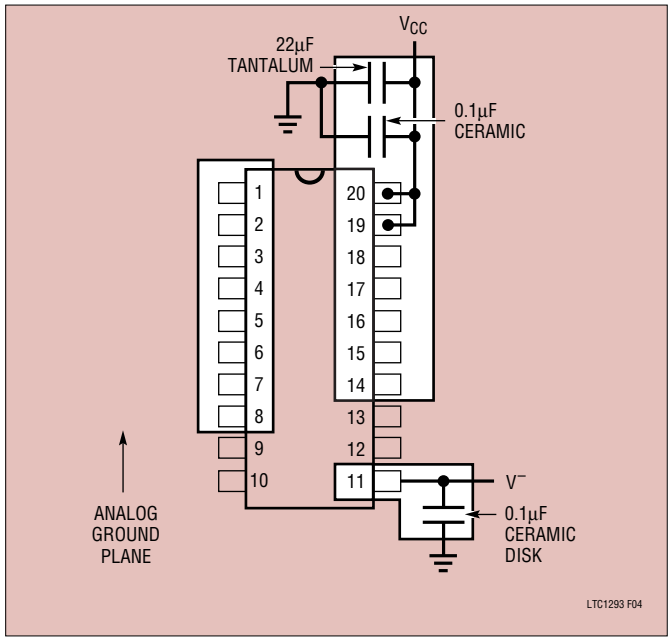

Figure 4. Ground Plane for the LTC1293/4/6

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance such as obtained from a voltage regulator (e.g., LT323A). For high frequency bypassing a 0.1µF ceramic disk placed in parallel with the 22µF is recommended. Again the leads should be kept to a minimum. Figure 5 and 6 show the effects of good and poor V_{CC} bypassing.

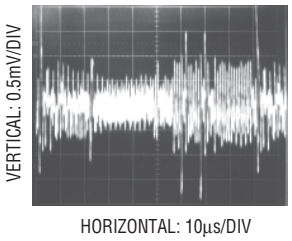

Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors.

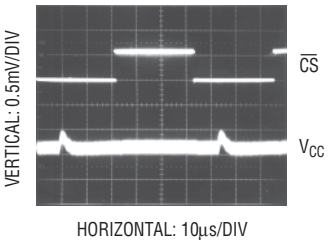

Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1293/4/6 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

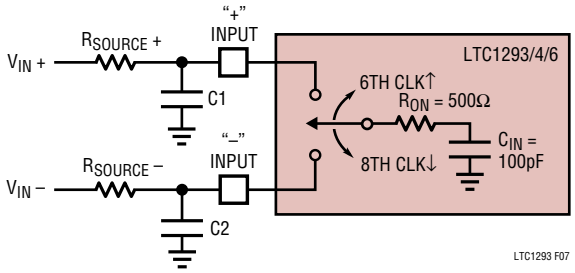

Figure 7. Analog Input Equivalent Circuit

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Source Resistance

The analog inputs of the LTC1293/4/6 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}). C_{IN} gets switched between (+) and (–) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

"+" Input Settling

The input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 8). The sample period 2 1/2 CLK cycles before a conversion starts. The voltage on the "+" input must settle completely within the sample period. Minimizing R_{SOURCE}+ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 2.5µs **R_{SOURCE}+ < 1.5kΩ and C1 < 20pF will provide adequate settling time.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "-" input and the conversion starts (see Figure 8). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 1MHz, **R_{SOURCE}– < 250Ω and C2 < 20pF will provide adequate settling**.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figure 8). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle

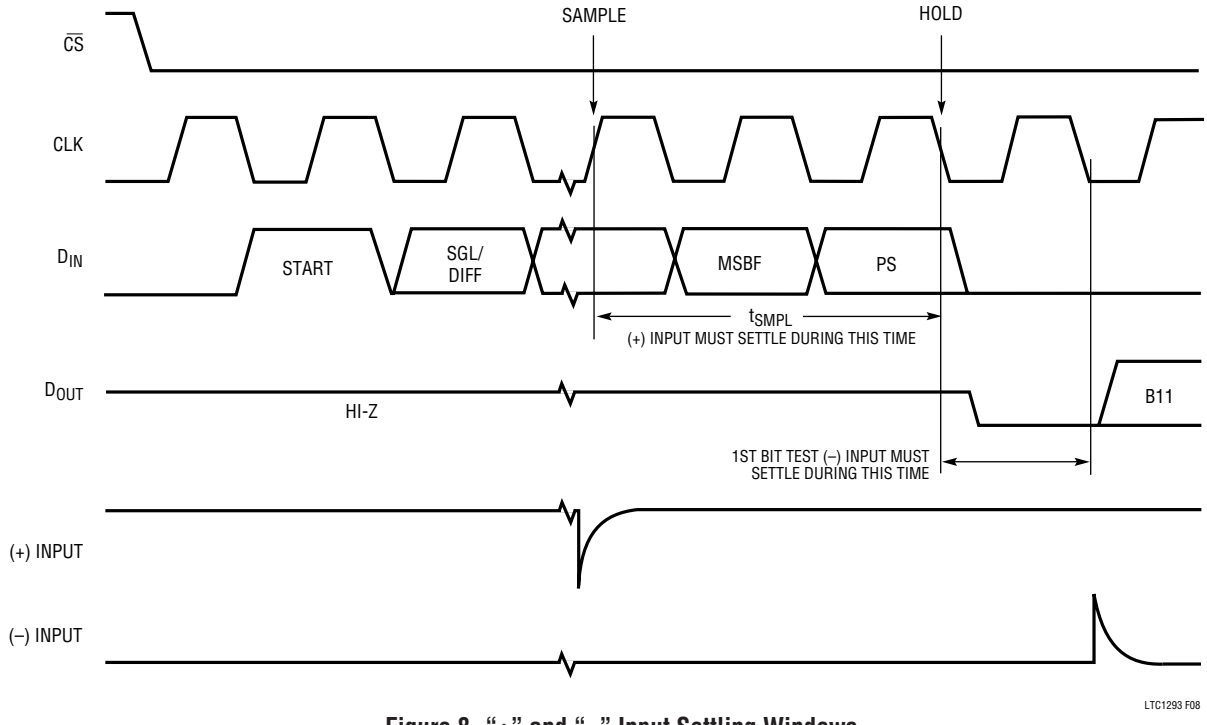

Figure 8. "+" and "–" Input Settling Windows

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within the minimum settling windows of 2.5µs ("+" input) and 1µs("–" input) that occurs at the maximum clock rate of 1MHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

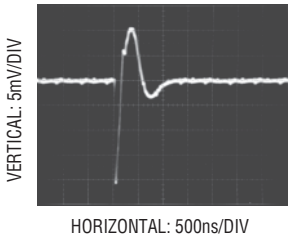

Figure 9. Adequate Settling of Op Amp Driving Analog Input

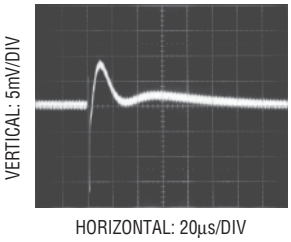

Figure 10. Poor Op Amp Settling Can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1µF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 21.5µs, the input current equals 23µA at V_{IN} = 5V. Here a filter resistor of 5Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the typical performance characteristic curve Maximum Filter Resistor vs Cycle Time.

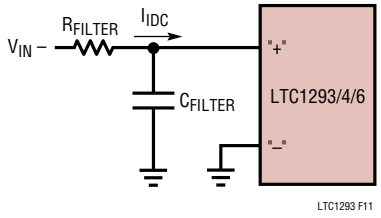

Figure 11. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical performance characteristic curve Input Channel Leakage Current vs Temperature).

SAMPLE AND HOLD

Single-Ended Input

The LTC1293/4/6 provides a built-in sample and hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). The sample and hold allows the LTC1293/4/6 to convert rapidly varying signals (see typical performance characteristic curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling edge of the PS bit is received. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the selected "+" input is sampled and held and can be rapidly time varying. The voltage on the "–" pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-)}$ is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK.

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Usually V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 0.25LSB error (300µV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-)MAX} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (300µV) the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz. **Unused inputs should be tied to the ground plane.**

Reference Input

The voltage on the reference input of the LTC1293/4/6 determines the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

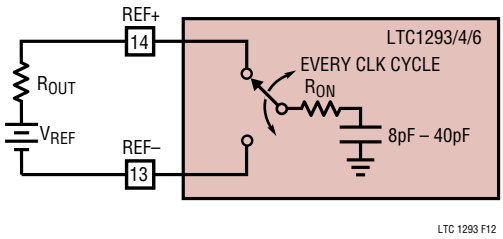

Figure 12. Reference Input Equivalent Circuit

Figure 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 1MHz most references and op amps can be made to settle within the 1µs bit time. For example the LT1027 will settle adequately or with a 10µF bypass capacitor at V_{REF} the LT1021 also can be used.

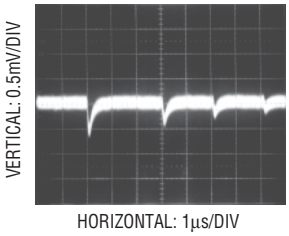

Figure 13. Adequate Reference Settling (LT1027)

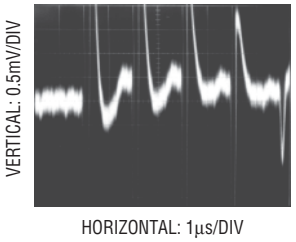

Figure 14. Poor Reference Settling Can Cause A/D Errors

Reduced Reference Operation

The effective resolution of the LTC1293/4/6 can be increased by reducing the input span of the converter. The LTC1293/4/6 exhibits good linearity over a range of reference voltages (see typical performance characteristics curves of Change in Linearity vs Reference Voltage and Change in Gain Error vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and Noise are factors that must be considered when operating at low V_{REF} values. For the LTC1293 REF^- has been tied to the AGND pin. Any voltage drop from the AGND pin to the ground plane will cause a gain error.

Offset with Reduced V_{REF}

The offset of the LTC1293/4/6 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristic curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSB's is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.1LSB with a 5V reference becomes 0.4LSB with

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a 1.25 reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1293/4/6.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1293/4/6 can be reduced to approximately 200μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference input but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristic curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200μV of noise.

For operation with a 5V reference, the 200μV noise is only 0.16LSB peak-to-peak. Here the LTC1293/4/6 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200μV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Gain Error due to Reduced V_{REF}

The gain error of the LTC1294/6 is very good over a wide range of reference voltages. The error component that is seen in the typical performance characteristics curve Change in Gain Error vs Reference Voltage for the LTC1293 is due the voltage drop on the AGND pin from the device to the ground plane. To minimize this error the LTC1293 should be soldered directly onto the PC board. The internal reference point for V_{REF} is tied to AGND. Any voltage drop in the AGND pin will make the reference voltage, internal to the device, less than what is applied externally (Figure 15). This drop is typically 400μV due to the product of the pin resistance (R_{PIN}) and the LTC1293 supply current. For example, with V_{REF} = 1.25V this will result in a gain error change of –1.0LSB from the gain error measured with V_{REF} = 5V.

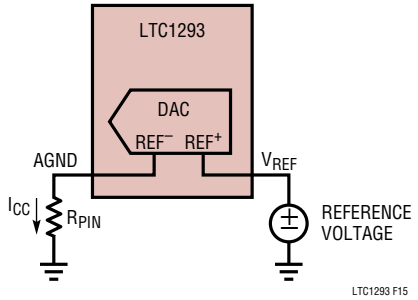

Figure 15. Parasitic Pin Resistance (R_{PIN})

LTC1293/4/6 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/Ds in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits"(ENOB). SNR is the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the non-fundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

SNR = (6.02N + 1.76dB)

where N is the number of bits. Thus the SNR depends on the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform (FFT) plot of the output spectrum of the LTC1294 is shown in Figures 16a and 16b. The input (f_{IN}) frequencies are 1kHz and 22kHz with the sampling frequency (f_S) at 45.4kHz. The SNR obtained from the plot are 72.7dB and 72.5dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \left(\frac{SNR - 1.76dB}{6.02} \right)$$

This is the so-called effective number of bits (ENOB). For the example shown in Figures 16a and 16b, N = 11.8 bits. Figure 17 shows a plot of ENOB as a function of input frequency. The top curve shows the A/D's ENOB remains at 11.8 for input frequencies up to $f_S/2$ with ±5V supplies.

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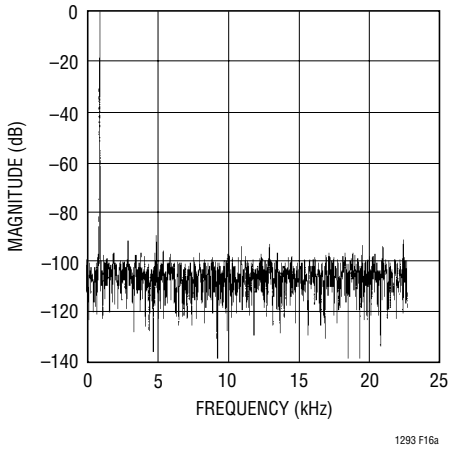

Figure 16a. LTC1294 FFT Plot f_{IN} = 1kHz, f_S = 45.4kHz, SNR = 72.7dB with ±5V Supplies

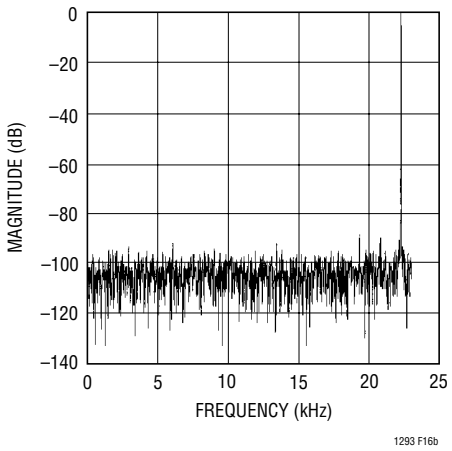

Figure 16b. LTC1294 FFT Plot f_{IN} = 22kHz, f_S = 45.4kHz, SNR = 72.5dB with ±5V Supplies

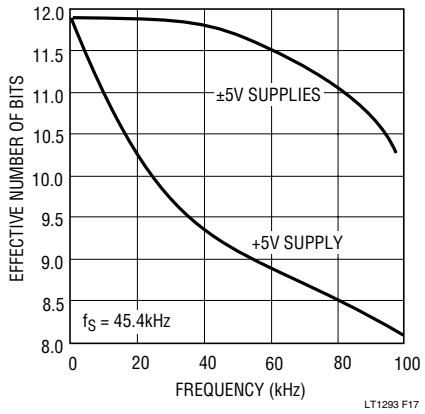

Figure 17. LTC1294 ENOB vs Input Frequency

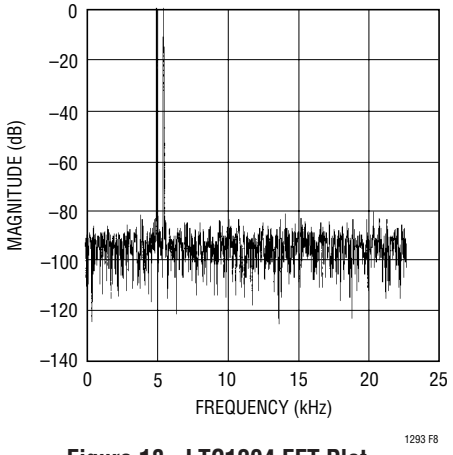

Figure 18. LTC1294 FFT Plot $f_{IN}1$ = 5.1kHz, $f_{IN}2$ = 5.6kHz, f_S = 45.4kHz with ±5V Supplies

For +5V supplies the ENOB decreases more rapidly. This is due predominantly to the 2nd harmonic distortion term.

Figure 18 shows a FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

Overvoltage Protection

Applying signals to the LTC1293/4/6's analog inputs that exceed the positive supply or that go below V^- will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1293/4/6. Another example is the input source is operating from different supplies of larger value than the LTC1293/4/6. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 19 diode clamps from the inputs to V_{CC} and V^- are used. The second method is to put resistors in series with the analog inputs for current limiting. As shown in Figure 20a, a 1kΩ resistor is enough to stand off ±15V (15mA for only one channel). If more than one channel exceeds the supplies than the following guidelines can be used. Limit the current to 7mA per channel and 28mA for all channels.

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This means four channels can handle 7mA of input current each. Reducing CLK frequency from a maximum of 1MHz (See typical performance characteristics curves Maximum CLK Frequency vs Source Resistance and Sample and Hold Acquisition Time vs Source Resistance) allows the use of larger current limiting resistors. The "+" input can accept a resistor value of 1kΩ but the "–" input cannot accept more than 250Ω when the maximum clock frequency of 1MHz is used. If the LTC1293/4/6 is clocked at the maximum clock frequency and 250Ω is not enough to current limit the "–" input source then the clamp diodes are recommended (Figures 20a and 20b). The reason for the limit on the resistor value is the MSB bit test is affected by the value of the resistor placed at the "–" input (see discussion on Analog Inputs and the typical performance characteristics curve Maximum CLK Frequency vs Source Resistance).

If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 21).

For dual supplies (bipolar mode) placing two Schottky diodes from V_{CC} and V^- to ground (Figure 22) will prevent power supply reversal from occuring when an input source is applied to the analog MUX before power is applied to the device. Power supply reversal occurs, for example, if the input is pulled below V^-. V_{CC} will then pull a diode drop below ground which could cause the device not to power up properly. Likewise, if the input is pulled above V_{CC}, V^- will be pulled a diode drop above ground. If no inputs are present on the MUX, the Schottky diodes are not required if V^- is applied first then V_{CC}.

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

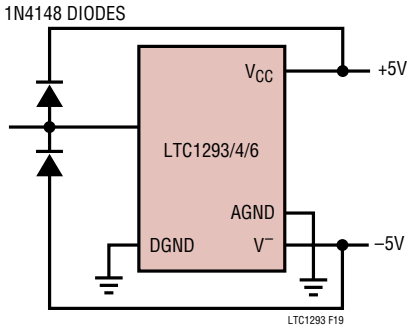


Figure 19. Overvoltage Protection for Inputs

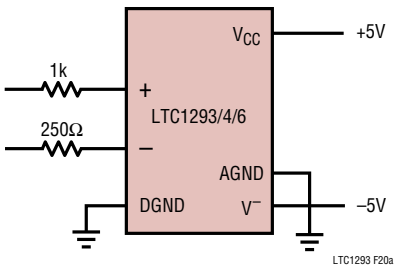


Figure 20a. Overvoltage Protection for Inputs

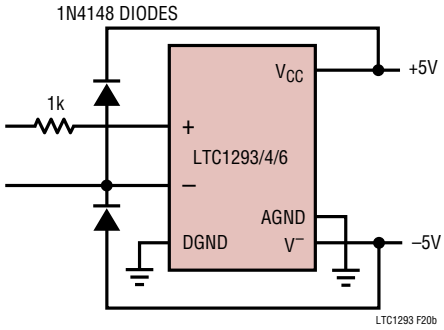


Figure 20b. Overvoltage Protection for Inputs

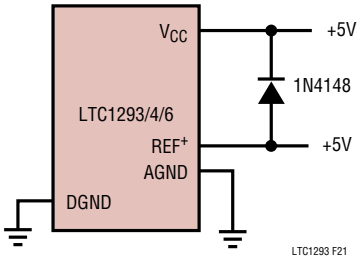


Figure 21

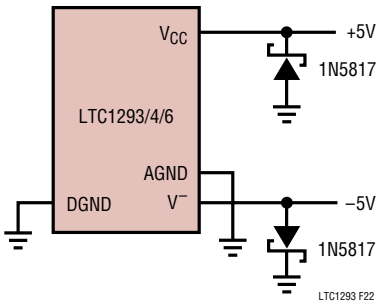


Figure 22. Power Supply Reversal

APPLICATIONS INFORMATION

A "Quick Look" Circuit for the LTC1294/6

Users can get a quick look at the function and timing of the LTC1294/6 by using the following simple circuit (Figure 23). V_{REF} is tied to V_{CC}. D_{IN} is tied high which means V_{IN} should be applied to the CH7 with respect to COM. A Unipolar conversion is requested and the data is output MSB first. $\overline{CS}$ is driven at 1/64 the clock rate by the CD4520 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 24).

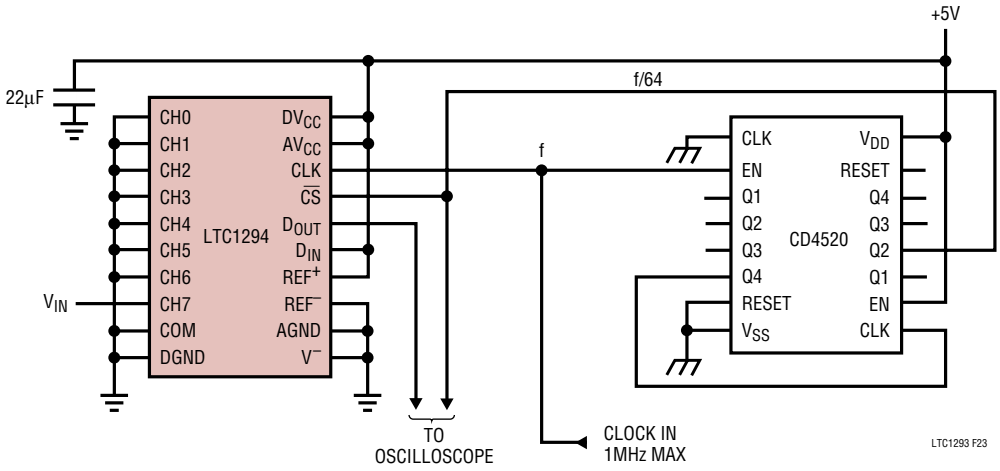


Figure 23. "Quick Look" Circuit for the LTC1294/6

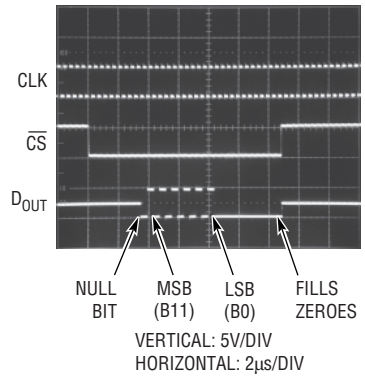
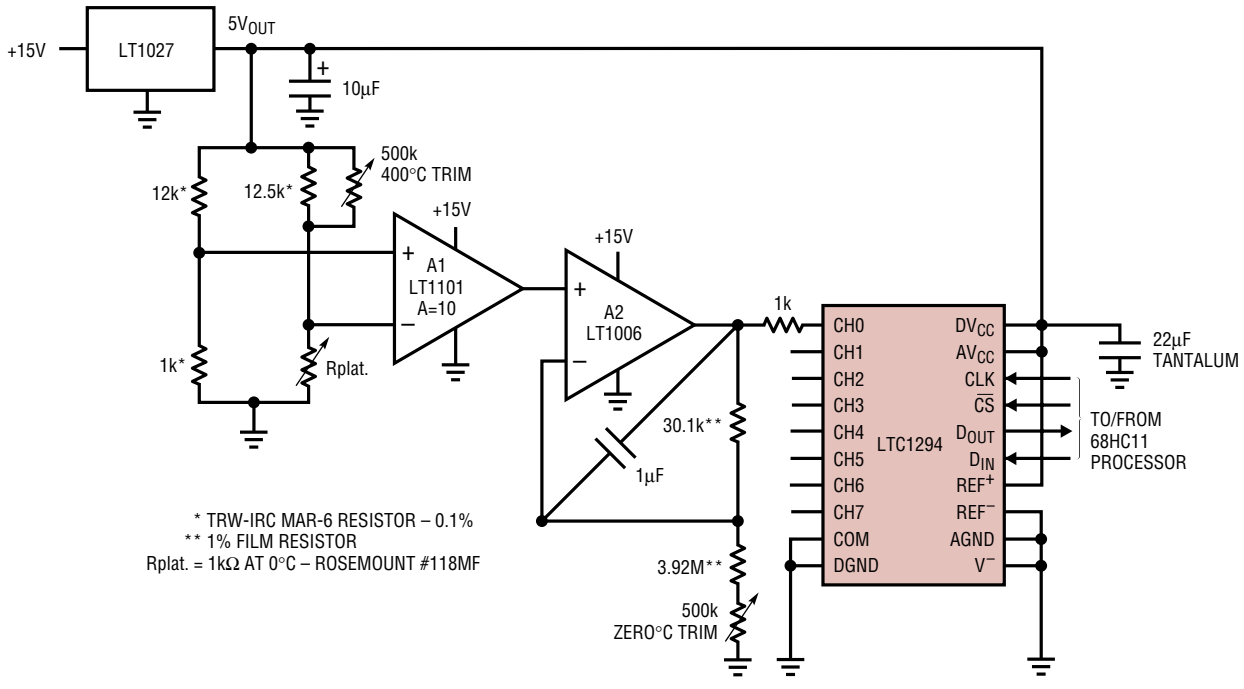


Figure 24. Scope Trace of the LTC1294/6 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

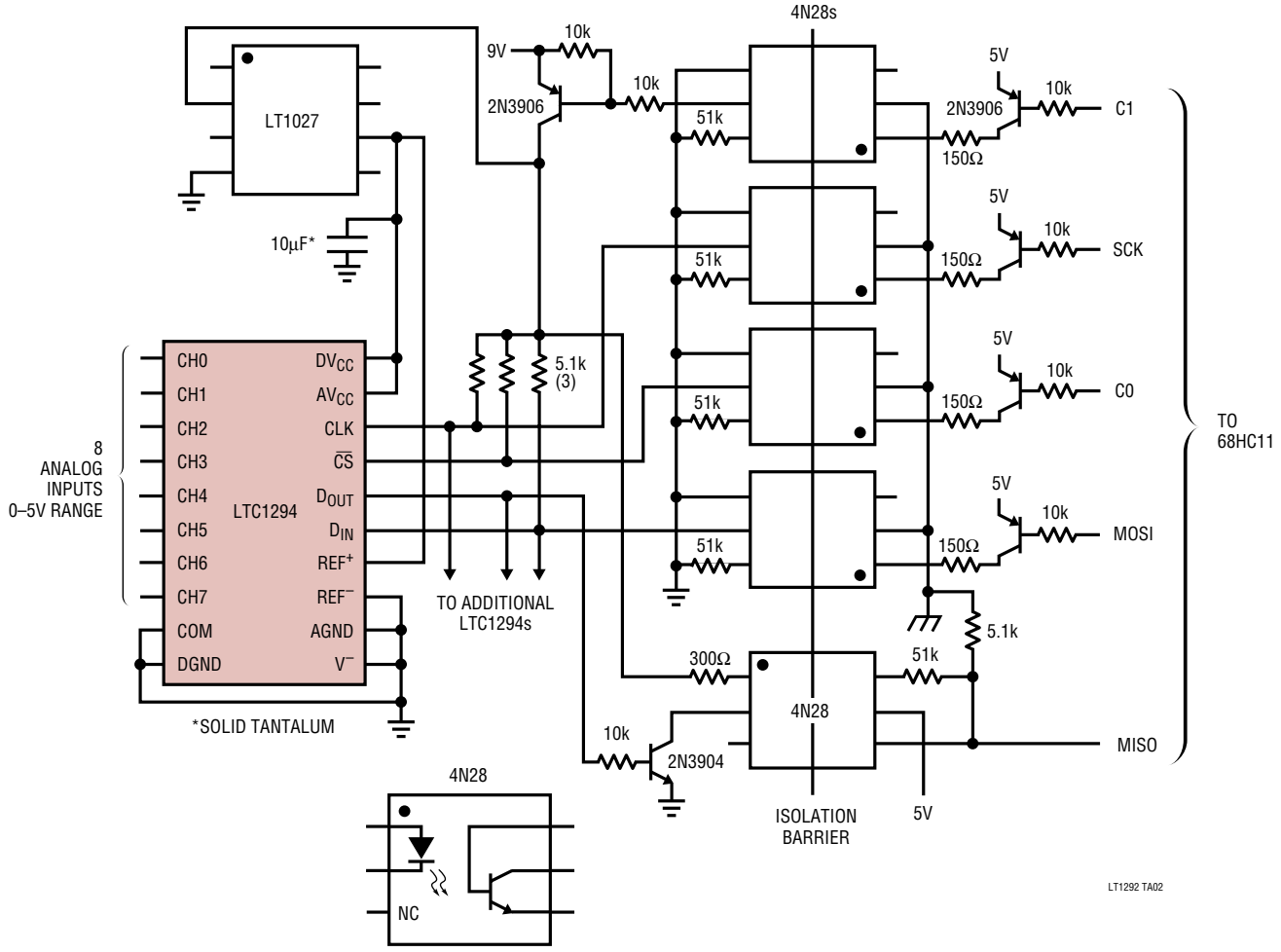
TYPICAL APPLICATIONS

Digitally Linearized Platinum RTD Signal Conditioner



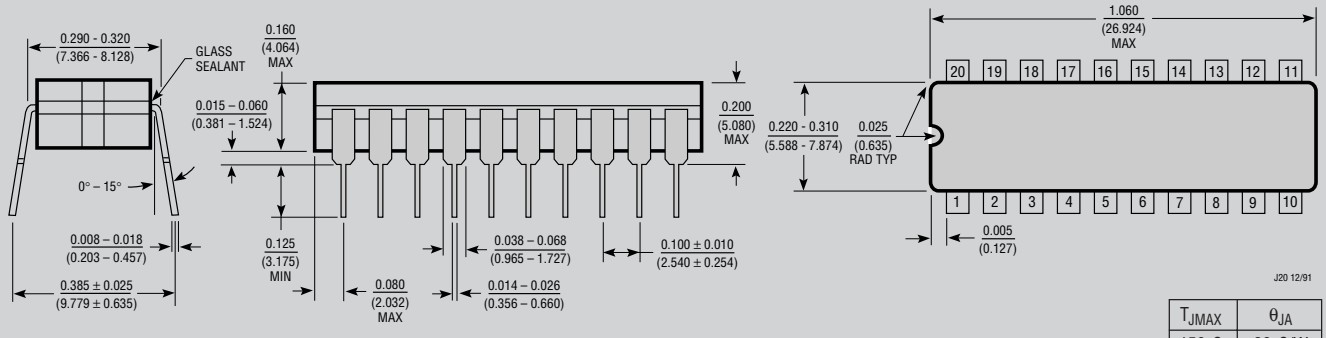
TYPICAL APPLICATIONS

Micropower, 5000V Opto-Isolated, Multichannel,12-Bit Data Acquisition System is Accessed Once Every Two Seconds



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
20-Lead Ceramic DIP

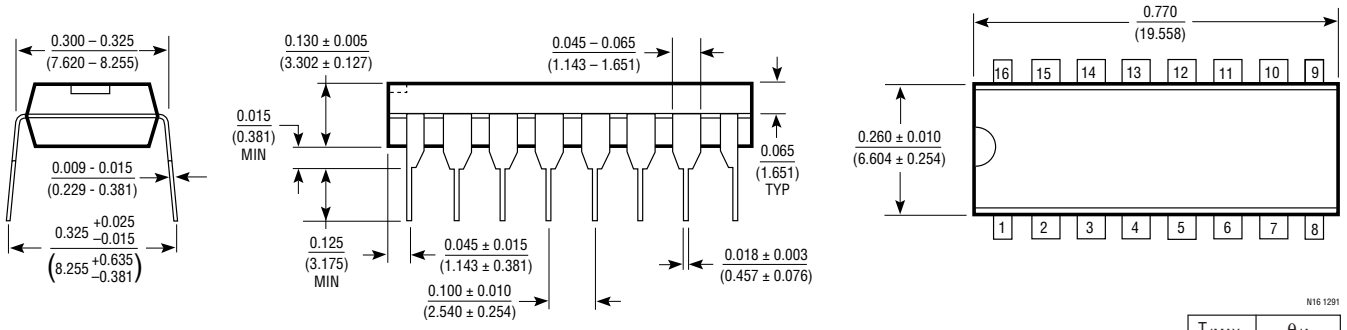


J20 12/91

T_{JMAX}	θ_{JA}
150°C	80°C/W

OBSOLETE PACKAGE

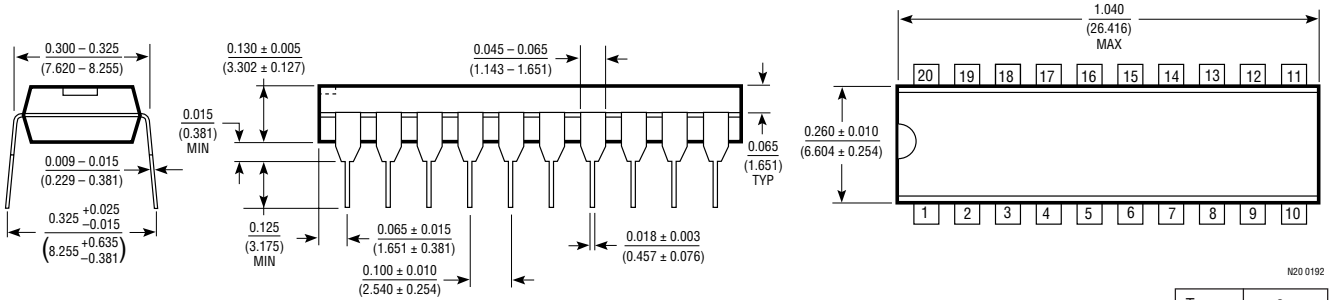
N Package
16-Lead Plastic DIP



N16 1291

T_{JMAX}	θ_{JA}
110°C	100°C/W

N Package
20-Lead Plastic DIP



N20 0192

T_{JMAX}	θ_{JA}
110°C	100°C/W

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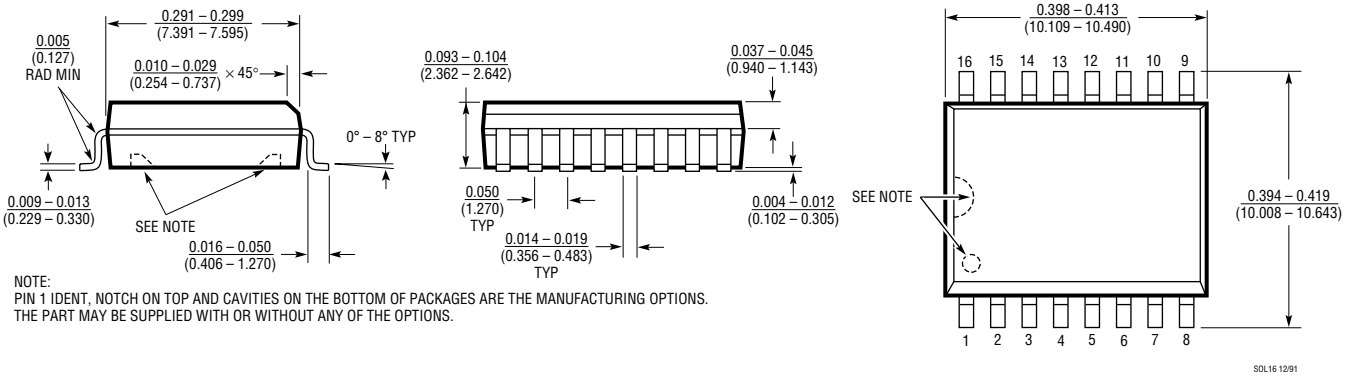
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

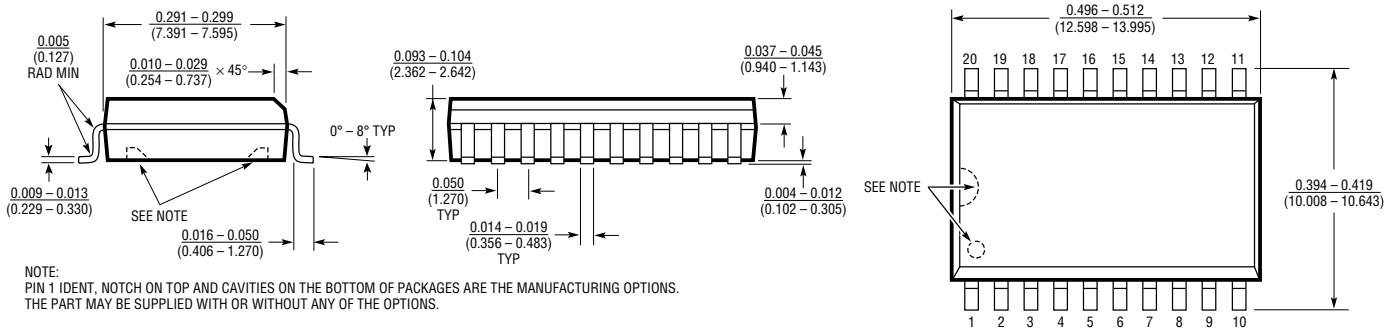
S Package
16-Lead Plastic SOL



NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

T_{JMAX}	θ_{JA}
110°C	150°C/W

S Package
20-Lead Plastic SOL



NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

T_{JMAX}	θ_{JA}
110°C	150°C/W

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