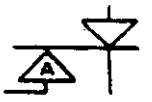
SILICON POWER

High Power 53mm Silicon Controlled Rectifier

1000 A Avg. Up To 3200 Volts

C702



The C702 Reverse Blocking Thyristor now has extended voltage blocking capability through unique multi-diffusion processing of 53 mm nominal silicon without sacrificing essential ratings and characteristics.

The C702 is designed specifically for phase control applications like DC motor control, power supplies, cycloconverters and load commutated inverters.

THYRISTOR (SCR) PRESSPAK

FEATURES

- Optimized pilot gate for high di/dt rating
- Excellent withstand to high dv/dt voltage fronts
- Enhanced surge and I^2t ratings for fuse coordination
- Glazed-fluted ceramic with metal — metal welded seal 1.0 in., 25.4 mm creepage ⅜ in., 15.9 mm clearance

MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE V_{DRM}/V_{RRM}[2] T_J = -40°C to +125°C	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE V_{DRM}/V_{RRM}[2] T_J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE, V_{RSM}[1] T_J = -40°C to 0°C
C702CB	3200 Volts	3300 Volts	3300 Volts
C702CA	3100	3200	3200
C702CP	3000	3100	3100
C702LT	2900	3000	3000
C702LN	2800	2900	2900
C702LS	2700	2800	2800
C702LM	2600	2700	2700
C702LE	2500	2600	2600
C702LD	2400	2500	2500
C702LC	2300	2400	2400
C702LB	2200	2300	2300

Average Forward Current, On-State @ T_{case} = 70°C, $I_{T(AV)}$ 1000A
Peak One-Cycle Surge On-State Current, I_{TSM} 8.3ms 16KA
10.0ms 15KA
Maximum Repetitive Rate-of-Rise of Anode Current @ 1500V bias 100A/μs
(Switching Rates ≤ 60 Hz; snubber discharge ≤ 65A; see required gate drive)
I^2t (for fusing) (at 8.3 milliseconds)
Peak Gate Power Dissipation, P_{GM} ..... 200 W @ 40μs pulse
Average Gate Power Dissipation, $P_{G(AV)}$ 20W
Peak Reverse Gate Voltage, V_{GRM} 20V
Peak Gate Current 15A
Storage Temperature, T_{STG} ..... -40°C to +150°C
Operating Temperature, T_J ..... -40°C to +125°C
Mounting Force Required ..... 5000 - 6000 lb.
22.4 - 26.7 KN

NOTES:

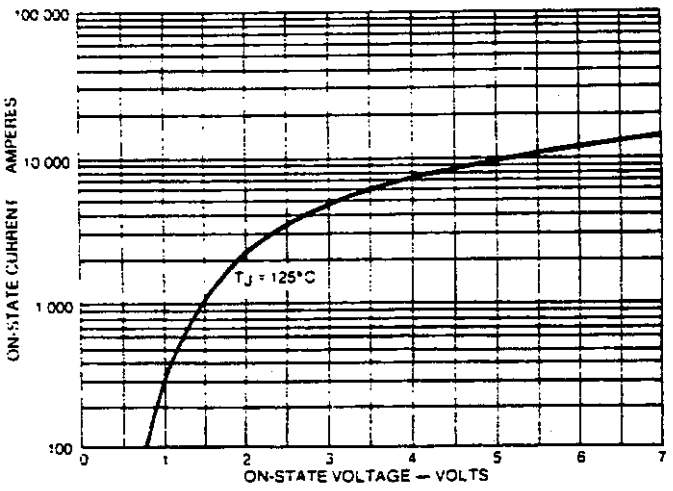
1. Half sine pulse, 10ms MAXIMUM pulse width, non repetitive
2. Assume presspak mounted to heat dissipator of less than 0.3 °C/W
3. All ratings and tests in accordance with NEMA-EIA JEDEC Standard RS-397

175 Great Valley Pkwy., Malvern, PA 19355, USA

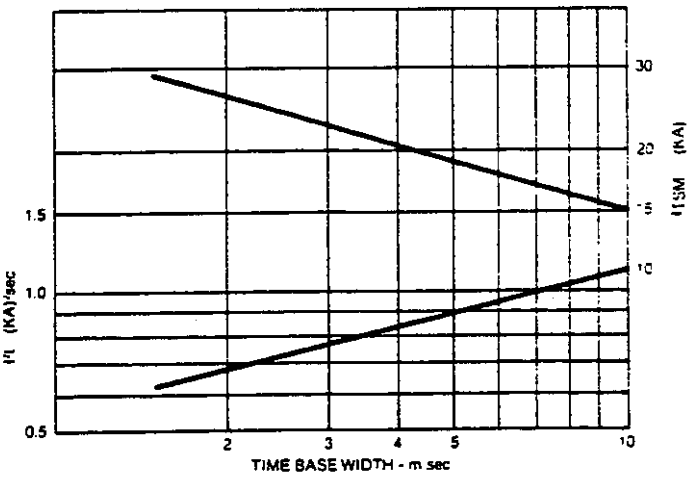
CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Units	Test Conditions or Qualifications
Peak reverse and off-state leakage current @ V_{DRM} V_{RRM} @ V_{DRM} V_{RRM} @ 0.8 V_{DRM} 0.8 V_{RRM}				10 200 75	ma	Tj = 25°C, opened gate 125°C, opened gate 125°C, opened gate
Critical rate of rise at off-state voltage (higher may cause destructive switching)	dv/dt	500	1000		V/µs	Tj = 125°C opened gate V_D = 0.8 V_{DRM}
Delay Time	t_d			2.5 1.5	µs	See gate V_D = 1500V source V_D = 500V below
Peak On-State Voltage	V_{TM}			1.5	V	IT = 1000A, 125°C Half sine pulse 8.3 msec V_D = 10V
DC Gate Trigger Current (not for operational use)	I_{GT}			200	ma	T_C = 25°C, V_D = 10V
		5				T_C = 125°C, V_D = 0.5V_{DRM}
DC Gate Trigger Current (not for operational use) *	V_{GT}			4.5	V	T_C = 25°C, V_D = 10V
		0.5				T_C = 125°C, V_D = 0.5V_{DRM}
Circuit Commutated Turn-off Time	t_q		125	250	µs	T_C = 125°C, IT = 1000A, 10A/µs Min. Reverse Voltage = 100V Reapplied off-state voltage 20 V/ms to 2000 volts
Holding Current	I_H	50 30 25	100 60 50	200 120 100	ma	T_j = 25°C, di/dt = -0.5ma/µs 105°C E = 7.5 Vrms 125°C R = 10 Ω Freq = 60 Hz
Latching Current	I_L	250 175 155	450 315 285	800 560 500	ma	T_j = 25°C, Gate Drive 105°C, 30V 10Ω 125°C, duration 15µs

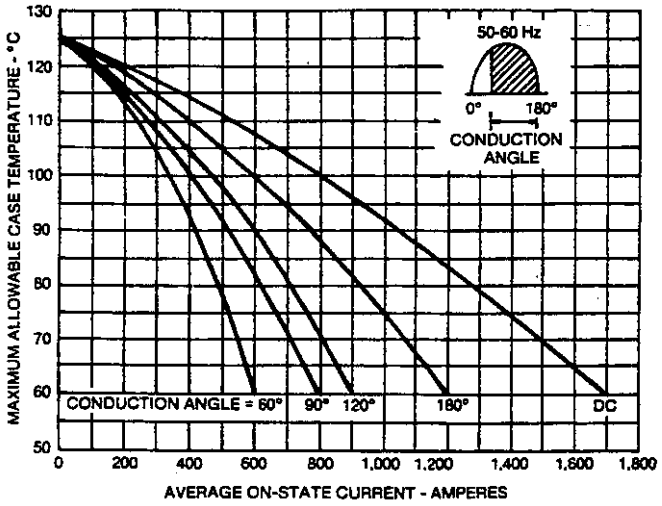
* DC trigger current and voltage are indicated as a characteristic. Turn-on in this manner will not support rated di/dt.



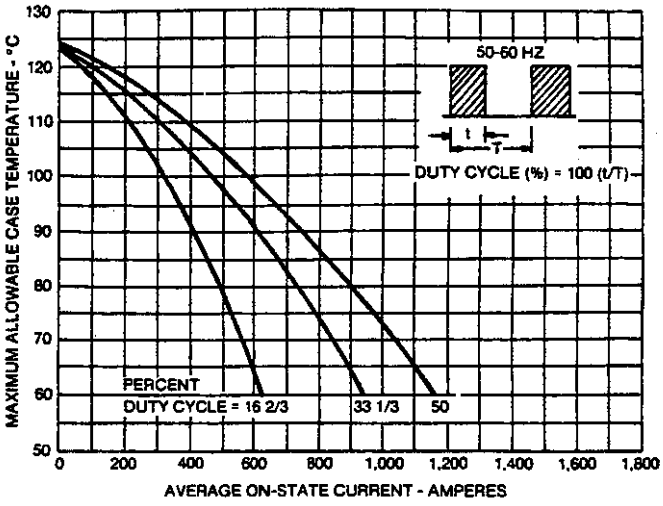
MAXIMUM FORWARD CONDUCTION CHARACTERISTIC ON-STATE



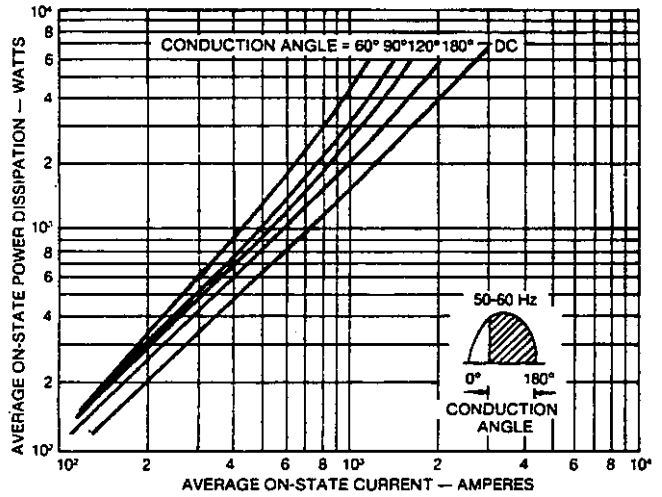
NON-REPETITIVE I_{TSM} AND I^2T CAPABILITY FOR FUSE COORDINATION



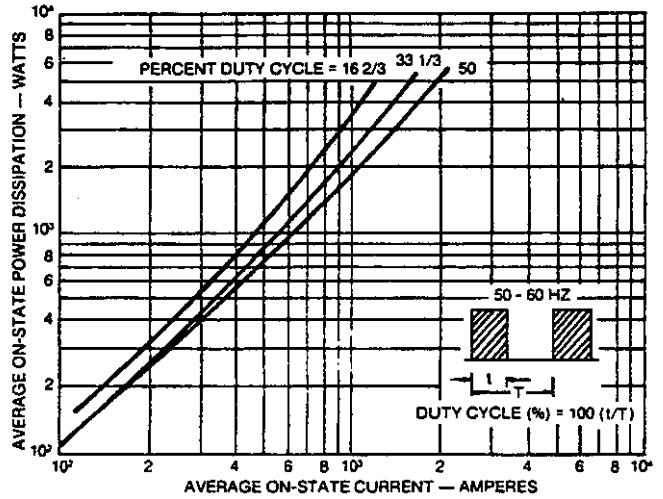
MAXIMUM ALLOWABLE CASE TEMPERATURES FOR SINUSOIDAL CURRENT WAVEFORM — DOUBLE-SIDE COOLED



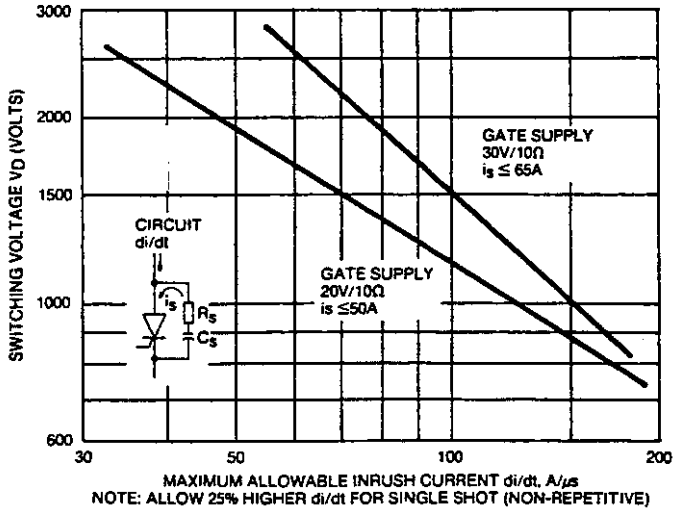
MAXIMUM ALLOWABLE CASE TEMPERATURES FOR RECTANGULAR CURRENT WAVEFORM — DOUBLE-SIDE COOLED



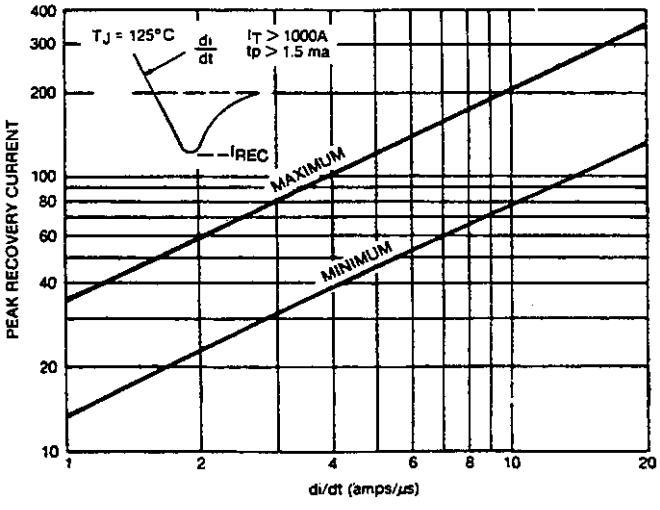
AVERAGE FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



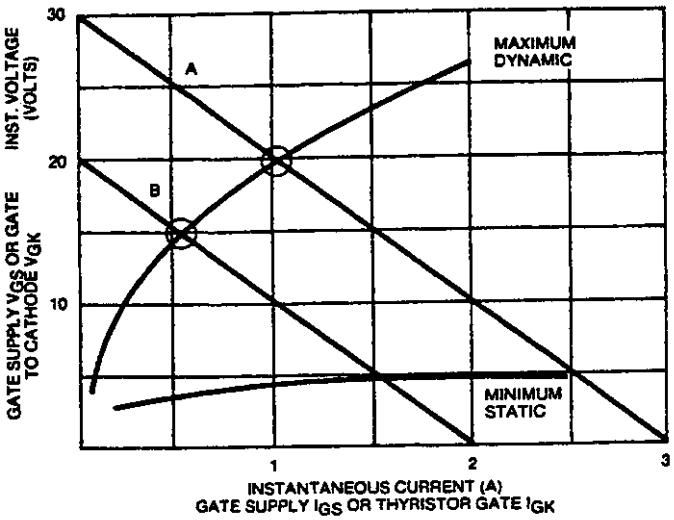
AVERAGE FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



MAXIMUM ALLOWABLE INRUSH CURRENT, CIRCUIT DI/DT AND SNUBBER DISCHARGE IS FOR TWO LEVELS OF GATE DRIVE



PEAK RECOVERY CURRENT VERSUS COMMUTATING CIRCUIT DI/DT



Thyristor Gate Impedance

— This is enhanced by fast rising gate voltage, increasing anode bias and temperature.

— It is shown at a minimum for dc voltage, zero bias and low temperature.

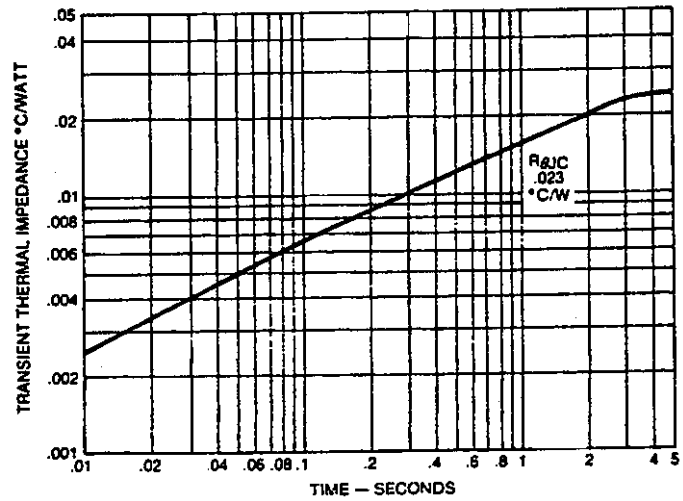
— It is shown at a maximum for operating bias and recommended gate drive.

Gate Supply

— Load lines (A) and (B) are applicable in accordance with di/dt ratings. The short circuit current rise time should be approximately 0.5μs and the duration longer than the delay time expected for the thyristor.

Minimum Acceptable Gate Current

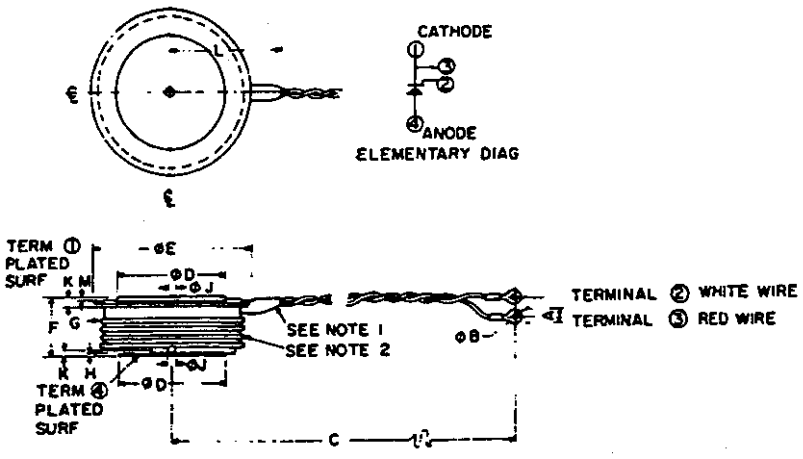
— The intersection of load line and gate characteristic (encircled) indicates the minimum value of actual current flowing into the gate that is required during the delay time interval needed for the published di, dt and snubber discharge ratings.



NOTES:

1. Add .006°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R_{\theta JS}$ = .029°C/W. See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
   - end of conducting portion of cycle
     - — 120° sq. wave add .0025°C/W along entire curve
     - — 180° sq. wave add .0018°C/W along entire curve
     - — 180° sine wave add .0010°C/W along entire curve
   - end of cycle
     - — any wave, subtract .001°C/W along entire curve.
3. Ask for general mounting instructions.

OUTLINE DRAWING



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	0.200	0.240	5.08	6.10	1
ϕB	0.140	—	3.56	—	
C	16.000	20.000	406.40	508.00	
ϕD	1.700	1.900	43.18	48.26	
ϕE	—	2.960	—	75.18	
F	1.000	1.070	25.40	27.18	
G	—	—	—	—	2
H	.005	.067	0.13	1.70	
ϕJ	0.136	0.146	3.45	3.71	
K	.070	.100	1.78	2.54	
L	—	2.500	—	63.50	
M	.030	—	0.76	—	

NOTES:
1. Contour and orientation of term lugs is undefined.
2. Glazed ceramic insulator with 1.00 inch (25.40 mm) surface creepage, min.

4. Anode-Cathode Pole Faces ④ ① Nickel Plated Copper.
5. Mating Surface Requirement TIR ≤.0005 inch Finish 32.
6. Mounting Force, 5000-6000 Lb., 22.4-26.7 KN.
7. Electrical Insulation, Glazed Ceramic, Creepage 1 in. (25.4mm), Strike ⅜ in. (15.9mm)
8. Gate Leads ② ③ 18 in. #22 Terminated with #8 Ring Terminal, Cathode Wire-Red, Gate Wire-White.