

- Low $r_{DS(on)}$. . . 0.3 Ω Typ
- High Output Voltage . . . 60 V
- Pulsed Current . . . 6 A Per Channel
- Avalanche Energy Capability . . . 36 mJ
- Input Transient Protection . . . 2000 V

description

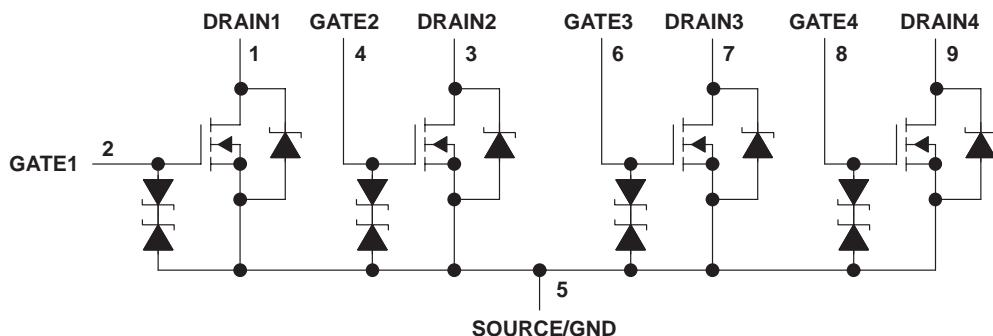
The TPIC2401 is a monolithic power DMOS array that consists of four electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains. Each transistor features integrated high-current zener diodes to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 2000 V of ESD protection when tested using the human-body model.

The TPIC2401 is offered in a 9-pin PowerFLEX™ (KTA) package and is characterized for operation over the case temperature range of -40°C to 125°C .

KTA PACKAGE
(TOP VIEW)

9	DRAIN4
8	GATE4
7	DRAIN3
6	GATE3
5	SOURCE/GND
4	GATE2
3	DRAIN2
2	GATE1
1	DRAIN1

schematic



NOTE A: For correct operation, no output pin may be taken below GND.



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TPIC2401

4-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

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absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Gate-to-source voltage, V_{GS}	-9 V to 18 V
Continuous drain current, each output, all outputs on, $T_C = 25^\circ\text{C}$	1.5 A
Pulsed drain current, each output, $I_{D\text{max}}$, $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 7)	6 A
Continuous gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	± 25 mA
Pulsed gate-to-source zener diode current, $T_C = 25^\circ\text{C}$	± 250 mA
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figures 4 and 6)	36 mJ
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$	1.7 W
Power dissipation at (or below) $T_C = 75^\circ\text{C}$, all outputs on	15 W
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range, T_{stg}	-40°C to 125°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage $I_D = 250 \mu\text{A}, V_{GS} = 0$	60			V
$V_{GS(\text{th})}$	Gate-to-source threshold voltage $I_D = 1 \text{ mA}, V_{DS} = V_{GS},$ See Figure 5	1.5	2.05	2.2	V
$V_{GS(\text{th})\text{match}}$	Gate-to-source threshold voltage matching		5	40	
$V_{(BR)GS}$	Gate-to-source breakdown voltage $I_{GS} = 250 \mu\text{A}$	18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage $I_{SG} = 250 \mu\text{A}$	9			V
$V_{DS(\text{on})}$	Drain-to-source on-state voltage $I_D = 1.5 \text{ A}, V_{GS} = 10 \text{ V},$ See Notes 2 and 3		0.45	0.54	V
$V_F(\text{SD})$	Forward on-state voltage, source-to-drain $I_S = 1.5 \text{ A}, V_{GS} = 0 \text{ V},$ See Notes 2 and 3 and Figure 12		0.85	1	V
I_{DSS}	Zero-gate-voltage drain current $V_{DS} = 48 \text{ V},$ $V_{GS} = 0$	0.05	1		μA
			0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source $V_{GS} = 15 \text{ V}, V_{DS} = 0$	20	200		nA
I_{GSSR}	Reverse gate current, drain short circuited to source $V_{SG} = 5 \text{ V}, V_{DS} = 0$	10	100		nA
$r_{DS(\text{on})}$	Static drain-to-source on-state resistance $V_{GS} = 10 \text{ V},$ $I_D = 1.5 \text{ A},$ See Notes 2 and 3 and Figures 6 and 7	0.3	0.36		Ω
			0.48	0.6	
g_{fs}	Forward transconductance $V_{DS} = 15 \text{ V}, I_D = 1 \text{ A},$ See Notes 2 and 3 and Figure 9	0.9	1.15		S
C_{iss}	Short-circuit input capacitance, common source		180	225	
C_{oss}	Short-circuit output capacitance, common source $V_{DS} = 25 \text{ V},$ $f = 1 \text{ MHz},$ $V_{GS} = 0,$ See Figure 11	100	138		pF
C_{rss}	Short-circuit reverse transfer capacitance, common source		75	100	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr} Reverse-recovery time	$I_S = 0.75 \text{ A}, V_{DS} = 48 \text{ V},$ $V_{GS} = 0, \frac{di}{dt} = 100 \text{ A}/\mu\text{s},$ See Figures 1 and 14	80			ns
Q_{RR} Total diode charge		180			nc

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Delay time, $V_{GS} \uparrow$ to $V_{DS} \downarrow$ turn on	$V_{DD} = 25 \text{ V}, R_L = 25 \Omega, t_{on} = 10 \text{ ns},$ $t_{dis} = 10 \text{ ns},$ See Figure 2	194			ns
$t_{d(off)}$ Delay time, $V_{GS} \downarrow$ to $V_{DS} \uparrow$ turn off		430			
t_r Rise time, V_{DS}		180			
t_f Fall time, V_{DS}		90			
Q_g Total gate charge	$V_{DD} = 48 \text{ V}, I_D = 1 \text{ A}, V_{GS} = 10 \text{ V},$ See Figure 3	4	5		nC
$Q_{gs(th)}$ Threshold gate-to-source charge		0.45	0.56		
Q_{gd} Gate-to-drain charge		1.55	1.93		
L_D Internal drain inductance		5			nH
L_S Internal source inductance		5			
R_g Internal gate resistance		500			Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	All outputs with equal power	72			°C/W
$R_{\theta JC}$ Junction-to-case thermal resistance		5			
		8.5			

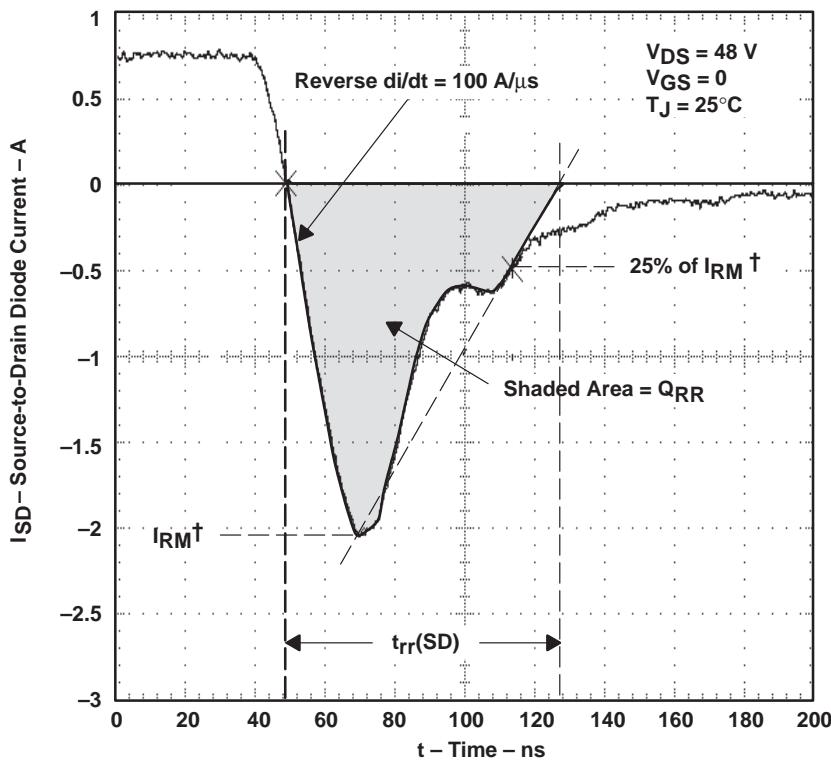
NOTES:

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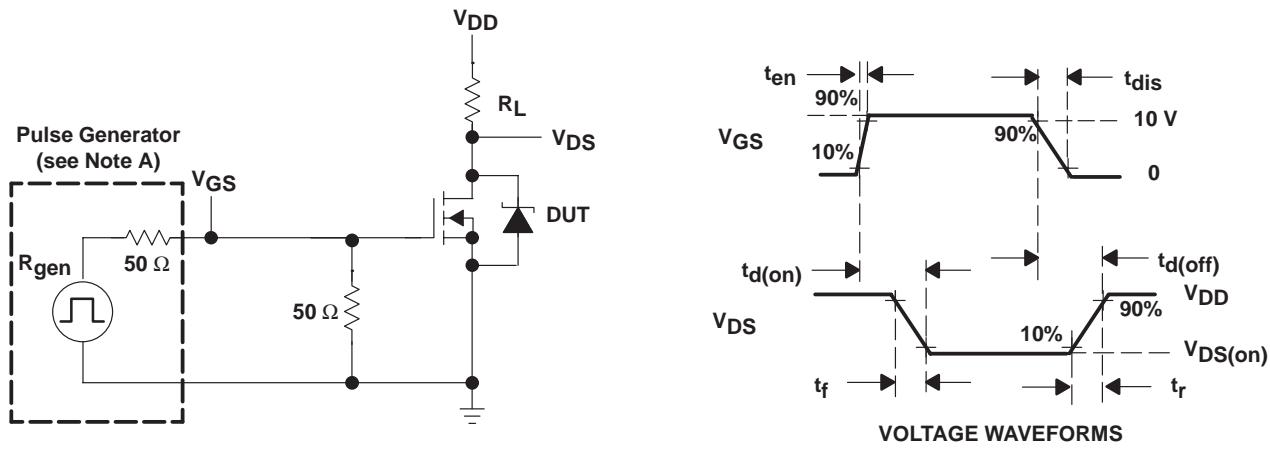
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PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery Current Waveform of Source-to-Drain Diode



NOTE A: The pulse generator has the following characteristics: $t_{en} \leq 10$ ns, $t_{dis} \leq 10$ ns, $Z_O = 50 \Omega$.

Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

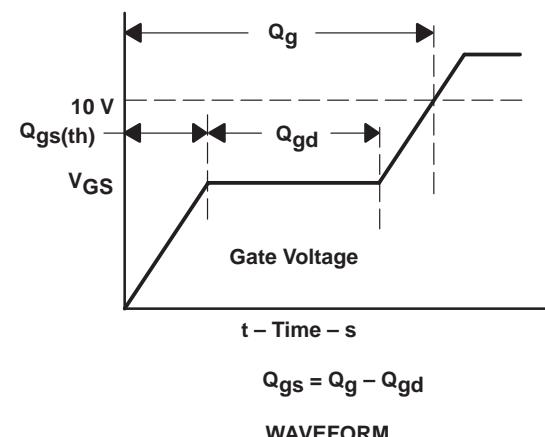
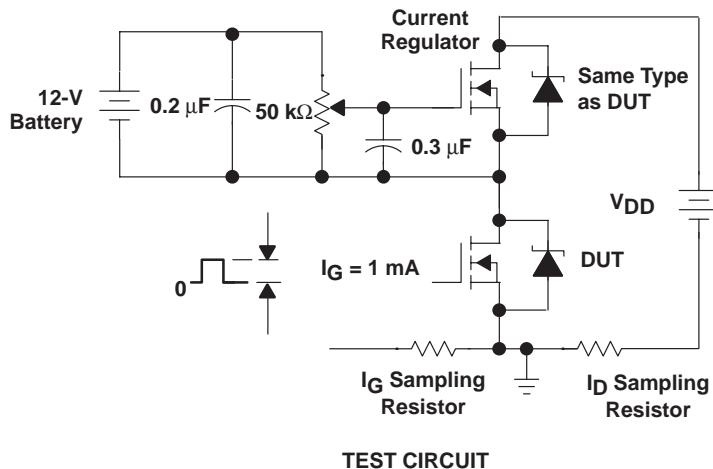
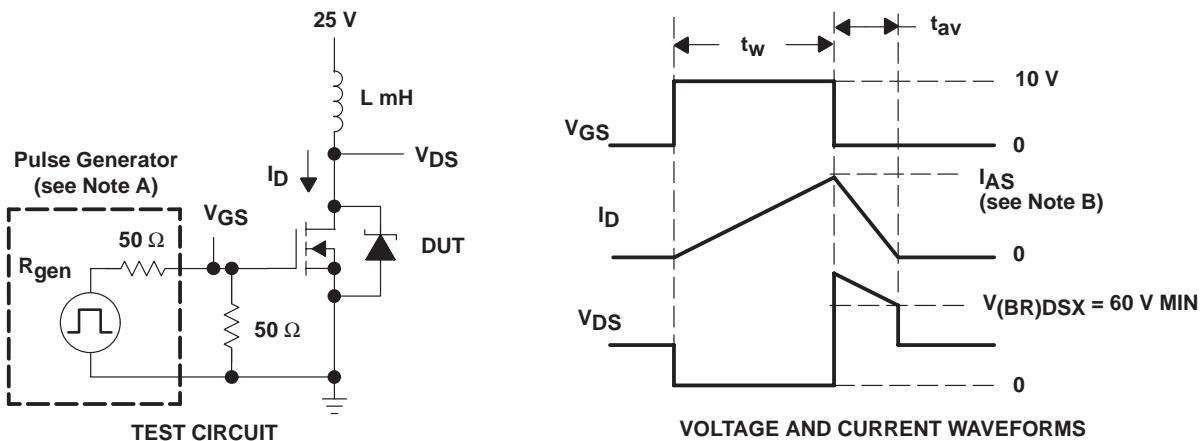


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 1.5$ A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 36$ mJ minimum where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

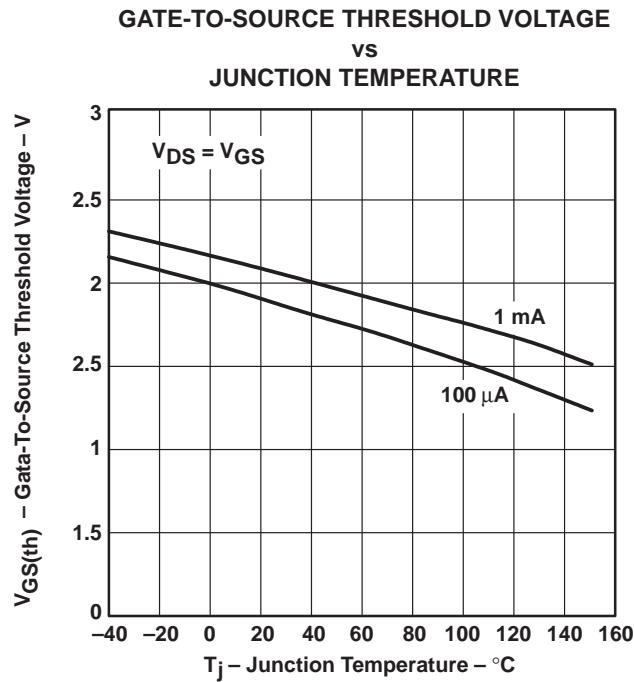


Figure 5

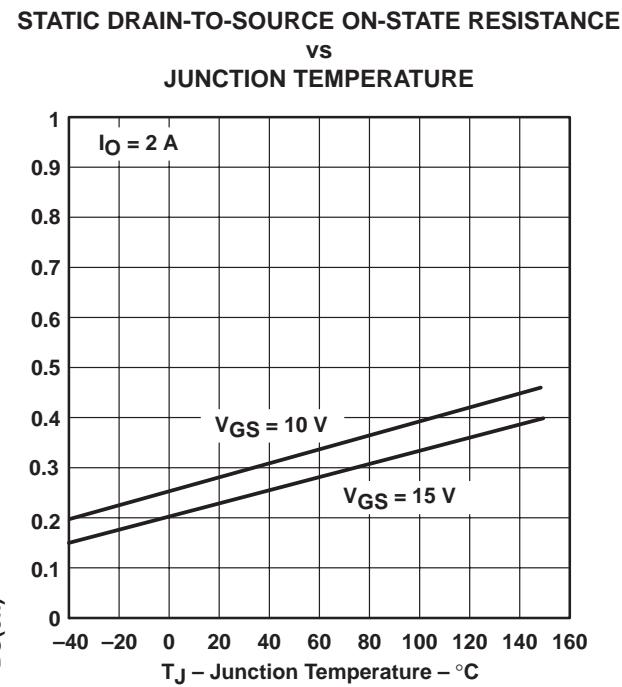


Figure 6

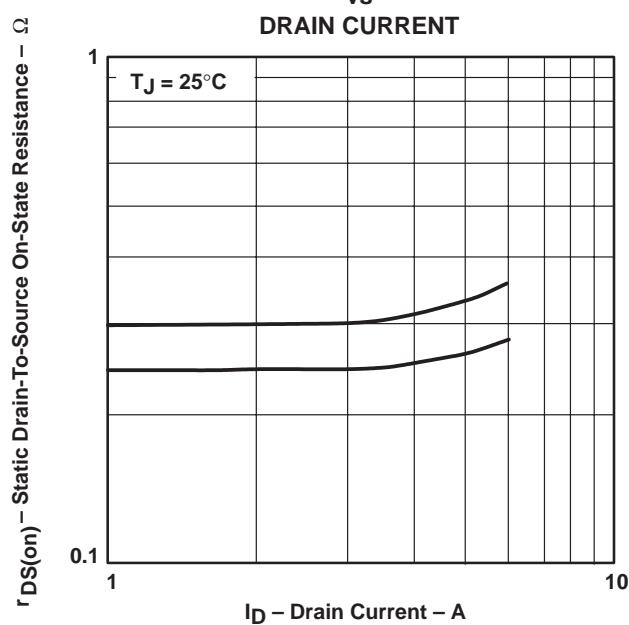


Figure 7

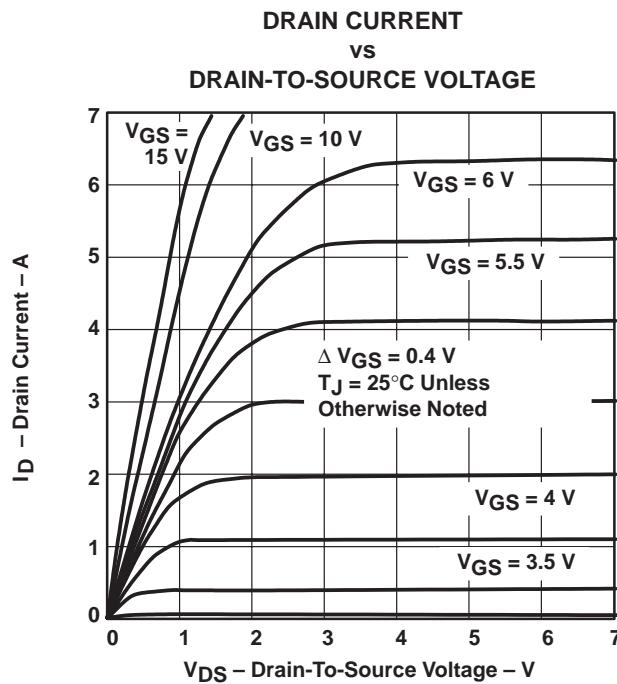


Figure 8

TYPICAL CHARACTERISTICS

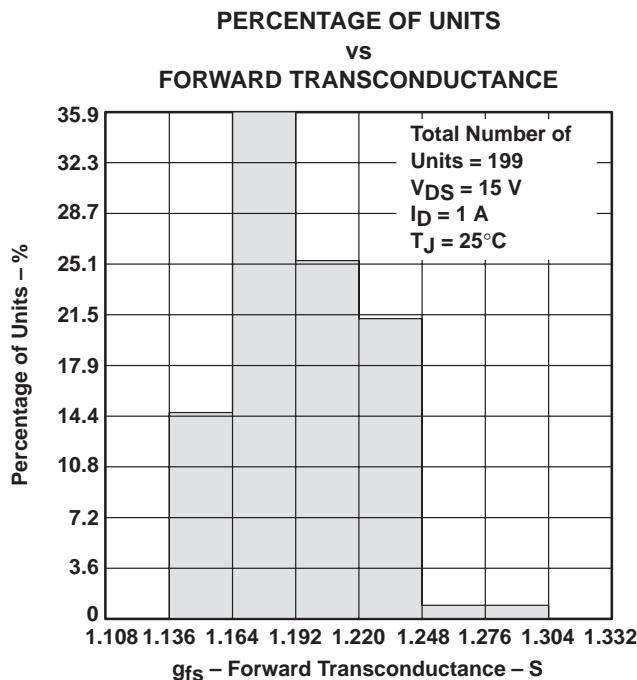


Figure 9

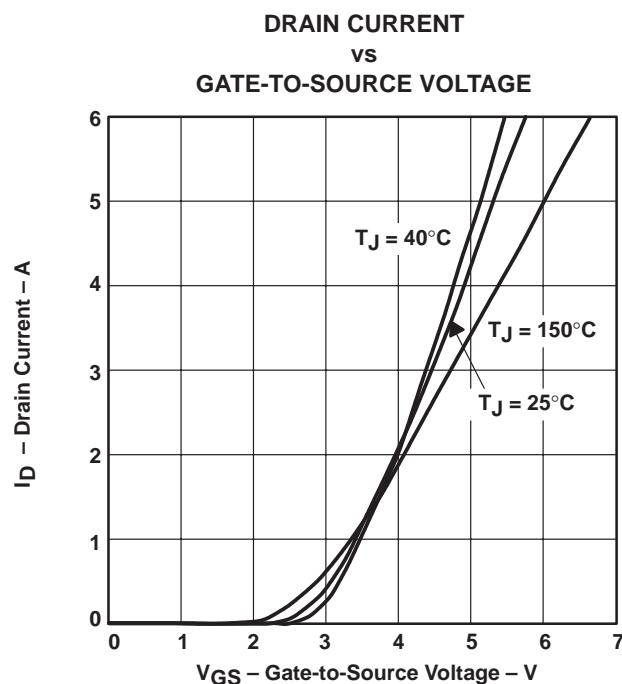


Figure 10

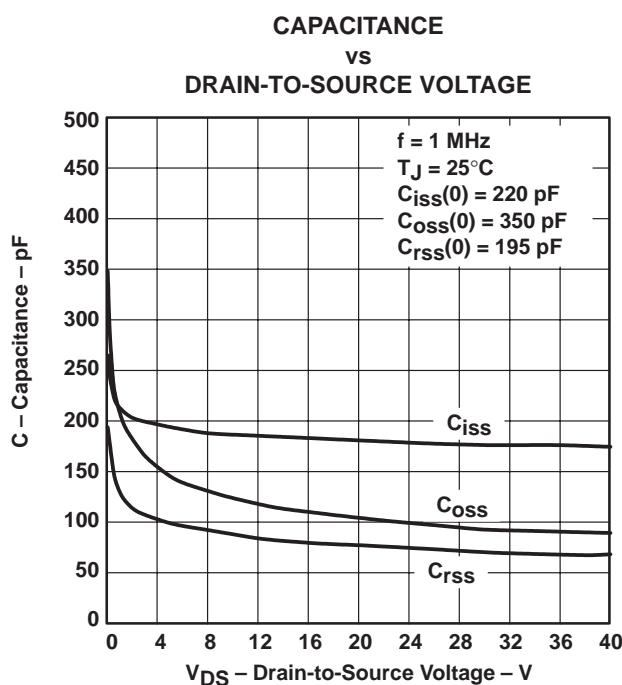


Figure 11

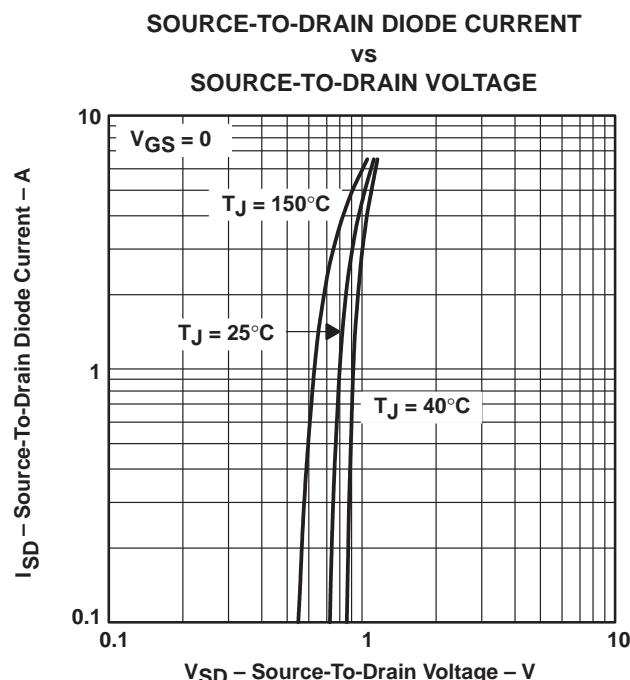


Figure 12

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4-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

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TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

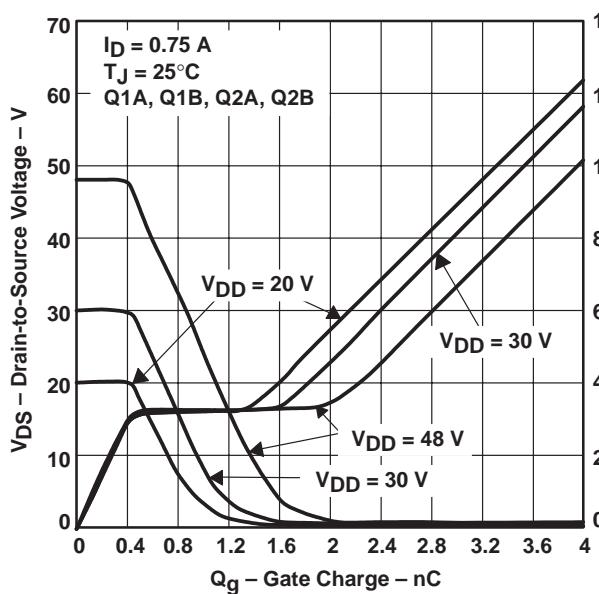


Figure 13

REVERSE RECOVERY TIME
vs
REVERSE di/dt

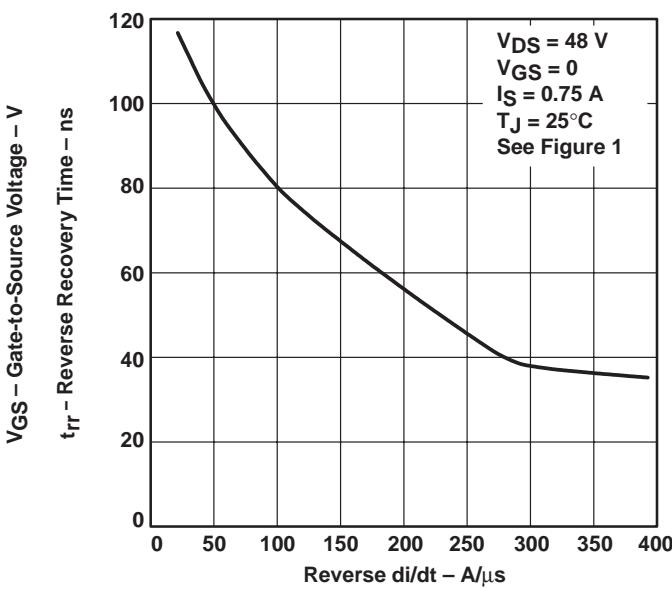


Figure 14

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE
INFINITE HEATSINK

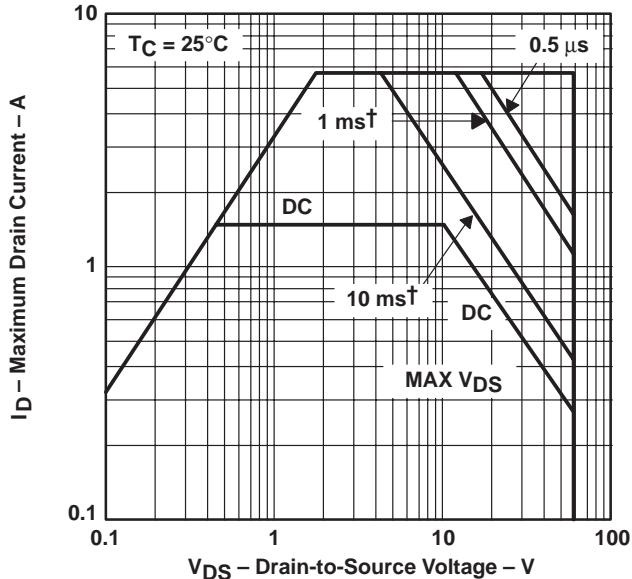


Figure 15

MAXIMUM PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

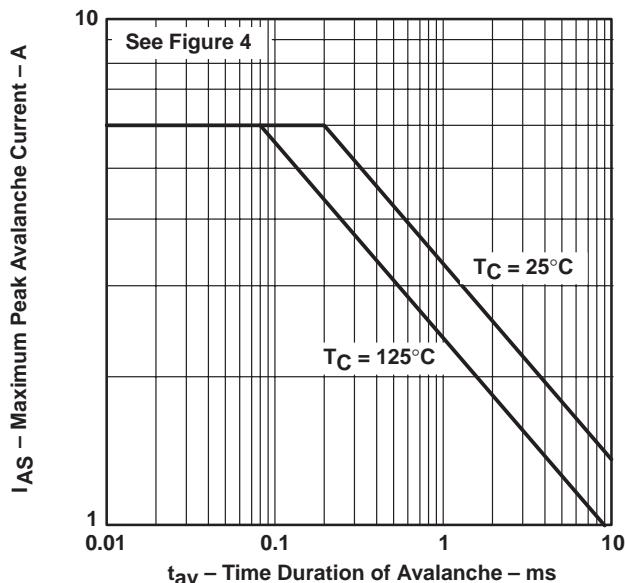
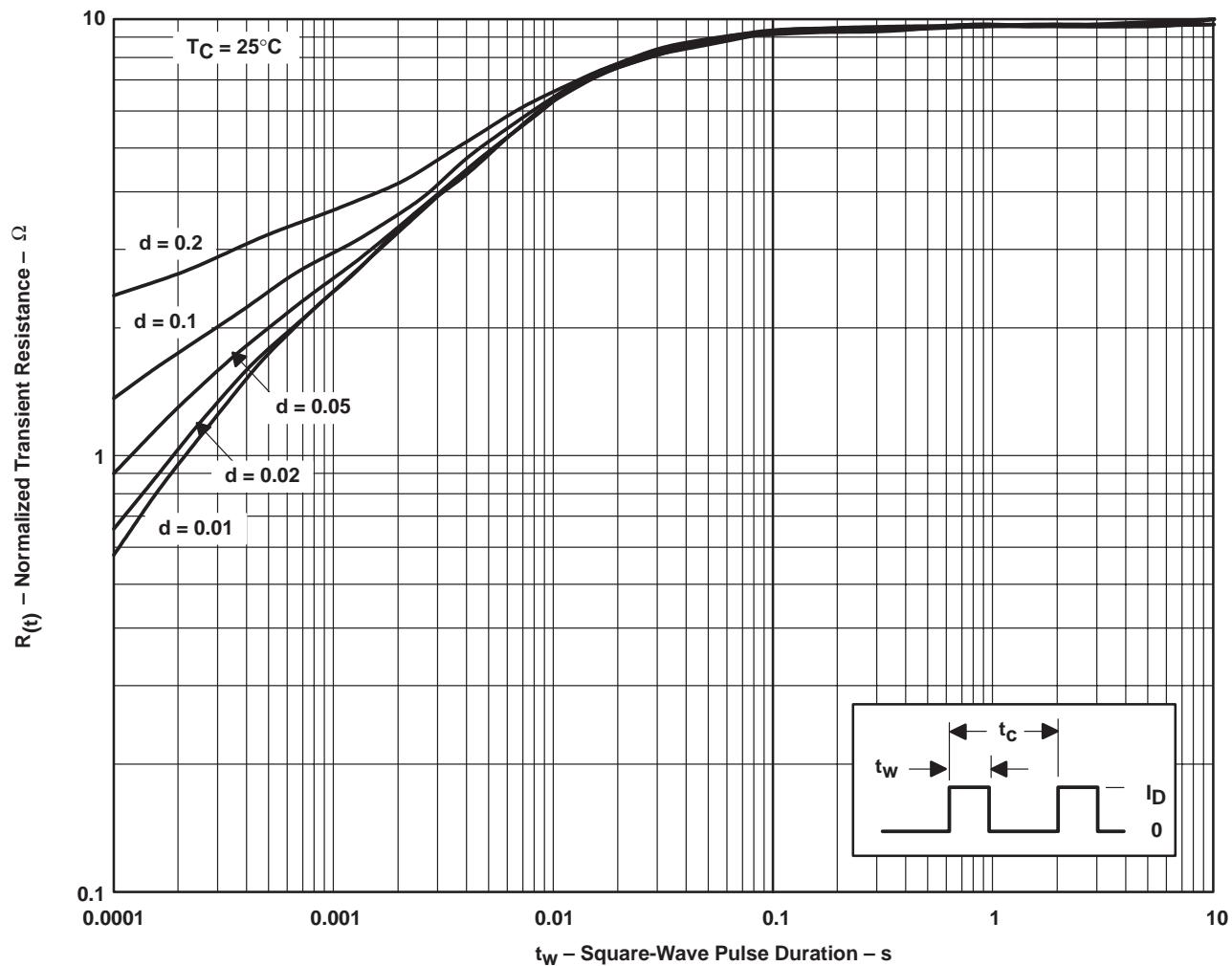


Figure 16

THERMAL INFORMATION

**NORMALIZED TRANSIENT RESISTANCE
vs
SQUARE-WAVE PULSE DURATION**



† Package mounted in intimate contact with infinite heat sink.

NOTE A: $Z_{\theta,JC}(t) = r(t) R_{\theta,JC}$

t_w = pulse duration

t_c = cycle time

d = duty cycle = t_w/t_c

Figure 17

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPIC2401KTA	OBsolete	PFM	KTA	9		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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