LXT361

Integrated T1/E1 LH/SH Transceiver for DS1/DSX-1 or PRI Applications

Datasheet

Applications

- ISDN PRI
- CSU/NTU interface to T1/E1 Service
- Wireless Base Station interface
- T1/E1 LAN/WAN bridge/routers
- T1/E1 Mux; Channel Banks
- Digital Loop Carrier - Subscriber Carrier Systems

Product Features

- Fully integrated transceiver for Long or Short-Haul T1, or E1 interfaces
- Crystal-less digital jitter attenuation
  - —Select either transmit or receive path
  - —No crystal or high speed external clock required
- Meets or exceeds specifications in ANSI T1.102, T1.403 and T1.408; ITU I.431, G.703, G.736, G.775 and G.823; ETSI 300-166 and 300-233; and AT&T Pub 62411
- Supports 75 Ω (E1 coax), 100 Ω (T1 twisted-pair) and 120 Ω (E1 twisted-pair) applications
- Selectable receiver sensitivity – fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or 0 to 36 dB @ 772 kHz and 0 to 43 dB @ 1024 kHz
- Five Pulse Equalization Settings for T1 Short-Haul applications
- Four Line Build-Outs for T1 Long-Haul applications from 0 dB to -22.5 dB
- Transmit/receive performance monitors with Driver Fail Monitor Open and Loss Of Signal (lOS) outputs
- Selectable unipolar or bipolar data I/O and B8ZS/HDB3 encoding/decoding
- Line attenuation indication output in 2.9 dB steps
- QRSS generator/detector for testing or monitoring
- Output short circuit current limit protection
- Local, remote, and analog loopback, plus in-band network loopback code generation and detection
- Intel/Motorola compatible 8-bit parallel interface for microprocessor control
- Available in 28-pin PLCC, 44-pin PQFP and 44-pin LQFP packages

As of January 15, 2001, this document replaces the Level One document known as *LXT361 — Integrated T1/E1 LH/SH Transceiver for DS1/DSX-1 or PRI Applications*.

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04-Jan-2006

Datasheet

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Revision History

Revision	Date	Description
002	04-Jan-2006	Modified Figure 1 “LXT351 Block Diagram” on page 7. Added RoHS information as follows: • Section 6.1, “Top Label Markings” on page 47. • Section 7.0, “Product Ordering Information” on page 48.
001	Jan 2001	Initial release.

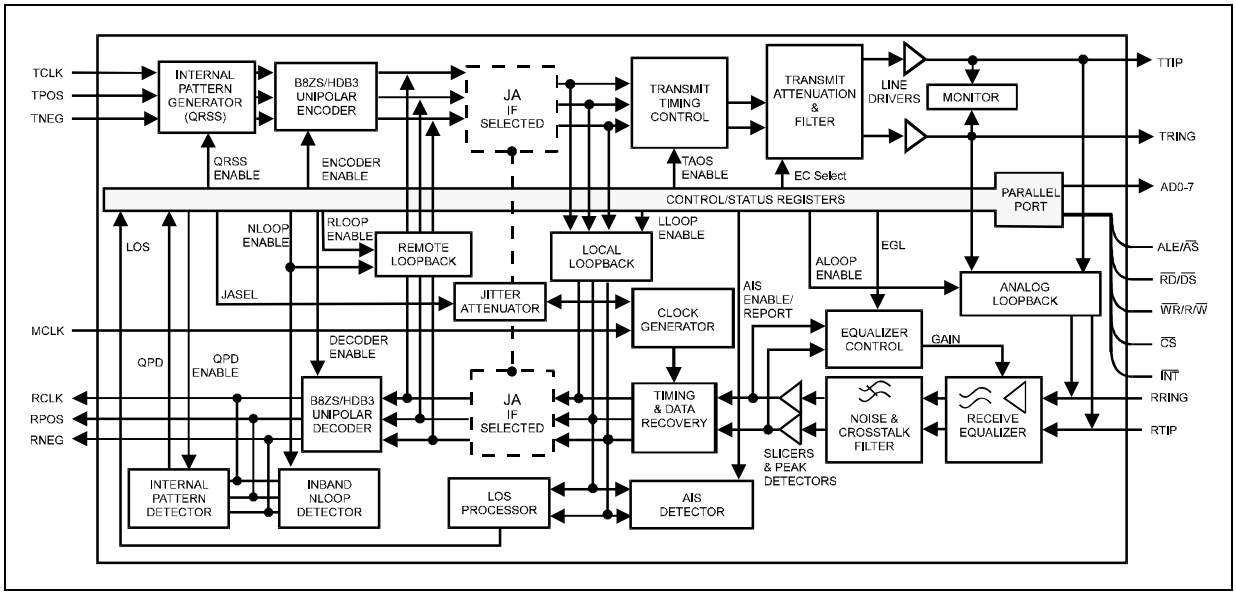
1.0 General Description

The LXT361 is a fully integrated, combination transceiver for T1/E1 ISDN Primary Rate Interface (ISDN PRI) and general T1/E1 Long and Short Hual applications. The device operates over 0.63 mm (22 AWG) twisted-pair cables for 0 to 2 km (6 kft) and offers Line Build Outs (LBO) and pulse equalization settings for all T1 and E1 Line Interface Unit (LIU) applications.

The LXT361 features an Intel or Motorola compatible parallel port for microprocessor control. The LXT361 incorporates advanced crystal-less digital jitter attenuation in either the transmit or receive data path starting at 3 Hz. B8ZS/HDB3 encoding/decoding and unipolar or bipolar data I/O are available. The LIU provides loss of signal monitoring and a variety of diagnostic loopback modes.

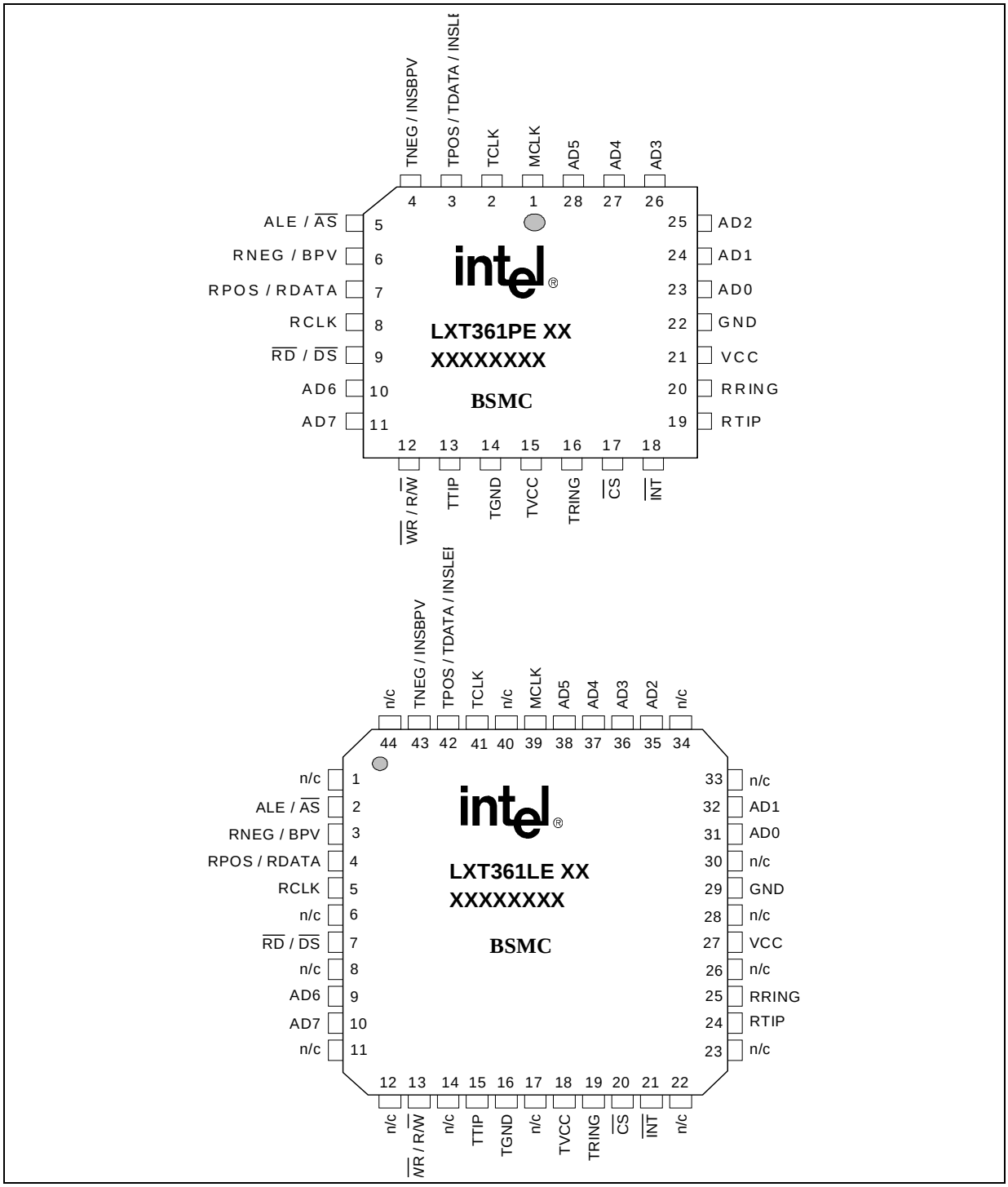
The parallel port is ideal for applications with multiple T1/E1 interfaces.

Figure 1. LXT361 Block Diagram



2.0 Pin Assignments and Signal Descriptions

Figure 2. LXT361 Pin Assignments and Markings



2.1 Mode Dependent Signals

As shown in Figure 2, the LXT361 has several pins that change function (and signal name) according to the selected mode(s) of operation. These pins, associated signal names, and operating modes are summarized in Table 1 and Table 2. LXT361 signals are described in Table 3.

Table 1. LXT361 Clock and Data Pin Assignments by Mode[1]

Pin #		External Data Modes		QRSS Modes	
PLCC	QFP	Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
16	19	TRING			
19	24	RTIP			
20	25	RRING			

1. Data pins change based on whether external data or internal QRSS mode is active.

Table 2. LXT361 Processor Interface Pins

Pin #		Address/Data Bus Type		Pin #		Address/Data Bus Type	
PLCC	QFP	Intel	Motorola	PLCC	QFP	Intel	Motorola
5	2	ALE	$\overline{AS}$	25	35	AD2	
9	7	$\overline{RD}$	$\overline{DS}$	26	36	AD3	
12	13	$\overline{WR}$	R/$\overline{W}$	27	37	AD4	
17	20	$\overline{CS}$		28	38	AD5	
18	21	$\overline{INT}$		10	9	AD6	
23	31	AD0		11	10	AD7	
24	32	AD1		-	-	-	

Table 3. LXT361 Signal Descriptions

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
1	39	MCLK	DI	**Master Clock**. External, independent clock signal required to generate internal clocks. For T1 applications, a 1.544 MHz clock is required; for E1, a 2.048 MHz clock. MCLK must be jitter-free and have an accuracy better than ± 50 ppm with a typical duty cycle of 50%. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2	41	TCLK	DI	**Transmit Clock**. For T1 applications, a 1.544 MHz clock is required; for E1, a 2.048 MHz clock. The transceiver samples TPOS and TNEG on the **falling edge** of TCLK (or MCLK, if TCLK is not present).
3 4	42 43	TPOS/TDATA/ INSLER TNEG/INSBPV	DI DI	**BIPOLAR MODES:** **Transmit – Positive and Negative**. TPOS and TNEG are the positive and negative sides of a bipolar input pair. Data to be transmitted onto the twisted-pair line is input at these pins. TPOS/TNEG are sampled on the falling edge of TCLK (or MCLK, if TCLK is not present). **UNIPOLAR MODES:** **Transmit Data**. TDATA carries unipolar data to be transmitted onto the twisted-pair line and is sampled on the falling edge of TCLK. Transmit Insert Logic Error. In *QRSS mode*, a Low-to-High transition on INSLER inserts a logic error into the transmitted QRSS data pattern. The error follows the data flow of the active loopback mode. The LXT361 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present). **Transmit Insert Bipolar Violation**. INSBPV is sampled on the falling edge of TCLK (or MCLK, if TCLK is not present) to control Bipolar Violation (BPV) insertions in the transmit data stream. A Low-to-High transition is required to insert each BPV. In ***QRSS mode***, the BPV is inserted into the transmitted QRSS pattern.
5	2	ALE/$\overline{AS}$	DI	**Address Latch Enable.** Connect to ALE signal of Intel microprocessor **Address Strobe** Connect to $\overline{AS}$ signal of Motorola microprocessor. Note that leaving this pin floating forces all output pins to a high impedance state.
6 7	3 4	RNEG/BPV RPOS/RDATA	DO DO	**BIPOLAR MODES:** **Receive – Negative and Positive**. RPOS and RNEG are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS are Non-Return-to-Zero (NRZ). The PLCKE bit in register CR3 selects the RCLK clock edge when RPOS /RNEG are stable and valid. **UNIPOLAR MODES:** **Receive Bipolar Violation.** BPV goes High to indicate detection of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK. **Receive Data**. RDATA is the unipolar NRZ output of data recovered from the line interface. The PLCKE bit in register CR3 selects the RCLK clock edge when RDATA is stable and valid.
8	5	RCLK	DO	**Receive Recovered Clock**. The clock recovered from the line input signal is output on this pin. Under LOS conditions, there is a smooth transition from the RCLK signal (derived from the recovered data) to the MCLK signal at the RCLK pin.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.

Table 3. LXT361 Signal Descriptions (Continued)

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
9	7	$\overline{RD}/\overline{DS}$	DI	**Read.** On an Intel bus, driving $\overline{RD}$ Low commands a LXT361 register read operation. **Data Strobe.** On a Motorola bus, $\overline{DS}$ goes Low when data is being driven on the address/data bus. Data is valid on the rising edge of $\overline{DS}$.
10 11	9 10	AD6 AD7	DI/O	**Address/Data Bus 6 and 7.** Used with AD0 - AD5 to form the address/data bus. Conforms to Intel and Motorola multiplexed address/data bus specifications.
12	13	$\overline{WR}$ / R/$\overline{W}$	DI	**Write.** On an Intel bus, driving $\overline{WR}$ Low commands a LXT361 register write operation. **Read/Write.** On a Motorola bus, driving R/$\overline{W}$ High commands a LXT361 register read operation; driving it Low commands a write operation.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential driver output pair designed to drive a 50 - 200 Ω load. The transformer and line matching resistors should be selected to give the desired pulse height and return loss performance. See "Application Information" on page 32.
14	16	TGND	-	**Ground** return for the transmit driver power supply TVCC.
15	18	TVCC	-	**+5 VDC Power Supply** for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	$\overline{CS}$	DI	**Chip Select.** During a read or write operation, $\overline{CS}$ must remain Low. See Figure 16 and Figure 17 for timing requirements. In the case of a single processor controlling several chips, this line is used to select a specific transceiver.
18	21	$\overline{INT}$	DO	**Interrupt.** $\overline{INT}$ goes Low to flag the host when LOS, AIS, NLOOP, QRSS, DFMS or DFMO bits changes state, or when an elastic store overflow or underflow occurs. To identify the specific interrupt, read the Performance Status Register (PSR). To clear or mask an interrupt, write a one to the appropriate bit in the Interrupt Clear Register (ICR). To re-enable the interrupt, write a zero. $\overline{INT}$ is an **open drain output** that must be connected to VCC through a pull-up resistor.
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The Alternate Mark Inversion (AMI) signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock recovered from RTIP/RRING are output on the RPOS/RNEG (or RDATA in ***Unipolar mode***), and RCLK pins.
21	27	VCC	-	**+5 VDC Power Supply** for all circuits except the transmit drivers. Transmit drivers are supplied by TVCC.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.

Table 3. LXT361 Signal Descriptions (Continued)

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
22	29	GND	-	**Ground** return for VCC.
23 24 25 26 27 28	31 32 35 36 37 38	AD0 AD1 AD2 AD3 AD4 AD5	DI/O	**Address/Data Bus 0 - 5**. Used with AD6 and AD7 to form the address/ data bus. Conforms to Intel and Motorola multiplexed address/data bus specifications.
-	8, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, 44	n/c	-	**Not Connected**

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.

3.0 Functional Description

The LXT361 is a fully integrated, PCM transceiver for Long- or Short-Hual, 1.544 Mbps (T1) or 2.048 Mbps (E1) applications allowing full-duplex transmission of digital data over existing twisted-pair installations. The device interfaces with two twisted-pair lines (one pair each for transmit and receive) through standard pulse transformers and appropriate resistors.

The figure on the front page of this data sheet shows a block diagram of the LXT361. Control of the chip is via the 8-bit parallel microprocessor port. Stand-alone operation is not supported.

The LXT361 provides a high-precision, crystal-less Jitter Attenuator (JA). The user may place the JA in the transmit or receive path, or bypass it completely.

The transceiver meets or exceeds FCC, ANSI, and AT&T specifications for CSU and DSX-1 applications, as well as ITU and ETSI requirements for E1 ISDN PRI applications.

3.1 Initialization

During power up, the transceiver remains static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the Phase Lock Loops (PLL). The transceiver uses a reference clock to calibrate the PLLs: the transmitter reference is TCLK, and the receiver reference clock is MCLK. MCLK is mandatory for chip operation and must be independent, free running, and jitter free.

3.1.1 Reset Operation

A reset operation initializes the status and state machines for the LOS, AIS, NLOOP, and QRSS blocks. Writing a 1 to the bit CR2.RESET commands a reset which clears all registers to 0. Allow 32 ms for the device to settle.

3.2 Transmitter

3.2.1 Transmit Digital Data Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs. In Unipolar mode, the TDATA pin accepts unipolar data.

Input data may pass through either the Jitter Attenuator or B8ZS/HDB3 encoder or both. Setting CR1.ENCENB = 1 enables B8ZS/HDB3 encoding. With zero suppression enabled, Control Register #1 (CR1) bits EC1 through EC4 determine the coding scheme as listed in Table 8 on page 27.

TCLK supplies input synchronization. See the Figure 14 on page 41 for the transmit timing requirements for TCLK and the Master Clock (MCLK).

3.2.2 Transmit Monitoring

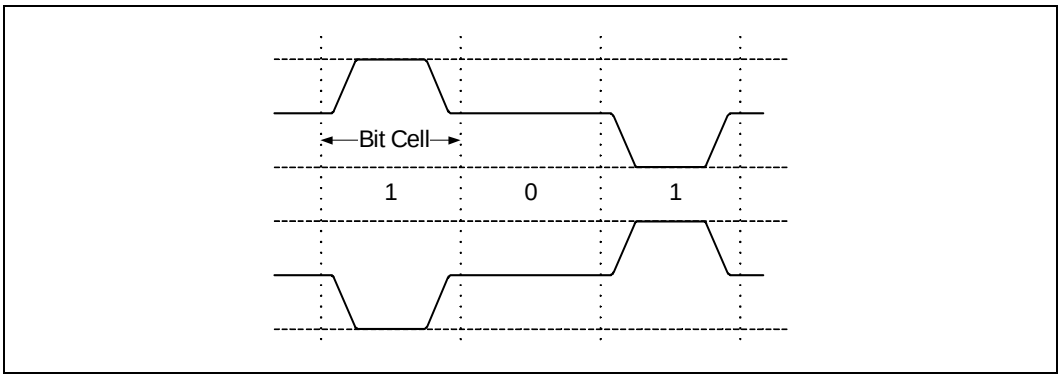
The transmitter includes a short circuit limiter that limits the current sourced into a low impedance load. The limiter automatically resets when the load current drops below the limit. The current is determined by the interface circuitry (total resistance on transmit side).

The Performance Status Register (PSR) flags open circuits in bit PSR.DFMO. A transition of DFMO can provide an interrupt, and its transition sets bit TSR.DFMO = 1. Writing a 1 in bit ICR.CDFMO clears the interrupt; leaving a 1 in the bit masks that interrupt.

3.2.3 Transmit Drivers

The transceiver transmits data as a 50% line code as shown in Figure 3. To reduce power consumption, the line driver is active only during transmission of marks, and is disabled during transmission of spaces. Biasing of the transmit DC level is on-chip.

Figure 3. 50% Duty Cycle Coding



3.2.4 Transmit Idle Mode

Transmit Idle mode allows multiple transceivers to be connected to a single line for redundant applications. When TCLK is not present, Transmit Idle mode becomes active, and TTIP and TRING change to the high impedance state. Remote loopback, Dual loopback, TAOS, or detection of Network Loop Up code in the receive direction, temporarily disable the high impedance state.

3.2.5 Transmit Pulse Shape

As shown in Table 8 on page 27, the transmitted pulse shape is established by bits EC1 through EC4 of Control Register #1 (CR1).

Shaped pulses meeting the various T1, DS1, DSX-1 and E1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The transceiver produces DSX-1 pulses for Short-Hual T1 applications (settings from 0 dB to +6.0 dB of cable), DS1 pulses for Long-Hual T1 applications (settings from 0 dB to -22.5 dB), and a G.703 pulse for E1 applications. Refer to the Test Specifications section for pulse mask specifications.

3.3 Receiver

A 1:1 transformer provides the interface to the twisted-pair line. Recovered data is output at RPOS/RNEG (RDATA in Unipolar mode), and the recovered clock is output at RCLK. Refer to Table 31 on page 42 for receiver timing specifications.

3.3.1 Receive Equalizer

The receive equalizer processes the signal received at RTIP and RRING. The equalizer gain is up to 43 dB in E1 Long-Hual applications and up to 36 dB in T1 applications. In T1 Long-Hual applications, bits EC1 through EC4 in Control Register #1 determine the maximum gain applied at the equalizer. When EC1 = 0, up to 36 dB of gain may be applied. When EC1 = 1, 26 dB is the gain limit to provide an increased noise margin in shorter loop operations.

3.3.2 Receive Data Recovery

The transceiver filters the equalized signal and applies it to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. The data slicers are set at 50% of the peak value to ensure optimum signal-to-noise performance.

After processing through the data slicers, the received signal goes to the data and timing recovery section, then to the B8ZS/HDB3 decoder (if selected) and to the receive monitor. The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411 and ITU G.823. See the “Test Specifications” section for details.

Recovered data is routed to the Loss of Signal (LOS) Monitor and through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. The jitter attenuator (JA) may be enabled or disabled in the receive data path or the transmit path. Received data may be routed to either the B8ZS or HDB3 decoder or neither. Finally, the device may send the digital data to the framer as either unipolar or bipolar data.

When transmitting unipolar data to the framer, the device reports reception of bipolar violations by driving the BPV pin High. During E1 operation, the device can report HDB3 code violations and Zero Substitution Violations on the BPV pin.

3.3.3 Receiver Monitor Mode

The LXT361 receive equalizer can be used in Monitor mode applications. Monitor mode applications require 20 dB to 30 dB resistive attenuation of the signal, plus a small amount of cable attenuation (less than 6 dB). Setting bit CR3.EQZMON = 1 configures the device to operate in Monitor mode. The device must be in T1/E1 Long-Hual receiver mode (set bits CR1.EC4:1 = 0xx0 or 1001 or 1010) for Monitor mode.

In Monitor mode, the receive equalizer will handle signals attenuated resistively by 20 to 30 dB, along with 0 to 6 dB of cable attenuation for both E1 and T1 applications.

3.4 Jitter Attenuation

A Jitter Attenuation Loop (JAL) with an Elastic Store (ES) provides jitter attenuation as shown in the Test Specifications section. The JAL requires no special circuitry, such as an external quartz crystal or high-frequency clock (higher than the line rate). Its timing reference is MCLK.

Bit CR1.JASEL0 enables or disables the JA circuit. With bit CR1.JASEL0 = 1, bit CR1.JASEL1 controls the JA circuit placement (see Table 7 on page 27). The ES can be either a 32 x 2-bit or 64 x 2-bit register depending on the value of bit CR3.ES64 (see Table 10 on page 28.)

The device clocks data into the ES using either TCLK or RCLK depending on whether the JA circuitry is in the transmit or receive data path, respectively. Data is shifted out of the elastic store using the dejittered clock from the JAL. When the FIFO is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^{1}/_{8}$ of a bit period. The ES produces an average delay of 16 bits (or 32 bits, with the 64-bit ES option selected) in the associated data path. When the Jitter Attenuator is in the receive path, the output RCLK transitions smoothly to MCLK in the event of a LOS condition.

The Transition Status Register bits TSR.ESOVR and TSR.ESUNF indicate an elastic store overflow or underflow, respectively. Note that these are sticky bits that once set to 1, remain set until the host reads the register. The ES can also provide a maskable interrupt on either overflow or underflow.

3.5 Diagnostic Mode Operation

The LXT361 offers multiple diagnostic modes as listed in Table 4. The diagnostic modes are selected by setting the appropriate register bits as described in the following paragraphs.

3.5.1 Loopback Modes

3.5.1.1 Local Loopback

See Figure 4 and Figure 5. Local loopback is selected by setting CR2.ELLOOP to 1. LLOOP inhibits the receiver circuits. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the jitter attenuator (if enabled) and show up at RCLK and RPOS/RNEG or RDATA. Note that during LLOOP, the JASEL input is strictly an Enable/Disable control; it does not affect the placement of the JAL. If JA is enabled, it is active in the loopback circuit. If JA is bypassed, it is not active in the loopback circuit.

The transmitter circuits are unaffected by LLOOP. LXT361 transmits the TPOS/TNEG or TDATA inputs (or a stream of 1s if TAOS is asserted) normally. When used in this mode, the transceiver can function as a stand-alone jitter attenuator.

Table 4. Diagnostic Mode Summary

Diagnostic Mode	Interrupt Maskable
Loopback Modes	
Local Loopback (LLOOP)	No
Analog Loopback (ALOOP)	No

Table 4. Diagnostic Mode Summary

Diagnostic Mode	Interrupt Maskable
Remote Loopback (RLOOP)	No
In-band Network Loopback (NLOOP)	Yes
Dual Loopback (DLOOP)	No
Internal Data Pattern Generation and Detection	
Transmit All Ones (TAOS)	No
Quasi-Random Signal Source (QRSS)	Yes
In-band Loop Up/Down Code Generator	No
Error Insertion and Detection	
Bipolar Violation Insertion (INSBPV)	No
Logic Error Insertion (INSLER)	No
Bipolar Violation Detection (BPV)	No
HDB3 Code Violation Detection (CODEV)	No
HDB3 Zero violation Detection (ZEROV)	No
Alarm Condition Monitoring	
Receive Loss of Signal (LOS) Monitoring	Yes
Receive Alarm Indication Signal (AIS) Monitoring	Yes
Transmit Driver Failure Monitoring Open (DFMO)	Yes
Elastic Store Overflow and Underflow Monitoring	Yes
Other Diagnostic Reports	
Receive Line Attenuation Indicator (LATN)	No
Built-In Self Test (BIST)	Yes

Figure 4. TAOS with LLOOP

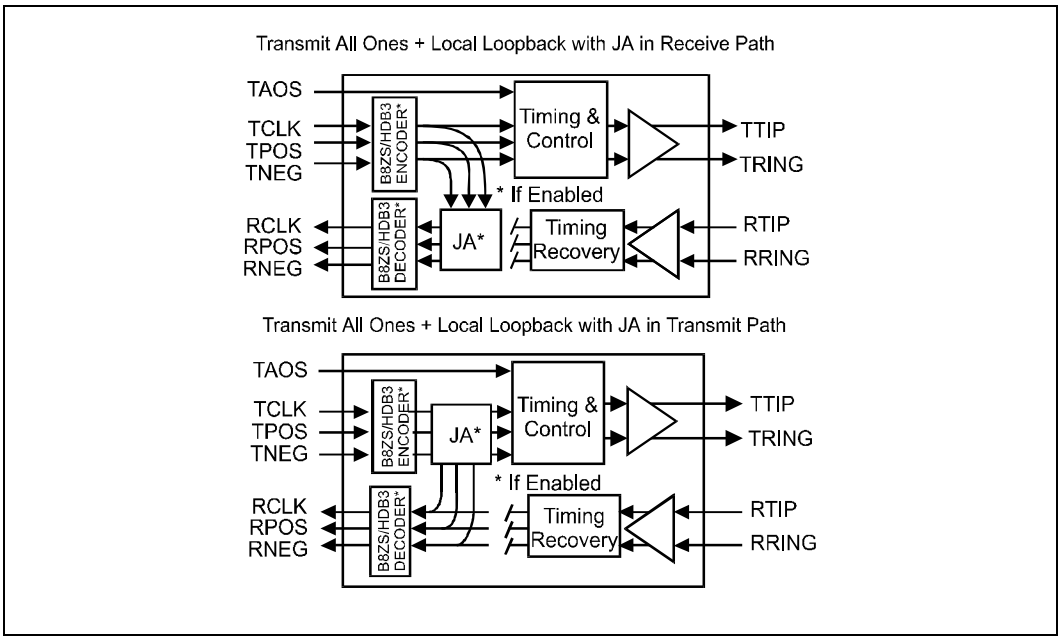
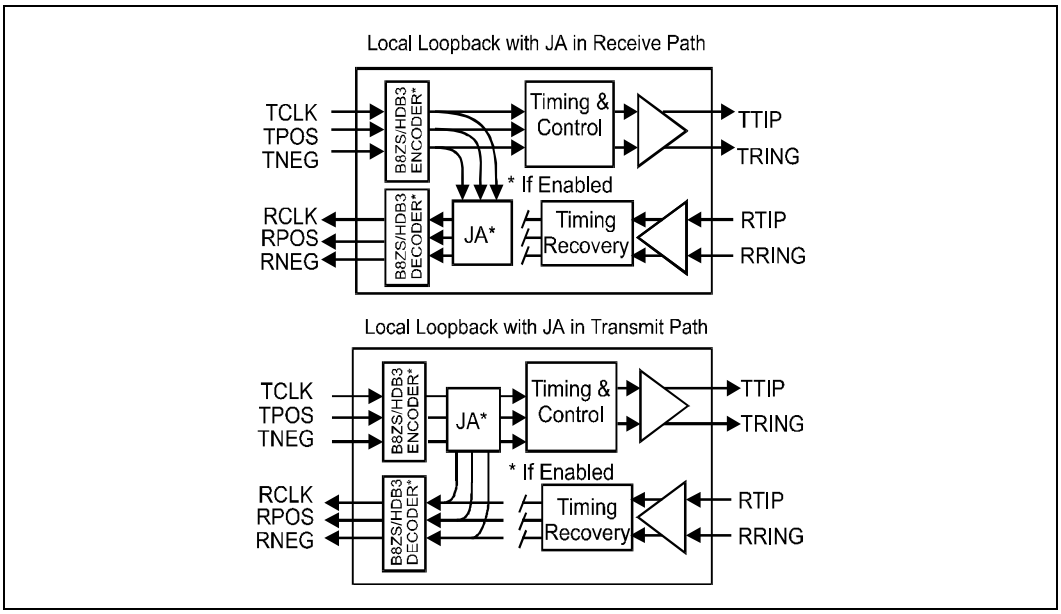


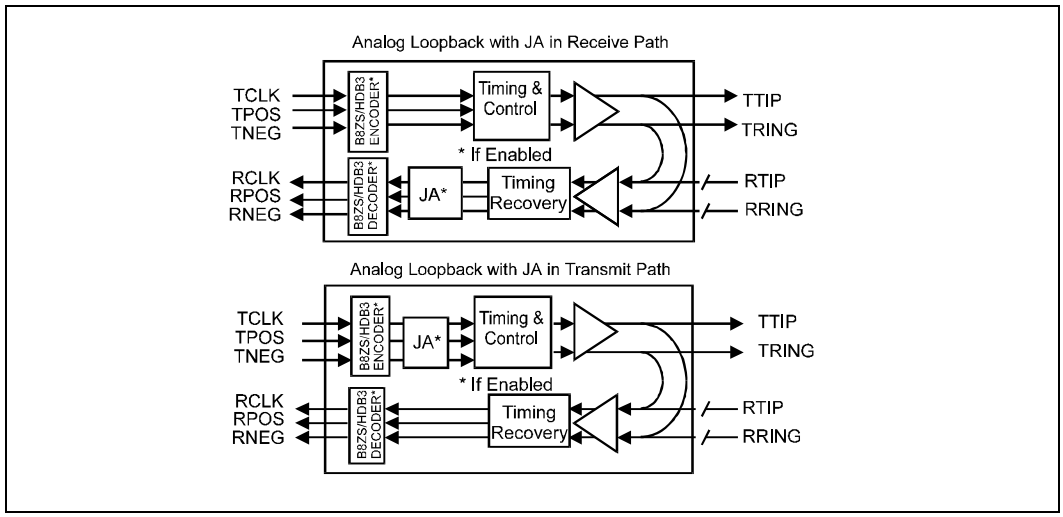
Figure 5. Local Loopback



3.5.1.2 Analog Loopback

See Figure 6. Analog loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING inputs from the line and routes the transmit outputs back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. Writing a 1 to bit CR2.EALOOP enables the ALOOP mode. Note that ALOOP will override all other loopback modes.

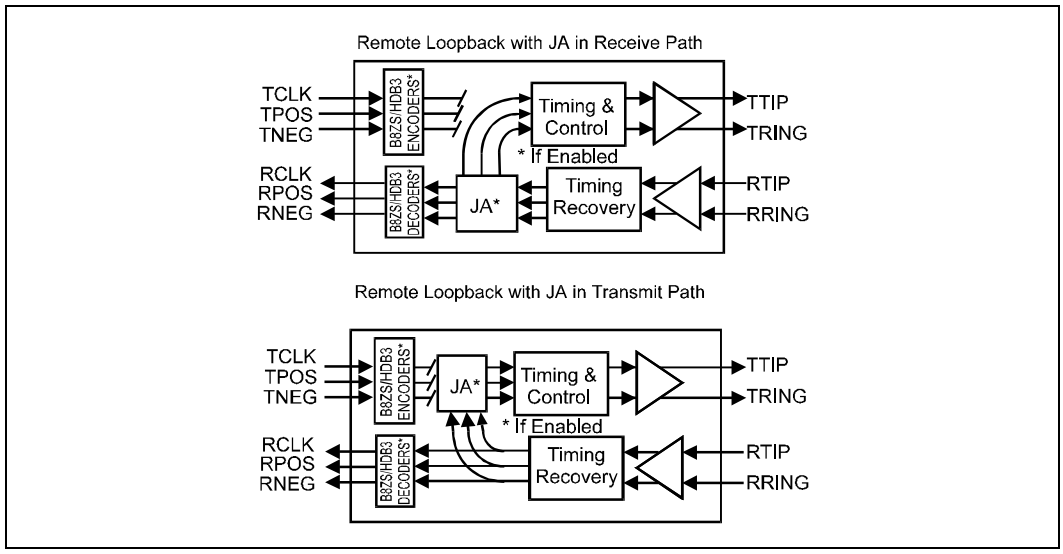
Figure 6. Analog Loopback



3.5.1.3 Remote Loopback

See Figure 7. In Remote loopback (RLOOP) mode, the device ignores the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA), and bypasses the in-line encoders/decoders. The RPOS/RNEG or RDATA outputs loop back through the transmit circuits to TTIP and TRING at the RCLK frequency. The RLOOP command does not affect the receiver circuits which continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. RLOOP is selected by writing a 1 to bit CR2.ERLOOP.

Figure 7. Remote Loopback



3.5.1.4 Network Loopback

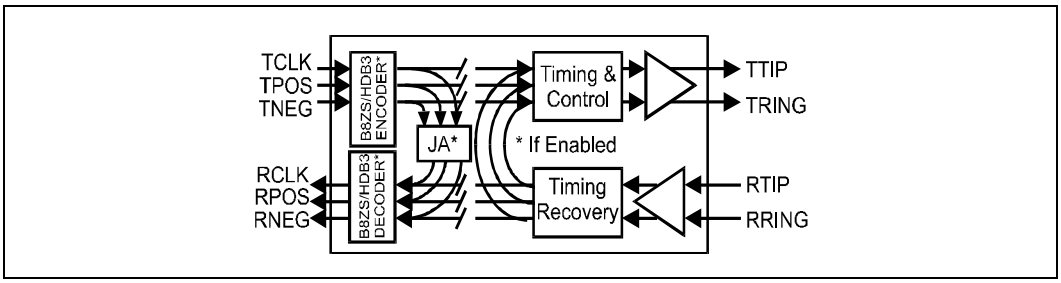
Network loopback (NLOOP) can be initiated only when the Network loopback detect function is enabled. Writing a 1 to CR2.ENLOOP enables NLOOP detection.

With NLOOP detection enabled, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP. The device responds to both framed and unframed NLOOP patterns. Once NLOOP detection is enabled at the chip and activated by the appropriate data pattern, it is identical to Remote loopback (RLOOP). NLOOP is disabled by receiving the 001 pattern for five seconds, or by activating RLOOP or ALOOP, or by disabling NLOOP detection. The device goes into Dual loopback mode (DLOOP) in the case where it detects both the NLOOP and LLOOP functions.

3.5.1.5 Dual Loopback

See Figure 8. To select Dual loopback (DLOOP) set bits CR2.ERLOOP and CR2.ELLOOP to 1. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the Jitter Attenuator (unless disabled) to RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the twisted-pair line loop back through the transmit circuits to TTIP and TRING without jitter attenuation.

Figure 8. Dual Loopback

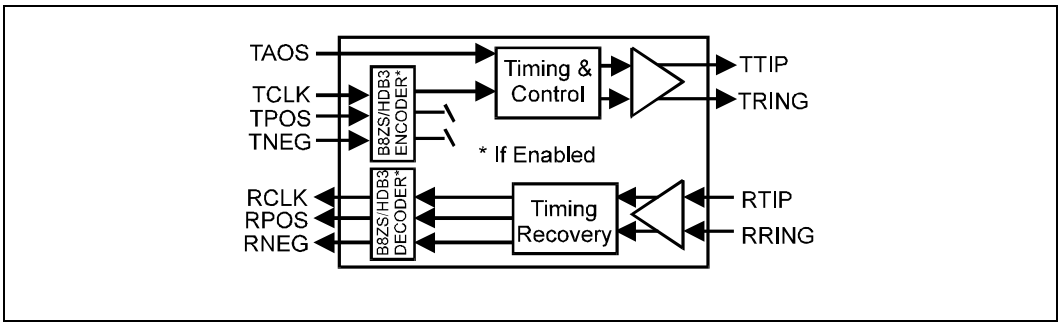


3.5.2 Internal Pattern Generation and Detection

3.5.2.1 Transmit All Ones

See Figure 9. In Transmit All Ones (TAOS) mode the transceiver ignores the TPOS and TNEG inputs and transmits a continuous stream of 1s at the TCLK frequency. (With no TCLK, the TAOS output clock is MCLK.) This can be used as the Alarm Indication Signal (AIS–also called the Blue Alarm). TAOS is commanded by writing a 1 to bit CR2.ETAOS. Both TAOS and Local loopback can occur simultaneously as shown in Figure 4, however, Remote loopback inhibits TAOS. When both TAOS and LLOOP are active, TCLK and TPOS/TNEG loop back to RCLK and RPOS/RNEG through the jitter attenuator (if enabled), and an all ones pattern goes to TTIP/TRING.

Figure 9. TAOS Data Path

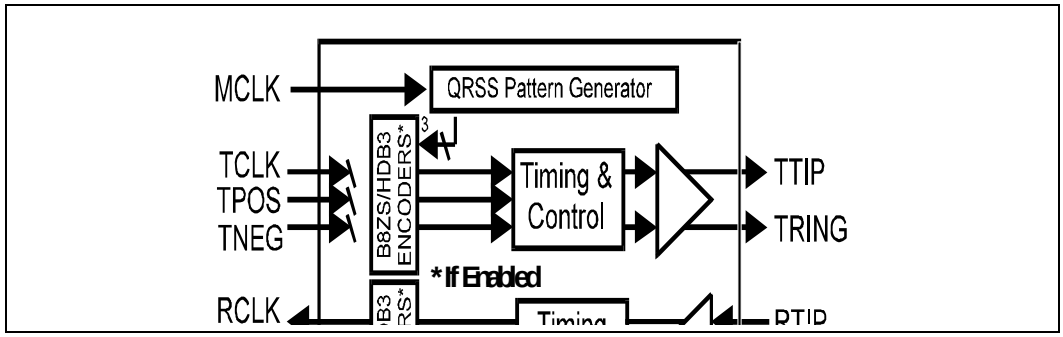


3.5.2.2 Quasi-Random Signal Source (QRSS)

See Figure 10. For T1 operation, the Quasi-Random Signal Source (QRSS) is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. For E1 operation, QRSS is 2^{15}-1 PRBS with inverted output. Setting bits CR2.EPAT0 = 0 and CR2.EPAT1 = 1 enables this function.

The QRSS pattern is normally locked to TCLK; but if there is no TCLK, MCLK is the clock source. Bellcore Pub 62411 defines the T1 QRSS transmit format and ITU G.703 defines the E1 format.

Figure 10. QRSS Mode



With QRSS transmission enabled, it is possible to insert a logic error into the transmit data stream by causing a Low-to-High transition on INSLER. However, if no logic or bit errors are to be inserted into the QRSS pattern, INSLER must remain Low. Logic Error insertion waits until the next bit if the current bit is “jammed”. When there are more than 14 consecutive 0s, the output is jammed to a 1.

Furthermore, a bipolar violation in the QRSS pattern is possible by causing a Low-to-High transition on the INSBPV pin, regardless of whether the device is in Bipolar or Unipolar mode.

Choosing QRSS mode also enables the QRSS Pattern Detection in the receive path. The QRSS pattern is synchronized when there are fewer than four errors in 128 bits. The PSR.QRSS bit provides an indication of QRSS pattern synchronization. This bit goes Low when no QRSS pattern detected (*i.e.*, when there are more than four errors in 128 bits). The TQRSS bit in the Transition Status Register indicates that QRSS status has changed since the last QRSS Interrupt Clear command.

The LXT361 can generate an interrupt to indicate that QRSS detection has occurred, or that synchronization is lost. The interrupt is enabled when ICR.CQRSS = 0.

3.5.2.3 In-Band Network Loop Up or Down Code Generator

The LXT361 can transmit in-band Network Loop Up or Loop Down code. The Loop Up code is 00001; Loop Down code is 001. A Loop Up code transmission occurs when Control Register #2 bits EPAT0 = 1 and EPAT1 = 0. A Loop Down code transmission requires that both EPAT0 and EPAT1 = 1.

With this mode enabled, logic errors and bipolar violations can be inserted into the transmit data stream. Inserting a logic error requires a Low-to-High transition in INSLER (pin 3). If no logic or bit errors are to be inserted, INSLER must remain Low. Inserting a bipolar violation requires a Low-to-High transition on the INSBPV pin, regardless of unipolar or bipolar operation.

3.5.3 Error Insertion and Detection

3.5.3.1 Bipolar Violation Insertion (INSBPV)

Bipolar violation insertion is available In Unipolar mode. Choosing Unipolar mode configures the INSBPV pin. To insert bipolar violation (BPV), a Low-to-High transition on the INSBPV is required. Sampling occurs on the falling edge of TCLK. When INSBPV goes High a BPV is inserted on the next available mark except in the four following situations:

- Zero suppression (HDB3 or B8ZS) is not violated
- If LLOOP and TAOS are both active, the BPV is looped back to RNEG/BPV indicator and the line driver transmits all ones with no violation
- BPV insertion is disabled with RLOOP active
- BPV insertion is disabled when NLOOP is active

With the LXT361 configured to transmit internally generated data patterns (QRSS or NLOOP), a BPV can be inserted into the transmit pattern regardless of whether the device is in the Unipolar or Bipolar mode of operation.

3.5.3.2 Logic Error Insertion (INSLER)

When configured to transmit internally generated data patterns (QRSS or NLOOP Up/Down codes), a logic error is inserted into the transmit data pattern when the INSLER pin transitions Low-to-High. Note that in QRSS mode, there is no logic error insertion on a jammed bit (i.e., a bit forced to one to suppress transmission of more than 14 consecutive zeros). The transceiver routes data patterns the same way it routes data applied to TPOS/TNEG. Therefore, the inserted logic error will follow the data flow path of the active loopback mode.

3.5.3.3 Bipolar Violation Detection (BPV)

When the internal encoders/decoders are disabled or when configured in Unipolar mode, bipolar violations are reported at the BPV pin. BPV goes High for a full clock cycle to indicate receipt of a BPV. When the encoders/decoders are enabled, the LXT361 does not report bipolar violations due to the line coding scheme.

3.5.3.4 HDB3 Code Violation Detection (CODEV)

An HDB3 code violation (CODEV) occurs when two consecutive bipolar violations of the same polarity are received (refer to ITU O.161). When CODEV detection is enabled, the BPV pin goes High for a full RCLK cycle to report a CODEV violation. Note that bipolar violations and zero substitution violations will also be reported on the BPV pin if these options are enabled.

HDB3 code violation detection is enabled when the HDB3 encoders/decoders are enabled. This requires that CR1.ENCENB = 1, also CR1.EC4:1 = 100x or 1010, which establishes E1 operation. To select CODEV detection, set bit CR4.CODEV = 1.

3.5.3.5 HDB3 Zero Substitution Violation Detection (ZEROV)

An HDB3 ZEROV is the receipt of four or more consecutive zeros. This does not occur with correctly encoded HDB3 data unless there are transmission errors. The BPV pin goes High for a full RCLK cycle to report a ZEROV. Note that when ZEROV detection enabled, the BPV pin will also indicate received BPVs and CODEVs, if these detection options are enabled.

ZEROV detection is enabled when the HDB3 encoders/decoders are enabled. This requires CR1.ENCENB = 1, also CR1.EC4:1 = 100x or 1010, which establishes E1 operation. To select ZEROV detection, set bit CR4.ZEROV = 1.

3.5.4 Alarm Condition Monitoring

3.5.4.1 Loss of Signal

The LXT361 Loss of Signal (LOS) monitor function is compatible with ITU G.775 and ETSI 300233. The receiver LOS monitor loads a digital counter at the RCLK frequency. The count increments with each received 0 and the counter resets to 0 on receipt of a 1. When the count reaches “n” 0s, bit PSR.LOS is set to ‘1’, and the MCLK replaces the recovered clock at the RCLK output in a smooth transition. For T1 operations, the number of 0s, n = 175, and for E1 operations, n = 32. For both T1 and E1 operation, “n” can be set to 2048 by setting bit CR4.LOS2048 = 1.

For T1 operation, when the received signal has 12.5% 1s (16 marks in a sliding 128-bit period, with fewer than 100 consecutive 0s), bit PSR.LOS = 0 and the recovered clock replaces MCLK at the RCLK output in another smooth transition.

For E1 operation, the LOS condition is cleared when the received signal has 12.5% 1s density (four 1s in a sliding 32-bit window with fewer than 16 consecutive 0s). In E1 operation, the out-of-LOS criterion can be modified from 12.5% marks density to 32 consecutive marks by setting bit CR4.COL32CM = 1.

During LOS, the device sends received data to the RPOS/RNEG pins (or RDATA in Unipolar mode). Bit PSR.LOS = 1 to indicate LOS condition, and can generate an interrupt to the host controller if so programmed.

3.5.4.2 Alarm Indication Signal Detection

The receiver detects an AIS pattern when it receives fewer than three 0s in any string of 2048 bits. The device clears the AIS condition when it receives three or more 0s in a string of 2048 bits.

The AIS bit in the Performance Status Register indicates AIS detection. Whenever the AIS status changes, bit TSR.TAIS =1. Unless masked, a change of AIS status generates an interrupt.

3.5.4.3 Driver Failure Open Mode

The DFM Open (DFMO) bit is available in the Performance Status Register to indicate an open condition on the lines. DFMO can generate an $\overline{\text{INT}}$ to the host controller. The Transition Status Register bit TDFMO indicates a transition in the status of the bit. Writing a 1 to ICR.CDFMO will clear or mask the interrupt.

3.5.4.4 Elastic Store Overflow/Underflow

When the bit count in the Elastic Store (ES) is within two bits of overflowing or underflowing the ES adjusts the output clock by $^{1}/_{8}$ of a bit period. The ES provides an indication of overflow and underflow via bits TRS.ESOVR and TSR.ESUNF. These are sticky bits and will stay set to 1 until the host controller reads the register. These interrupts can be cleared or masked by writing a 1 to the bits ICR.CESO and ICR.CESU, respectively.

3.5.5 Other Diagnostic Reports

3.5.5.1 Receive Line Attenuation Indication

The Equalizer Status Register (ESR) provides an approximation of the line attenuation encountered by the device. The four most significant bits of the register (ESR.LATN7:4) indicate line attenuation in approximately 2.9 dB steps for both T1 and E1 operation of the receive equalizer. For instance, if ESR.LATN7:4 is 10 (decimal), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB x 10) of cable loss.

3.5.5.2 Built-In Self Test

LXT361 provides a Built-In Self Test (BIST) capability. The BIST exercises the internal circuits by providing an internal QRSS pattern, running it through the encoders and the transmit drivers then looping it back through the receive equalizer, jitter attenuator and decoders to the QRSS pattern detection circuitry. If all the blocks in this data path function correctly, the receive pattern detector locks onto the pattern. It then pulls $\overline{\text{INT}}$ Low and sets the following bits:

- TSR.TQRSS = 1
- PSR.QRSS = 1
- PSR.BIST = 1

Note that during BIST, the TPOS/TNEG inputs must remain at logic level = 0

The most reliable test will result when a separate TCLK and MCLK are applied and the Line Build-Out (LBO) is set to -22.5 dB (CR1.EC4:1 = 011x).

3.6 Parallel Microprocessor Interface

The LXT361 multiplexed address/data bus and timing/control signals are compatible with both the Intel and Motorola microprocessors. See Figure 16 and Figure 17 for the I/O timing diagram for each bus. The LXT361 detects and distinguishes between Intel and Motorola timing and then automatically selects the appropriate bus timing. The maximum recommended processor speed for an Intel device is 20 MHz; for a Motorola device, 16.78 MHz. See “Test Specifications” on page 36 for microprocessor interface timing details.

The LXT361 contains five read/write and three read-only registers for control and status purposes. Table 6 on page 26 is a summary of the registers. Table 7 through Table 15 identify and explain the function of the register bits.

3.6.1 Interrupt Handling

The LXT361 provides a latched interrupt output pin ($\overline{\text{INT}}$). When enabled, a change in any of the Performance Status Register bits will generate an interrupt. An interrupt can also be generated when the elastic store overflows (TSR.ESOVR) or underflows (TSR.ESUNF). When an interrupt occurs, the $\overline{\text{INT}}$ output pin is pulled Low. Note that the output stage of the $\overline{\text{INT}}$ pin has internal pull-down only. Therefore, each device that shares the $\overline{\text{INT}}$ line ***requires an external pull-up resistor***.

The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1 to the respective interrupt causing bit(s) in the Interrupt Clear Register (ICR). Leaving a 1 in any of the ICR bits masks that interrupt. To re-enable an interrupt bit, write a 0.

4.0 Register Definitions

The LXT361 contains five read/write and three read-only registers. Table 5 lists the LXT361 register addresses. Note that only bits A6 through A1 of the address byte are valid; the address decoder ignores bits A7 and A0. Table 6 identifies the name of each register bit. Table 7 through Table 15 describe the function of the bits in each register.

Note: upon power-up or reset, all registers are cleared to 0.

Table 5. Register Addresses

Register		Address[1] A7 - A0
Name	Abbr	
Control #1	CR1	x010000x
Control #2	CR2	x010001x
Control #3	CR3	x010010x
Interrupt Clear	ICR	x010011x
Transition Status	TSR	x010100x
Performance Status	PSR	x010101x
Equalizer Status	ESR	x010110x
Control #4	CR4	x010111x

1. x = don't care.

Table 6. Register and Bit Summary

Register			Bit							
Name		Type	7	6	5	4	3	2	1	0
Control #1	CR1	R/W	JASEL1	JASEL0	ENCENB	UNIENB	EC4	EC3	EC2	EC1
Control #2	CR2	R/W	RESET	EPAT1	EPAT0	ETAOS	ENLOOP	EALOOP	ELLOOP	ERLOOP
Control #3	CR3	R/W	JA6HZ	PCLKE	SBIST	EQZMON	reserved[1]	ES64	ESCEN	ESJAM
Interrupt Clear	ICR	R/W	CESU	CESO	CDFMO	*reserved*[2]	CQRSS	CAIS	CNLOOP	CLOS
Transition Status	TSR	R	ESUNF	ESOVR	TDFMO	reserved[1]	TQRSS	TAIS	TNLOOP	TLOS
Performance Status	PSR	R	reserved[1]	BIST	DFMO	reserved[1]	QRSS	AIS	NLOOP	LOS
Equalizer Status	ESR	R	LATN7	LATN6	LATN5	LATN4	reserved[1]	reserved[1]	reserved[1]	reserved[1]
Control #4	CR4	R/W	reserved[1]	reserved[1]	reserved[1]	reserved[1]	COL32CM	LOS2048	ZEROV	CODEV

1. In writable registers, bits labeled *reserved* should be set to 0 (except as in note 2 below) for normal operation and ignored in read only registers.
2. Write a 1 to this bit for normal operation.

Table 7. Control Register #1 Read/Write, Address (A7-A0) = x010000x

Bit	Name	Function	Jitter Attenuator		
			JASEL0	JASEL1	Position
0	EC1	Sets mode (T1 or E1) and equalizer (see Table 8 below for control codes).	1	0	Transmit
1	EC2		1	1	Receive
2	EC3		0	X	Disabled
3	EC4				
4	UNIENB	1 = Enable Unipolar I/O mode and allow insertion/detection of BPVs. 0 = Enable Bipolar I/O mode			
5	ENCENB	1 = Enable B8ZS/HDB3 encoders/decoders and force Unipolar I/O mode. 0 = Disable B8ZS/HDB3 encoders/decoders			
6	JASEL0	Select jitter attenuation circuitry position in data path or disables the JA. See right hand section of table for codes. ↗			
7	JASEL1				

Table 8. Equalizer Control Bit Settings

Control Register #1				Function	Pulse	Cable	Gain	Coding[2]
EC4	EC3	EC2	EC1[1]					
0	0	0	0	T1 Long Haul	0.0 dB pulse	100 Ω TP	36 dB	B8ZS
0	0	1	0	T1 Long Haul	-7.5 dB pulse	100 Ω TP	36 dB	B8ZS
0	1	0	0	T1 Long Haul	-15.0 dB pulse	100 Ω TP	36 dB	B8ZS
0	1	1	0	T1 Long Haul	-22.5 dB pulse	100 Ω TP	36 dB	B8ZS
0	0	0	1	T1 Long Haul	0.0 dB pulse	100 Ω TP	26 dB	B8ZS
0	0	1	1	T1 Long Haul	-7.5 dB pulse	100 Ω TP	26 dB	B8ZS
0	1	0	1	T1 Long Haul	-15.0 dB pulse	100 Ω TP	26 dB	B8ZS
0	1	1	1	T1 Long Haul	-22.5 dB pulse	100 Ω TP	26 dB	B8ZS
1	0	0	0	E1 Short Haul	ITU G.703	120 Ω TP/75 Ω Coax	12 dB	HDB3
1	0	0	1	E1 Long Haul	ITU G.703	120 Ω TP	43 dB	HDB3
1	0	1	0	E1 Long Haul	ITU G.703	120 Ω TP/75 Ω Coax	43 dB	HDB3
1	0	1	1	T1 Short Haul	0-133 ft / 0.6 dB	100 Ω TP	12 dB	B8ZS
1	1	0	0	T1 Short Haul	133-266 ft / 1.2 dB	100 Ω TP	12 dB	B8ZS
1	1	0	1	T1 Short Haul	266-399 ft / 1.8 dB	100 Ω TP	12 dB	B8ZS
1	1	1	0	T1 Short Haul	399-533 ft / 2.4 dB	100 Ω TP	12 dB	B8ZS
1	1	1	1	T1 Short Haul	533-655 ft / 3.0 dB	100 Ω TP	12 dB	B8ZS

1. EC1 sets the receive equalizer gain (EGL) during T1 Long-Hual operation.
2. When enabled.

Table 9. Control Register #2 Read/Write, Address (A7-A0) = x010001x

Bit	Name	Function	Pattern		
			EPAT0	EPAT1	Selected
0	ERLOOP[1]	1 = Enable Remote loopback mode 0 = Disable Remote loopback mode	0	0	Transmit TPOS/TNEG
1	ELLOOP[1]	1 = Enable Local loopback mode 0 = Disable Local loopback mode	0	1	Detect and transmit QRSS
2	EALOOP	1 = Enable Analog loopback mode 0 = Disable Analog loopback mode	1	0	In-band Loop Up Code 00001
3	ENLOOP	1 = Enable Network loopback detection 0 = Disable Network loopback detection	1	1	In-band Loop Down Code 001
4	ETAOS	1 = Enable Transmit All Ones 0 = Disable Transmit All Ones			
5	EPAT0	Selects internal data pattern transmission. See right hand section of table for codes. ↗			
6	EPAT1				
7	RESET	1 = Reset device states and clear all registers. 0 = Reset complete.			

1. To enable Dual loopback (DLOOP), set both ERLOOP = 1 and ELLOOP = 1.

Table 10. Control Register #3 Read/Write, Address (A7-A0) = x010010x

Bit	Name	Description
0	ESJAM	1 = Disable jamming of Elastic Store read out clock ($^1/_8$ bit-time adjustment for over/underflow). 0 = Enable jamming of Elastic Store read out clock
1	ESCEN	1 = Center ES pointer for a difference of 16 or 32, depending on depth (clears automatically). 0 = Centering completed
2	ES64	1 = Set elastic store depth to 64 bits. 0 = Set elastic store depth to 32 bits.
3	-	reserved–set to 0 for normal operation.
4	EQZMON	1 = Configure receiver equalizer for monitor mode application (DSX-1 monitor). 0 = Configure receiver equalizer for normal mode application
5	SBIST	1 = Start Built-In Self Test. 0 = Built-In Self Test complete.
6	PLCKE	0 = RPOS/RNEG valid on the rising edge of RCLK. 1 = RPOS/RNEG valid on the falling edge of RCLK.
7	JA6HZ	1 = Set bandwidth of jitter attenuation loop to 6 Hz. 0 = Set bandwidth of jitter attenuation loop to 3 Hz.

Table 11. Interrupt Clear Register Read/Write, Address (A7-A0) = x010011x

Bit	Name	Function[1]
0	CLOS	1 = Clear/Mask Loss of Signal interrupt. 0 = Enable Loss of Signal interrupt.
1	CNLOOP	1 = Clear/Mask Network loopback interrupt. 0 = Enable Network loopback interrupt.
2	CAIS	1 = Clear/Mask Alarm Indication Signal interrupt. 0 = Enable Alarm Indication Signal interrupt.
3	CQRSS	1 = Clear/Mask Quasi-Random Signal Source interrupt. 0 = Enable Quasi-Random Signal Source interrupt.
4	-	reserved–set to 1 for normal operation.
5	CDFMO	1 = Clear/Mask Driver Failure Monitor Open interrupt. 0 = Enable Driver Failure Monitor Open interrupt.
6	CESO	1 = Clear/Mask Elastic Store Overflow interrupt. 0 = Enable Elastic Store Overflow interrupt.
7	CESU	1 = Clear/Mask Elastic Store Underflow interrupt. 0 = Enable Elastic Store Underflow interrupt.

1. Leaving a 1 of in any of these bits masks the associated interrupt.

Table 12. Transition Status Register Read Only, Address (A7-A0) = x010100x

Bit	Name	Function
0	TLOS	1 = Loss of Signal (LOS) has changed since last clear LOS interrupt occurred. 0 = No change in status.
1	TNLOOP	1 = NLOOP has changed since last clear NLOOP interrupt occurred. 0 = No change in status.
2	TAIS	1 = AIS has changed since last clear AIS interrupt occurred. 0 = No change in status.
3	TQRSS	1 = QRSS has changed since last clear QRSS interrupt occurred[1]. 0 = No change in status.
4	-	reserved-ignore.
5	TDFMO	1 = DFMO has changed since last clear DFMS interrupt occurred. 0 = No change in status.
6	ESOVR	1 = ES overflow status sticky bit[2]. 0 = No change in status.
7	ESUNF	1 = ES underflow status sticky bit[2]. 0 = No change in status.

1. A QRSS transition indicates receive QRSS pattern sync or loss. A simple error in QRSS pattern is not reported as a transition.
2. Tripping the overflow or underflow indicator in the ES sets the ESOVR/ESUNF status bit(s). Reading the Transition Status Register clears these bits. Setting CESO and CESU in the Interrupt Clear Register masks these interrupts.

Table 13. Performance Status Register Read Only, Address (A7-A0) = x010101x

Bit	Name	Function
0	LOS	1 = Loss of Signal occurred. 0 = Loss of Signal did not occur.
1	NLOOP	1 = Network loopback active. 0 = Network loopback not active.
2	AIS	1 = Alarm Indicator Signal detected. 0 = Alarm Indicator Signal not detected.
3	QRSS	1 = Quasi-Random Signal Source pattern detected. 0 = Quasi-Random Signal Source pattern not detected.
4	-	reserved–ignore.
5	DFMO	1 = Driver Failure Monitor Open detected. 0 = Driver Failure Monitor Open not detected.
6	BIST	1 = Built-In Self Test passed. 0 = Built-In Self Test did not pass (or was not run).
7	-	reserved–ignore.

Table 14. Equalizer Status Register Read Only, Address (A7-A0) = x010110x

Bit	Name	Function
0	-	reserved–ignore (Least Significant Bit)
1	-	reserved–ignore
2	-	reserved–ignore
3	-	reserved–ignore
4	LATN4	Receive Line Attenuation Indicators. Convert this binary output to a decimal number and multiply by 2.9 dB to determine the approximate cable attenuation as seen by the receiver. For example, if LATN7-4 = 1010_{BIN} (= 10_{DEC}), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB x 10) of cable. This approximation assumes that a 3 V pulse was transmitted.
5	LATN5	
6	LATN6	
7	LATN7	

Table 15. Control Register #4 Read/Write, Address (A7-A0) = x010111x

Bit	Name	Function
0	CODEV	1 = Enable detection of HDB3 code violations at the BPV pin along with bipolar violations and Zero Substitution Violations (if enabled). 0 = Disable detection of HDB3 code violations
1	ZEROV	1 = Enable detection of HDB3 Zero Substitution Violations (four consecutive zeros). Note that Zero Substitution Violations are reported at the BPV pin. 0 = Disable detection of HDB3 Zero Substitution Violations.
2	LOS2048	1 = Set LOS detection threshold to 2048 consecutive zeros. 0 = Set LOS detection threshold to 32 consecutive zeros (for E1 operation) or to 175 consecutive zeros (for T1 operation).
3	COL32CM	1 = Set LOS clear condition criterion to receipt of 32 consecutive marks (E1 operation). 0 = Set LOS clear condition criterion to 12.5% mark density (E1 operation).

Table 15. Control Register #4 Read/Write, Address (A7-A0) = x010111x

Bit	Name	Function
4	-	reserved–set to 0 for normal operation; ignore when reading.
5	-	reserved–set to 0 for normal operation; ignore when reading.
6	-	reserved–set to 0 for normal operation; ignore when reading.
7	-	reserved–set to 0 for normal operation; ignore when reading.

5.0 Application Information

5.1 Transmit Return Loss

Table 16 shows the specification for transmit return loss in E1 applications. The G.703/CH PTT specification is a Swiss Telecommunications Ministry specification.

Table 17 through Table 20 show the transmit return loss values for E1 Short- and Long-Hual and T1 applications. Table 26 shows the receive return loss values.

5.2 Transformer Data

Specifications for transformers are listed in Table 21. A list of transformers recommended for use with the LXT361 are specified in Table 22.

5.3 Application Circuit

Figure 11 shows a typical LXT361 application circuit.

Table 16. E1 Transmit Return Loss Requirements

Frequency Band	Return Loss	
	ETS 300 166	G.703/CH PTT
51-102 kHz	6 dB	8 dB
102-2048 kHz	8 dB	14 dB
2048 - 3072 kHz	8 dB	10 dB

Table 17. Transmit Return Loss (2.048 Mbit/s–Short-Haul)

EC4-1	Xfrmr/Rt	R_L (Ω)	C_L (pF)	Return Loss (dB)
1000	1:2/ 9.1 Ω	75	0	14
			470	16
		120	0	12
			470	13
	1:2.3/9.1 Ω	120	0	13
			470	16

Table 18. Transmit Return Loss (2.048 Mbit/s–Long-Haul) High Return Loss Configuration

EC4-1	Xfrmr/Rt	R_L (Ω)	C_L (pF)	Return Loss (dB)
1001	1:2/ 15 Ω	120	0	19
			470	28
	1:1.53/15 Ω	75	0	18
			470	28

Table 19. Transmit Return Loss (2.048 Mbit/s–Long-Haul)

EC4-1	Xfrmr/Rt	R_L (Ω)	C_L (pF)	Return Loss (dB)
1010	1:2/ 9.1 Ω	120	0	12
			470	13
		75	0	16
			470	18

Table 20. Transmit Return Loss (1.544 Mbit/s–Long- or Short-Haul)

EC4-1	Xfrmr/Rt	R_L (Ω)	C_L (pF)	Return Loss (dB)
Refer to Table 8	1:2/9.1 Ω	100	0	16
			470	17
	1:1.15[1]/ 0 Ω	100	0	2
			470	2

1. A 1:1.15 transmit transformer keeps the total transceiver power dissipation at a low level, a 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.

Table 21. Transformer Specifications for LXT361

Tx/Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric[1] Breakdown V (minimum)
Tx	1.544	1:1.15	600	0.80	60	0.90 pri, 1.70 sec	1500 V_{RMS}
	2.048	1:2.3	600	0.80	60	0.70 pri, 1.20 sec	1500 V_{RMS}[2]
	1.544/2.048	1:2	600	0.80	60	0.70 pri, 1.20 sec	1500 V_{RMS}[2]
Rx	1.544/2.048	1:1	600	1.10	60	1.10 pri, 1.10 sec	1500 V_{RMS}[2]

1. Some ETSI applications may require a 2.3 kV dielectric breakdown voltage.
2. Some applications require transformers with center tap (Long-Haul applications with DC current in the E1/T1 loop).

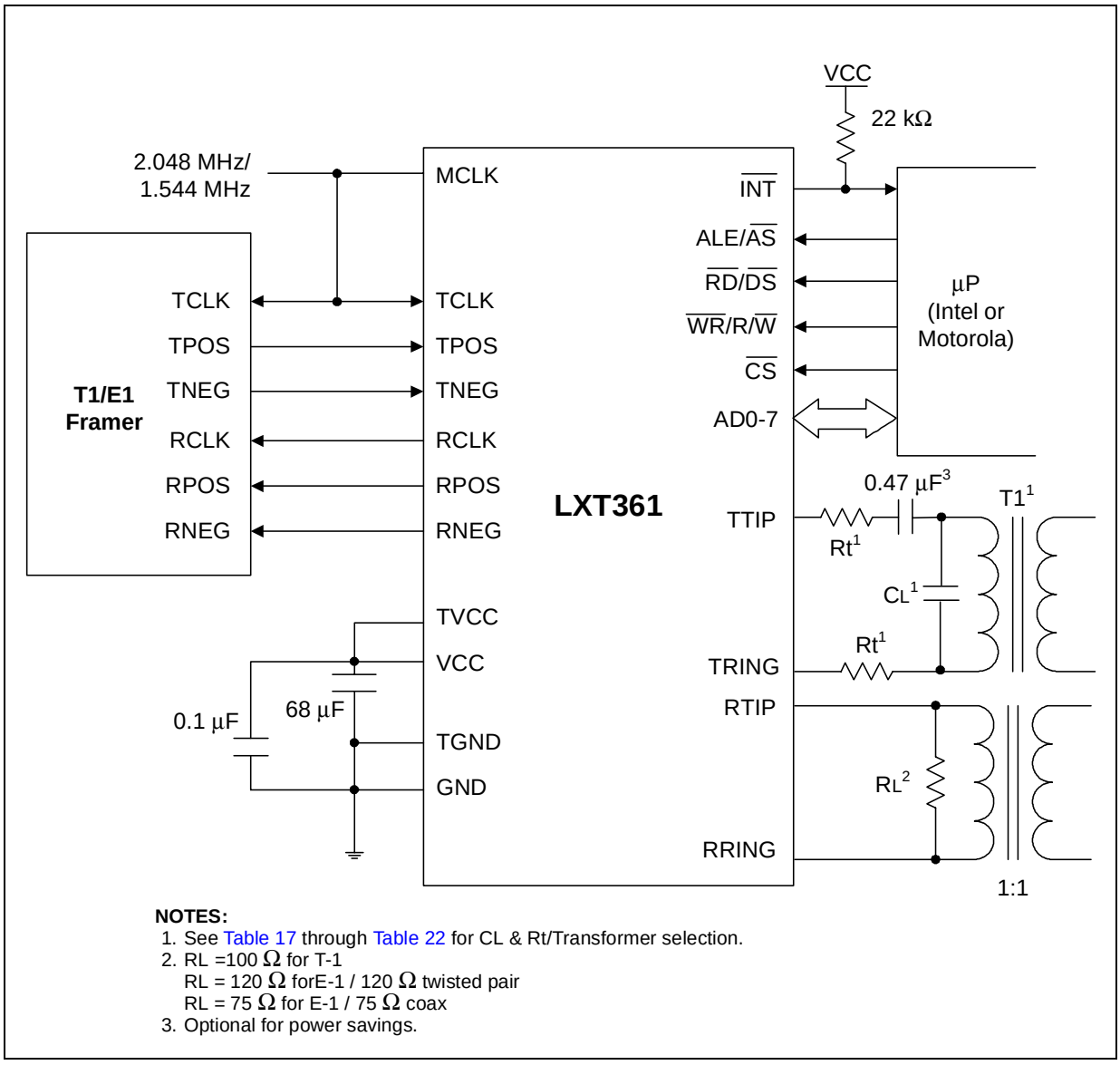
Table 22. Recommended Transformers for LXT361

Tx/Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:1.53	PE-68663	Pulse Engineering
	1:1.15	PE-65388	
		PE-65770	
		16Z5952	Vitec
	1:2	PE-65351	Pulse Engineering
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205D	HALO (combination Tx/Rx set)
		TG26-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1CT:2CT)
		TG48-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1:1)
		16Z5946	Vitec
	1:2.3	PE-65558	Pulse Engineering
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205D	HALO (combination Tx/Rx set)
		16Z5936	Vitec
		16Z5934	

Figure 11 shows a typical LXT361 application in either a T1 or E1 environment. See Table 17 through Table 22 to select the transformers (T1 and T2), resistors (Rt and RL) and capacitor (CL) needed for this application.

Note that if the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may be necessary to reduce the value of the capacitor CL or eliminate it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 11. Typical T1/E1 LXT361 Application



NOTES:
1. See Table 17 through Table 22 for CL & Rt/Transformer selection.
2. RL =100 Ω for T-1
   RL = 120 Ω forE-1 / 120 Ω twisted pair
   RL = 75 Ω for E-1 / 75 Ω coax
3. Optional for power savings.

6.0 Test Specifications

Note: Table 23 through Table 34 and Figure 12 through Figure 21 represent the performance specifications of the LXT361 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 25 through Table 34 are guaranteed over the recommended operating conditions specified in Table 24.

Table 23. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (reference to GND)	VCC, TVCC	–	6.0	V
Input voltage, any pin [1]	VIN	GND - 0.3 V	VCC + 0.3 V	V
Input current, any pin [2]	IIN	- 10	10	mA
Storage Temperature	TSTG	-65	150	° C

Caution: Exceeding these values may cause permanent damage.

Caution: Functional operation under these conditions is not implied.

Caution: Exposure to maximum rating conditions for extended periods may affect device reliability.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TVCC, and TGND can withstand continuous currents of up to 100 mA.

Table 24. Recommended Operating Conditions

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
DC supply [2]	VCC, TVCC	4.75	5.0	5.25	V	
Ambient operating temperature	TA	-40	–	85	° C	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 100 Ω load coupled through 1:1.15 transformer and 0 Ω resistor on TTIP/TRING. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load.
4. Power dissipation while driving 100 Ω load coupled through 1:2 transformer and 9.1 Ω resistor on TTIP/TRING. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load. This implementation has better return loss performance and is less sensitive to changes in impedances variations.
5. Power dissipation while driving 120 Ω load coupled through 1:2 transformer and 9.1 Ω resistor on TTIP/TRING. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load.

Table 24. Recommended Operating Conditions (Continued)

Parameter			Sym	Min	Typ[1]	Max	Unit	Test Conditions
Total power dissipation	T1[3] low power	Short Haul	P_D	–	310	380	mW	100% mark density
			P_D	–	225	295	mW	50% mark density
		Long Haul	P_D	–	245	325	mW	100% mark density
			P_D	–	195	265	mW	50% mark density
	T1[4] standard power	Short Haul	P_D	–	470	560	mW	100% mark density
			P_D	–	320	380	mW	50% mark density
		Long Haul	P_D	–	350	420	mW	100% mark density
			P_D	–	260	310	mW	50% mark density
	E1[5]	Short Haul/ Long Haul	P_D	–	275	330	mW	100% mark density
			P_D	–	215	270	mW	50% mark density

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 100 Ω load coupled through 1:1.15 transformer and 0 Ω resistor on TTIP/TRING. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load.
4. Power dissipation while driving 100 Ω load coupled through 1:2 transformer and 9.1 Ω resistor on TTIP/TRING. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load. This implementation has better return loss performance and is less sensitive to changes in impedances variations.
5. Power dissipation while driving 120 Ω load coupled through 1:2 transformer and 9.1 Ω resistor on TTIP/TRING. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load.

Table 25. Digital Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
High level input voltage (pins 1-5, 9-12, 17, 23-28)[2]	V_{IH}	2.0	–	–	V	
Low level input voltage (pins 1-5, 9-12, 17, 23-28)[2]	V_{IL}	–	–	0.8	V	
High level output voltage[1] (pins 6-8, 10, 11,23, 28)[2]	V_{OH}	2.4	–	–	V	I_{OUT} = 400 µA
Low level output voltage[1] (pins 6-8, 10, 11,23, 28)[2]	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current	I_{LL}	–	–	±50	µA	

1. Output drivers will output CMOS logic levels into CMOS loads.
2. Referenced pin numbers are for the PLCC package. Refer to Figure 2 on page 8 for the corresponding QFP pins.

Table 26. Analog Characteristics

Parameter		Min	Typ[1]	Max	Unit	Test Conditions
Recommended output load on TTIP/TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes	DSX-1, DS1	2.4	3.0	3.6	V	R_L = 100 Ω
	CEPT (ITU)	2.7	3.0	3.3	V	R_L = 120 Ω

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free. The Jitter Attenuator is in the receive path or disabled.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Table 26. Analog Characteristics (Continued)

Parameter		Min	Typ[1]	Max	Unit	Test Conditions
Jitter added by the transmitter[2]	10 Hz - 8 kHz [3]	–	–	0.02	UI	
	8 kHz - 40 kHz [3]	–	–	0.025	UI	
	10 Hz - 40 kHz[3]	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Receiver sensitivity @ 772 kHz (T1)	Mode 1 (EC1 = 1) (T1 Long-Haul)	0	–	26	dB	See Table 8 for Gain Setting
	Mode 2 (EC1 = 0) (T1 Long-Haul)	0	–	36	dB	
	Mode 3 (EC4 = 1) (T1 Short-Haul)	0	–	13.6	dB	
Receiver sensitivity @ 1024 kHz (E1 line loss)	Mode 1 (EC4-1 = 1000) (E1 Short-Haul/12 dB)	0	–	13.6	dB	
	Mode 2 (EC4-1 = 1001 or EC4-1 = 1010) (E1 Long-Haul/43 dB)	0	–	43	dB	
Allowable consecutive zeros before LOS (T1)		160	175	190	–	
Allowable consecutive zeros before LOS (E1)		–	32	–	–	
Input jitter tolerance (T1)	10 kHz - 100 kHz	0.4	–	–	UI	0 dB line AT&T Pub 62411
	1 Hz [3]	138	–	–	UI	
Input jitter tolerance (E1)	10 kHz - 100 kHz	0.2	–	–	UI	0 dB line ITU (G.823)
	1 Hz [3]	37	–	–	UI	
Jitter attenuation curve corner frequency [4]		–	3	–	Hz	selectable in data port
Receive Return Loss (E1)	51 kHz - 102 kHz	–	22	–	dB	
	102 kHz - 2.048 MHz	–	28	–	dB	
	2.048 MHz - 3.072 MHz	–	30	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free. The Jitter Attenuator is in the receive path or disabled.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Figure 12. 2.048 MHz E1 Pulse (See **Table 27**)

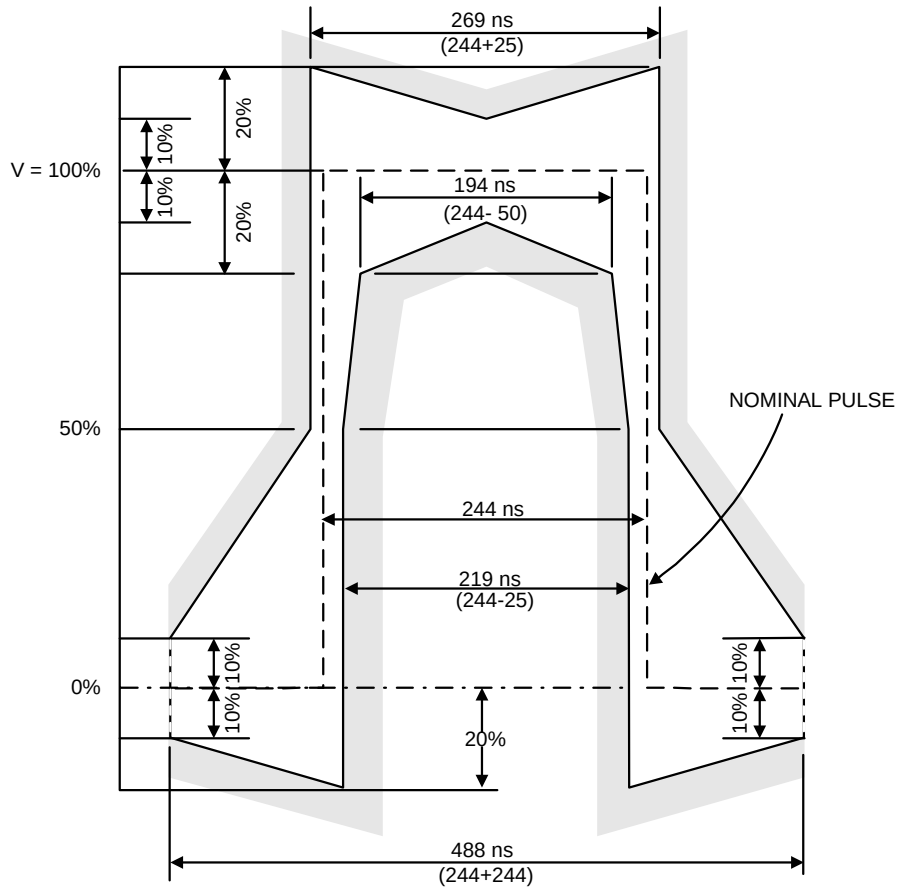


Table 27. 2.048 MHz E1 Pulse Mask Specifications

Parameter	TWP	Coax	Unit
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 13. 1.544 MHz T1 Pulse (DS1 and DSX-1) (See **Table 28**)

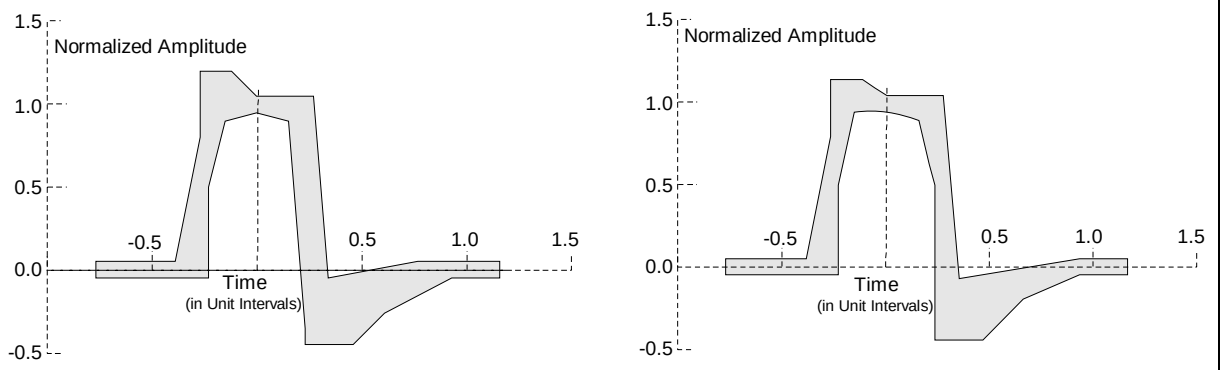


Table 28. 1.544 MHz T1 Pulse Mask Corner Point Specifications

DS1 Template (per ANSI T1. 403-1995)				**DSX-1 Template** (per ANSI T1. 102-1993)			
Minimum Curve		**Maximum Curve**		**Minimum Curve**		**Maximum Curve**	
Time (UI)	**Amplitude**	**Time** (UI)	**Amplitude**	**Time** (UI)	**Amplitude**	**Time** (UI)	**Amplitude**
-0.77	-0.05	-0.77	0.05	-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05	-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80	-0.23	0.50	-0.27	0.80
-0.15	0.90	-0.27	1.20	-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.20	0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05	0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05	0.23	0.50	0.27	1.05
0.23	-0.45	0.34	-0.05	0.23	-0.45	0.35	-0.07
0.46	-0.45	0.77	0.05	0.46	-0.45	0.93	0.05
0.61	-0.26	1.16	0.05	0.66	-0.20	1.16	0.05
0.93	-0.05			0.93	-0.05		
1.16	-0.05			1.16	-0.05		

Table 29. Master and Transmit Clock Timing Characteristics for T1 Operation (See Figure 14)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±50	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	1.544	–	MHz	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 29. Master and Transmit Clock Timing Characteristics for T1 Operation (See Figure 14)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 30. Master and Transmit Clock Timing Characteristics for E1 Operation (See Figure 14)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Master clock frequency	MCLK	–	2.048	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±50	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 14. Transmit Clock Timing

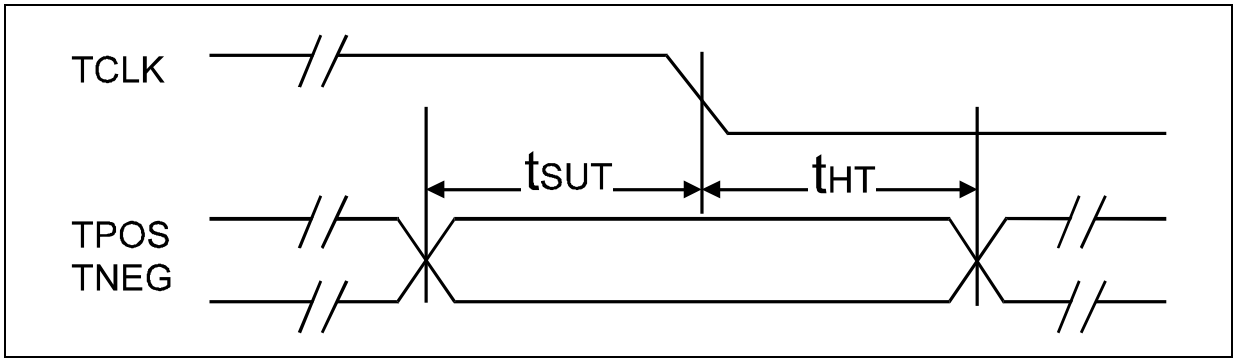


Table 31. Receive Timing Characteristics for T1 Operation (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	t_{PW}	–	648	–	ns
Receive clock pulse width high	t_{PWH}	–	324	–	ns
Receive clock pulse width low[1,3]	t_{PWL}	260	324	388	ns
RPOS/RNEG to RCLK rising time	t_{SUR}	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	t_{HR}	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 32. Receive Timing Characteristics for E1 Operation (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	t_{PW}	–	488	–	ns
Receive clock pulse width high	t_{PWH}	–	244	–	ns
Receive clock pulse width low[1,3]	t_{PWL}	195	244	293	ns
RPOS/RNEG to RCLK rising time	t_{SUR}	–	194	–	ns
RCLK rising to RPOS/RNEG hold time	t_{HR}	–	194	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz.)
3. Worst case conditions guaranteed by design only.

Figure 15. Receive Clock Timing

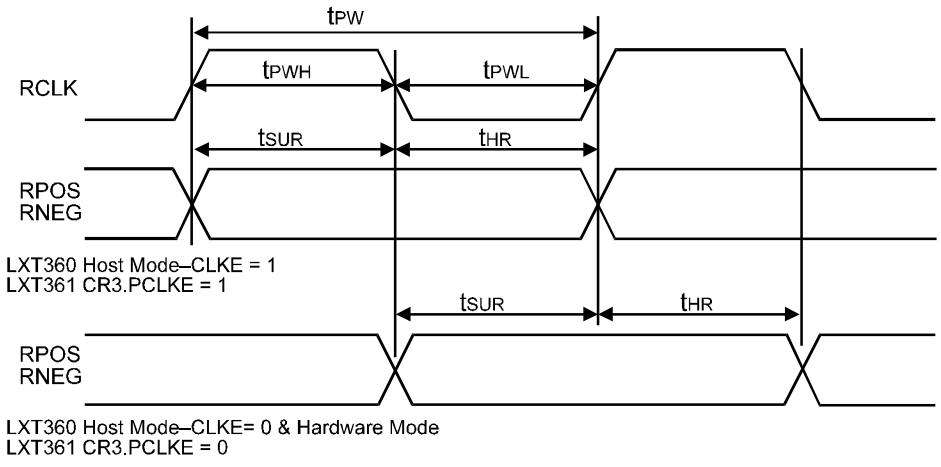


Table 33. LXT361 20 MHz Intel Bus Parallel I/O Timing Characteristics (See **Figure 16**)

Parameter	Sym	Min	Max	Unit	Test Conditions
ALE pulse width	T_{LHLL}	35	–	ns	
Address valid to ALE falling edge	T_{AVLL}	10	–	ns	
ALE falling edge to address hold time	T_{LLAX}	10	–	ns	
ALE falling edge to $\overline{RD}$ falling edge	T_{LLRL}	10	–	ns	
ALE falling edge to $\overline{WR}$ falling edge	T_{LLWL}	10	–	ns	
$\overline{CS}$ falling edge to $\overline{RD}$ falling edge	T_{CLRL}	10	–	ns	
$\overline{CS}$ falling edge to $\overline{WR}$ falling edge	T_{CLWL}	10	–	ns	
$\overline{RD}$ low pulse width	T_{RLRH}	95	–	ns	
$\overline{RD}$ falling edge to data valid	T_{RLDV}	10	55	ns	
Data hold time after $\overline{RD}$ rising edge	T_{RHDX}	5	35	ns	
$\overline{RD}$ rising edge to ALE rising edge	T_{RHLH}	15	–	ns	
$\overline{RD}$ rising edge to address valid	T_{RHAV}	35	–	ns	
$\overline{CS}$ low hold time after $\overline{RD}$ rising edge	T_{RHCH}	0	–	ns	
$\overline{WR}$ low pulse width	T_{WLWH}	95	–	ns	
Data setup time before $\overline{WR}$ rising edge	T_{DVWH}	40	–	ns	
Data hold time after $\overline{WR}$ rising edge	T_{WHDX}	30	–	ns	
$\overline{WR}$ rising edge to ALE rising edge	T_{WHLH}	15	–	ns	
$\overline{CS}$ low hold time after $\overline{WR}$ rising edge	T_{WHCH}	15	–	ns	

Figure 16. LXT361 I/O Timing Diagram for Intel Address/Data Bus

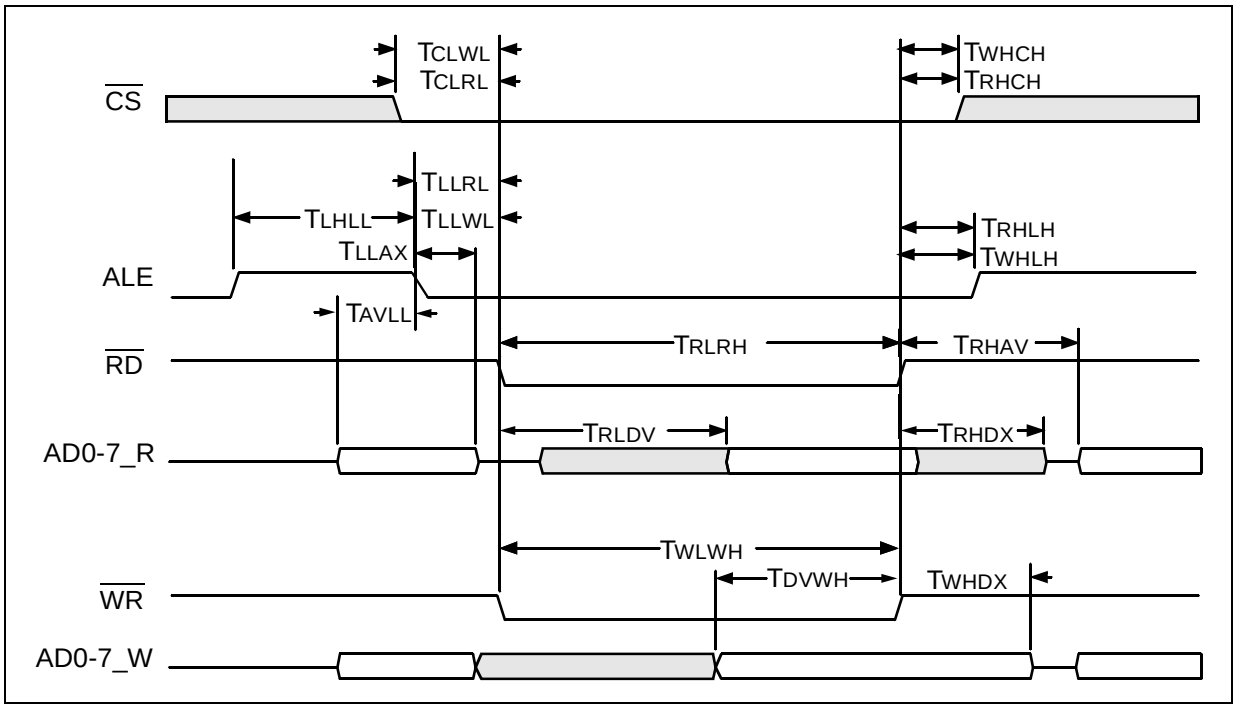


Table 34. LXT361 16.78 MHz Motorola Bus Parallel I/O Timing Characteristics (See Figure 17)

Parameter	Symbol	Min	Max	Units	Test Conditions
$\overline{DS}$ rising edge to $\overline{AS}$ rising edge	TDSHASH	15	–	ns	
$\overline{AS}$ high pulse width	TASHASL	35	–	ns	
Address valid setup time at $\overline{AS}$ falling edge	TAVASL	10	–	ns	
$\overline{AS}$ falling edge to Address valid hold time	Taslax	10	–	ns	
$\overline{AS}$ falling edge to $\overline{DS}$ falling edge	TASLDSL	20	–	ns	
$\overline{CS}$ falling edge to $\overline{DS}$ falling edge	TCSLDSL	10	–	ns	
$\overline{DS}$ low pulse width	TDSLDSH	95	–	ns	
$\overline{DS}$ falling edge to data valid	TDSLDV	10	55	ns	
Data hold time after $\overline{DS}$ rising edge	TDSHDX	5	35	ns	
R/$\overline{W}$ falling edge to $\overline{DS}$ falling edge	TRWLDSL	10	–	ns	
Data setup time before $\overline{DS}$ rising edge	TDVDSH	40	–	ns	
Data hold time after $\overline{DS}$ rising edge	Tdxdsh	30	–	ns	
R/$\overline{W}$ low hold time after $\overline{DS}$ rising edge	TDSHRWH	15	–	ns	
$\overline{CS}$ low hold time after $\overline{DS}$ rising edge	TDSHCSH	15	–	ns	

Figure 17. LXT361 I/O Timing Diagram for Motorola Address/Data Bus

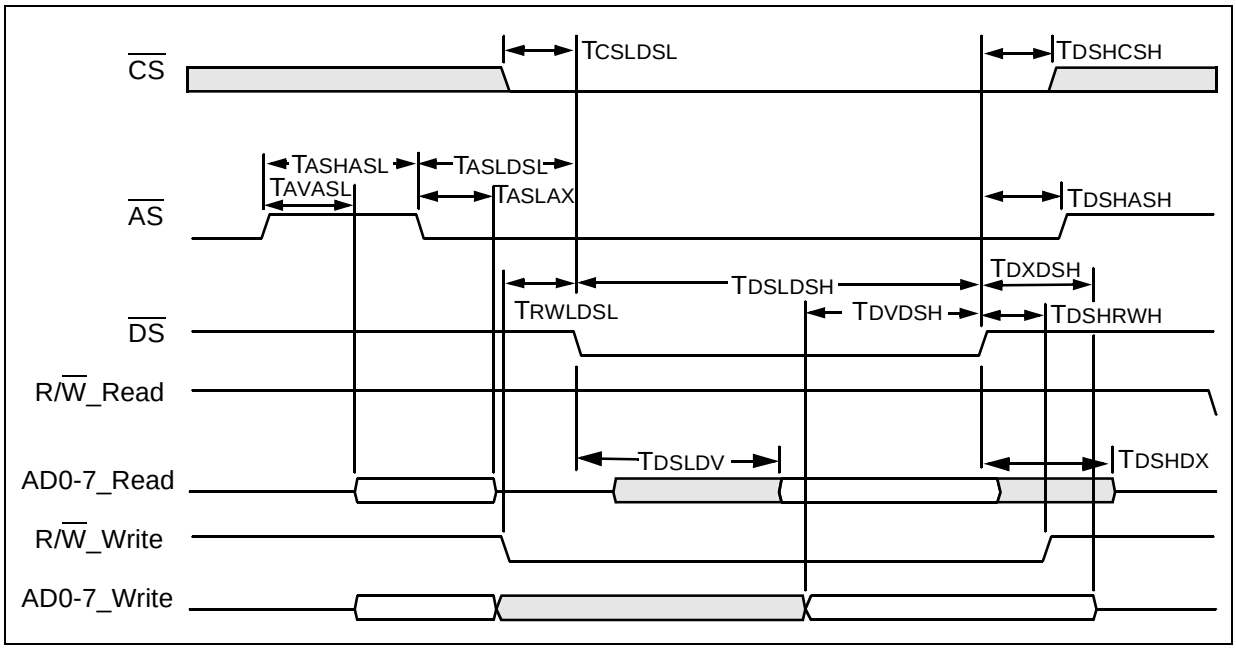


Figure 18. Typical T1 Jitter Tolerance at 36 dB

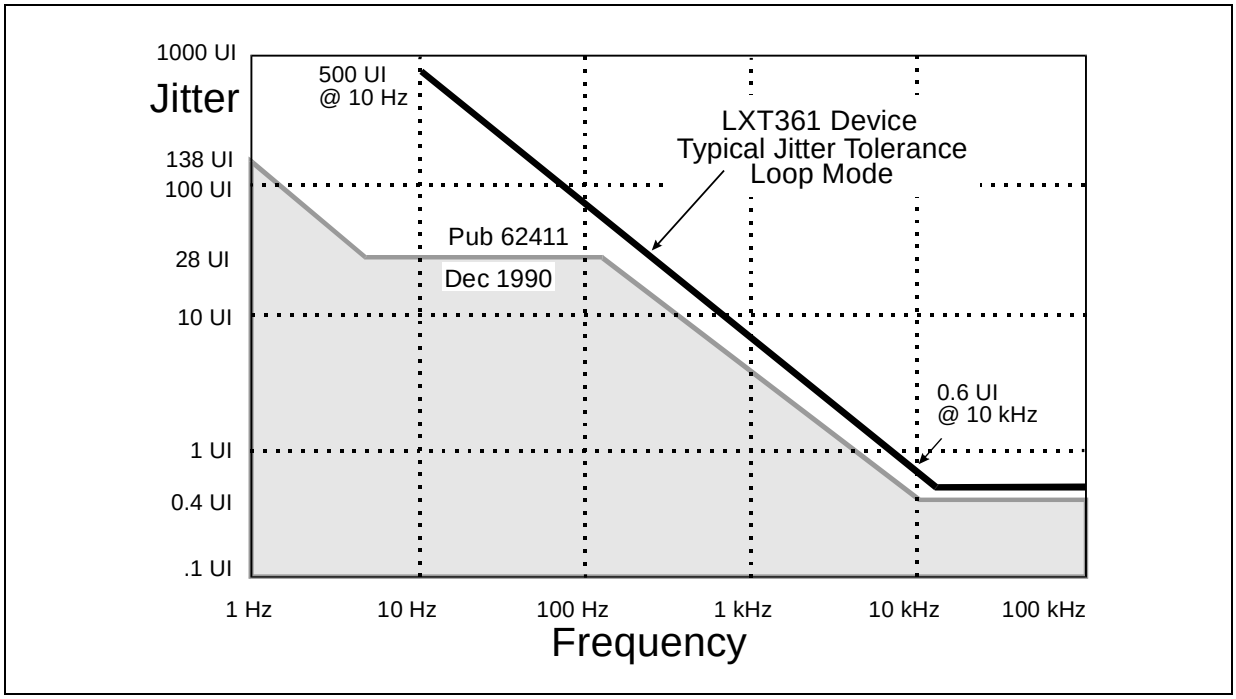


Figure 19. Typical E1 Jitter Tolerance at 43 dB

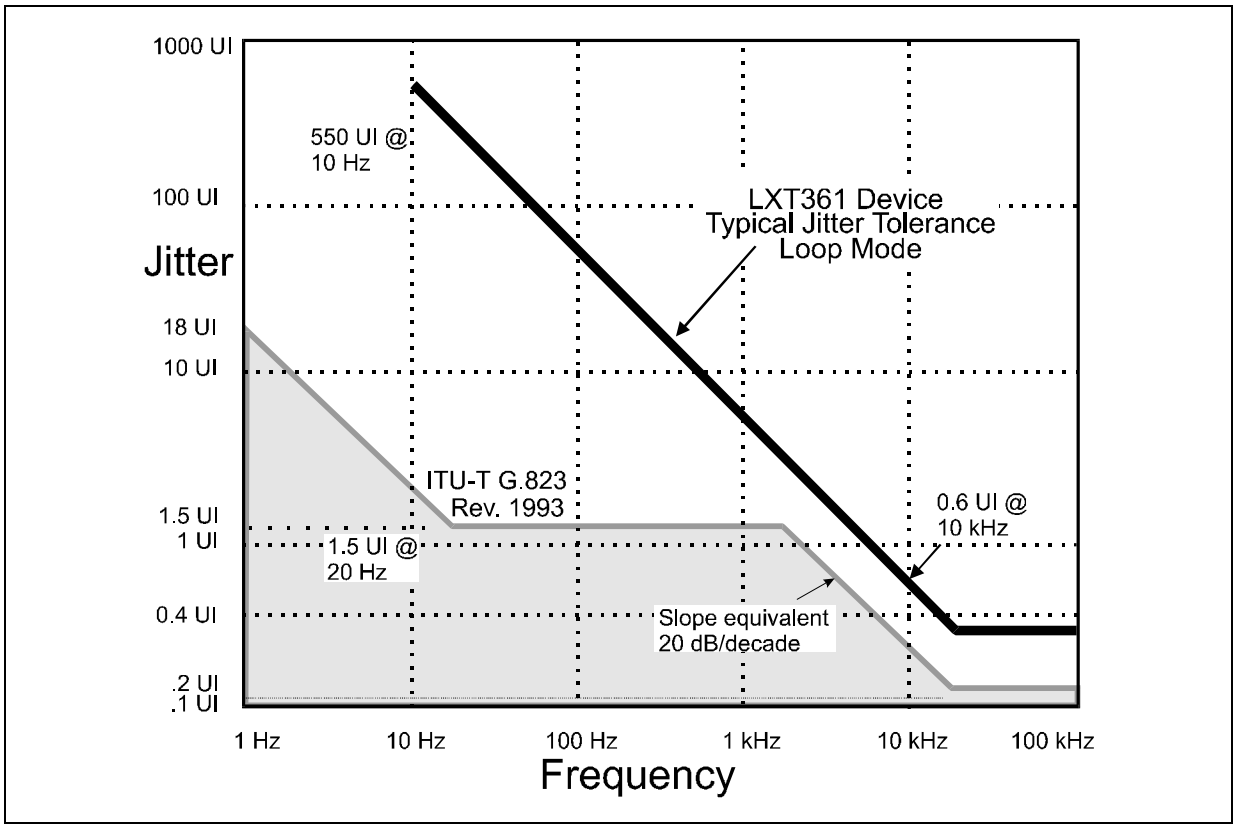


Figure 20. Typical E1 Jitter Attenuation

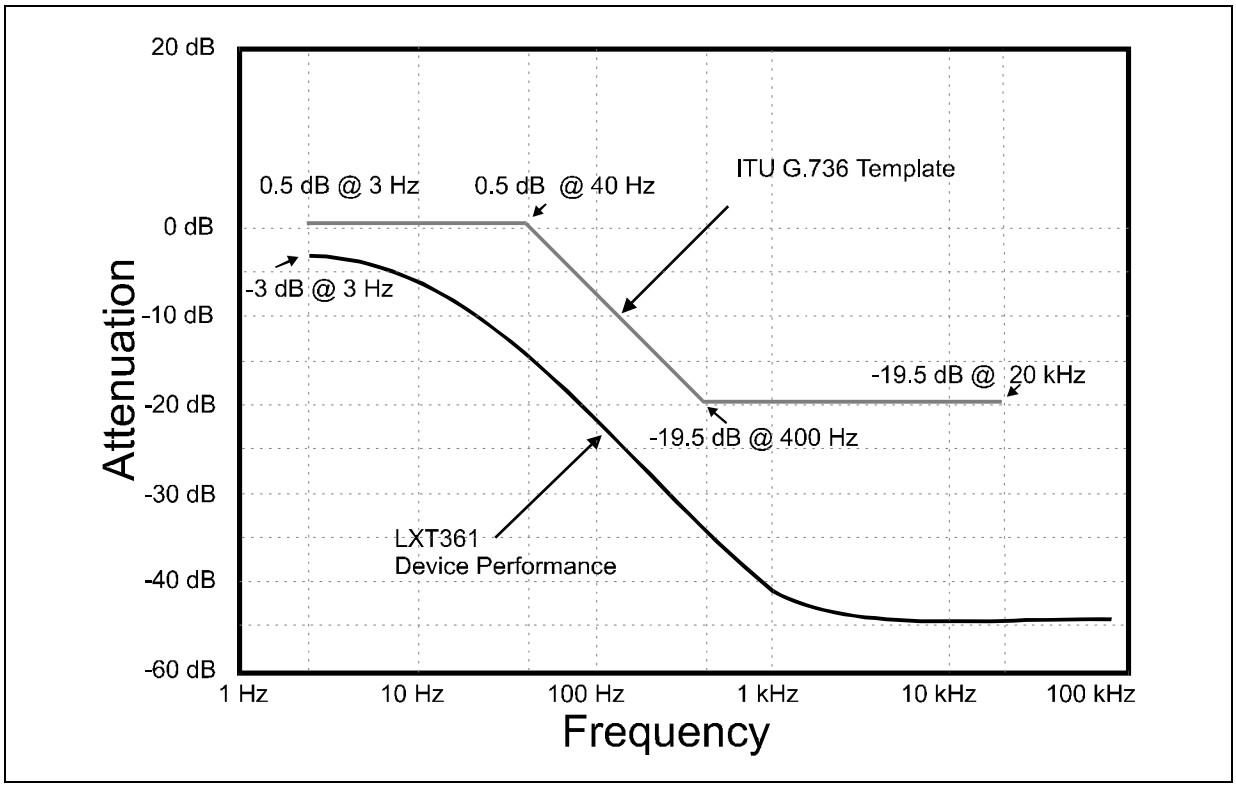
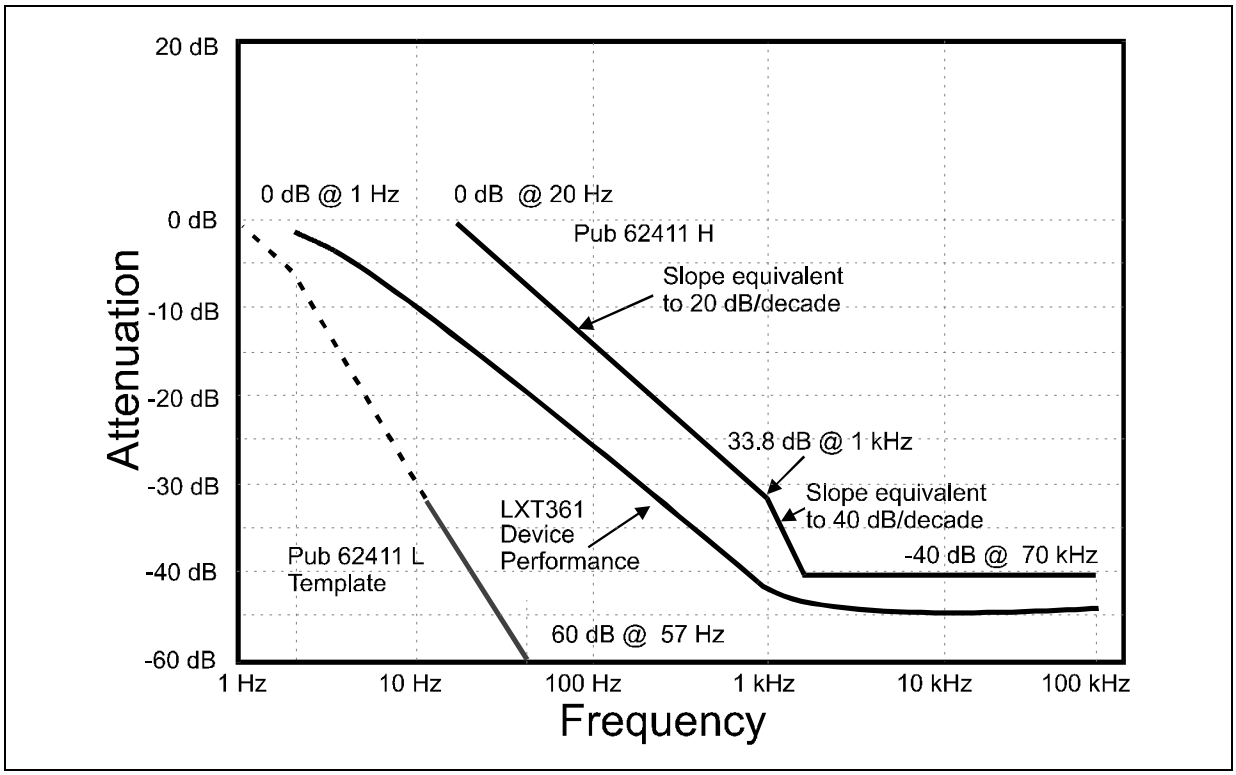


Figure 21. \T1 Jitter Attenuation

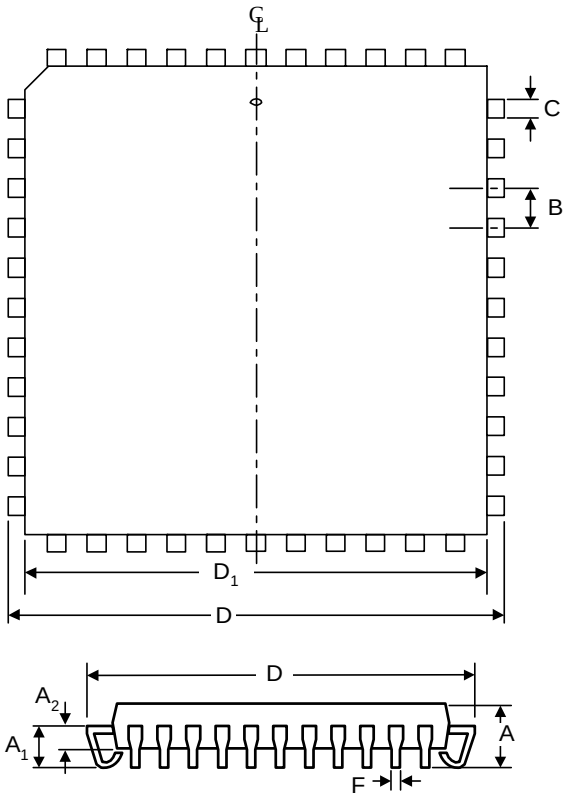


7.0 Mechanical Specifications

Figure 22. Plastic Leaded Chip Carrier (PLCC) Package Specifications

28-Pin PLCC

- Part Number LXT361PE
- Extended Temperature Range (-40 °C to 85 °C)



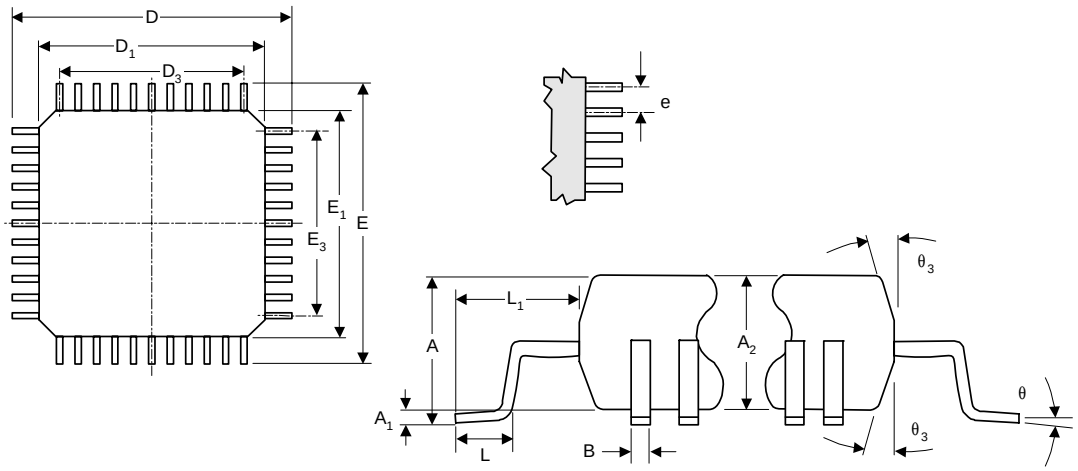
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers.

Figure 23. Plastic Quad Flat Package (PQFP) Specifications

44-Pin PQFP

- Part Number LXT361QE
- Extended Temperature Range (-40 °C to 85 °C)



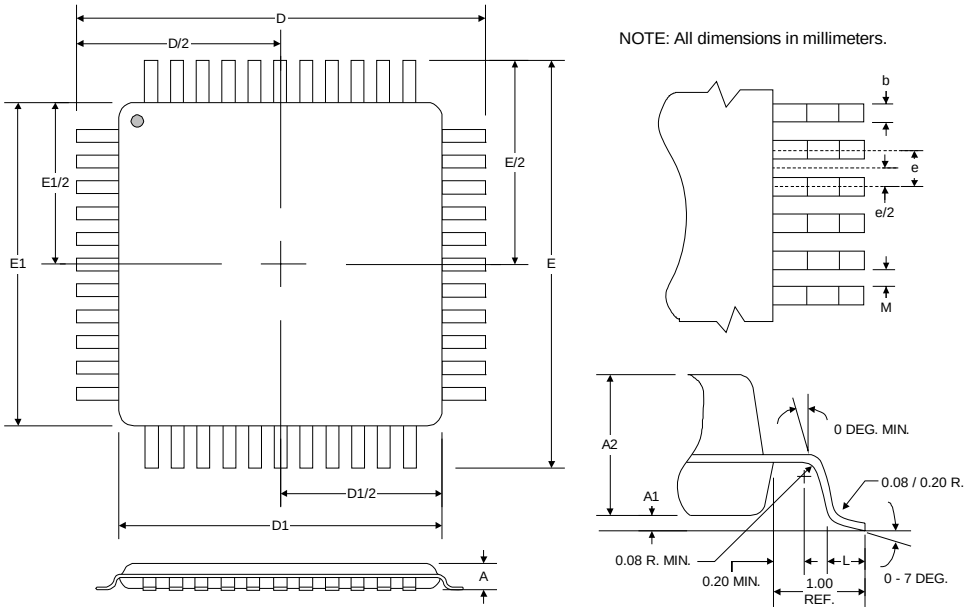
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.096	–	2.45
A1	0.010	–	0.25	–
A2	0.077	0.083	1.95	2.10
B	0.012	0.018	0.30	0.45
D	0.510	0.530	12.95	13.45
D1	0.390	0.398	9.90	10.10
D3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
E	0.510	0.530	12.95	13.45
E1	0.390	0.398	9.90	10.10
E3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
e	0.031 BSC[1] (nominal)		0.80 BSC[1] (nominal)	
L	0.029	0.041	0.73	1.03
L1	0.063 BSC[1] (nominal)		1.60 BSC[1] (nominal)	
q3	5°	16°	5°	16°
q	0°	7°	0°	7°

1. BSC—Basic Spacing between Centers.

Figure 24. Low-Profile Quad Flat Package (LQFP) Specifications

44-Pin LQFP

- Part Number LXT361LE
- Extended Temperature Range (-40 °C to 85 °C)



Dimension[1]	Millimeters		
	Minimum	Nominal	Maximum
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	12.00 (basic spacing between centers)		
D1	10.00 (basic spacing between centers)		
E	12.00 (basic spacing between centers)		
E1	10.00 (basic spacing between centers)		
e	0.80 (basic spacing between centers)		
L	0.45	0.60	0.75
M	0.15	-	-
1. See JEDEC Publication for additional specifications.			

7.1 Top Label Markings

Figure 25 shows a sample LQFP package for the LXT361 Transceiver.

Notes:

1. In contrast to the Pb-Free (RoHS-compliant) LQFP package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.
2. Further information regarding RoHS and lead-free components can be obtained from your local Intel representative.
   For general information, see http://www.intel.com/technology/silicon/leadfree.htm.

Figure 25. Sample PLCC Package – Intel® DJLXT361LE Transceiver

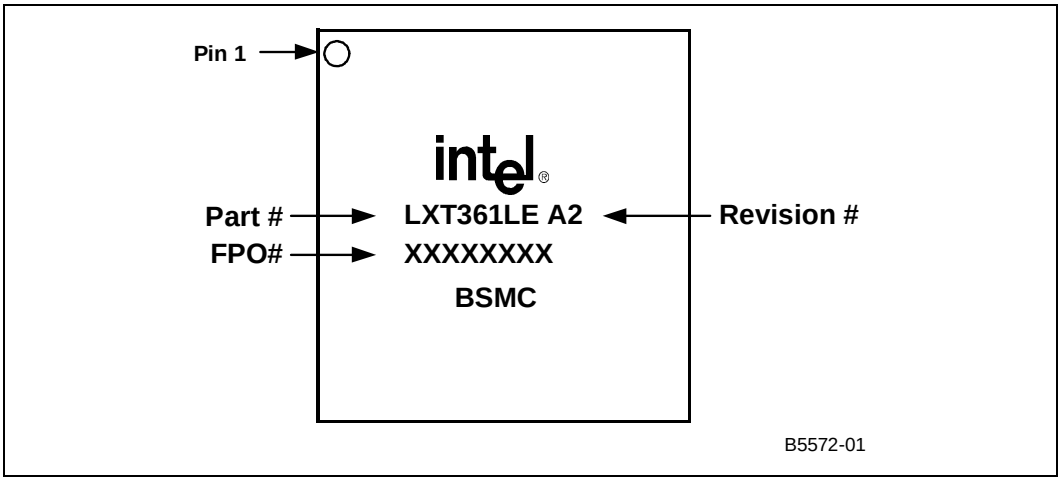


Figure 26 shows a sample Pb-Free (RoHS-compliant) LQFP package for the LXT361 Transceiver.

Figure 26. Sample Pb-Free (RoHS-Compliant) LQFP Package – Intel® WJLXT361LE Transceiver

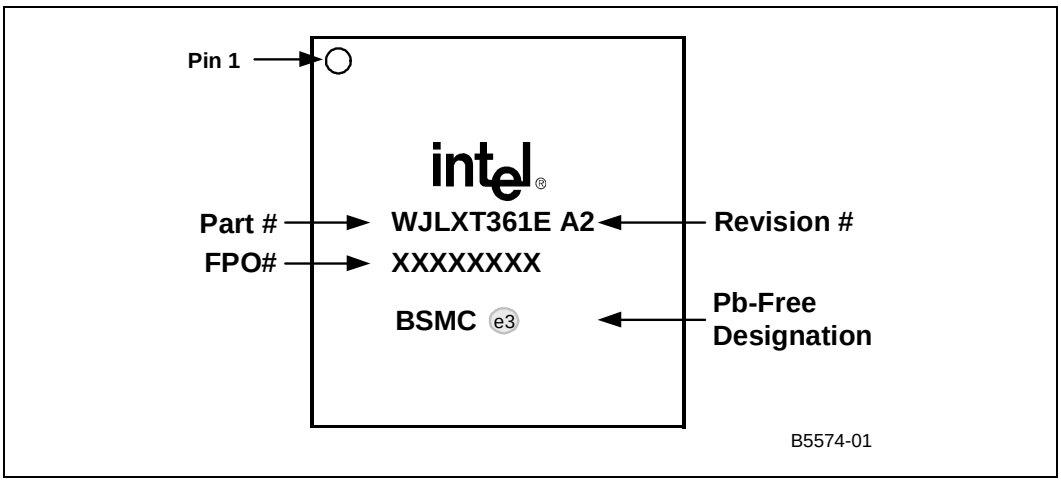


Figure 25 shows a sample PLCC package for the LXT361 Transceiver.

Notes:

1. In contrast to the Pb-Free (RoHS-compliant) PLCC package, the non-RoHS-compliant package does not have the “e3” symbol in the last line of the package label.

Figure 27. Sample PLCC Package – Intel® NLXT361PE Transceiver

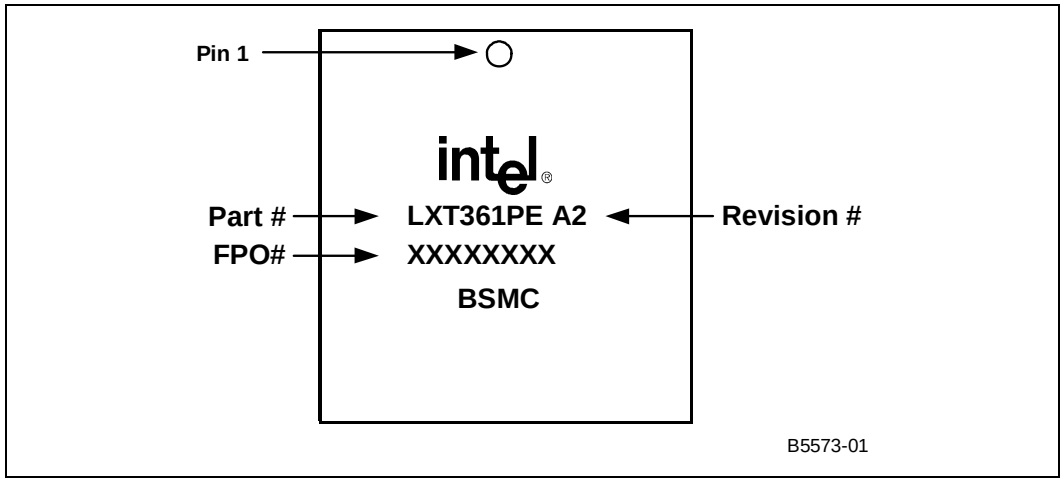
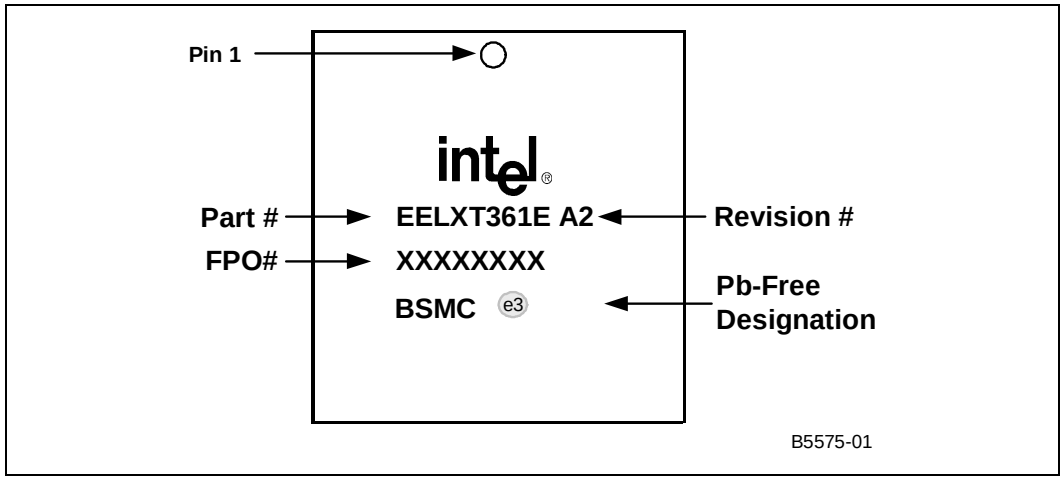


Figure 26 shows a sample Pb-Free (RoHS-compliant) PLCC package for the LXT361 Transceiver.

Figure 28. Sample Pb-Free (RoHS-Compliant) PLCC Package – Intel® EELXT361PE Transceiver



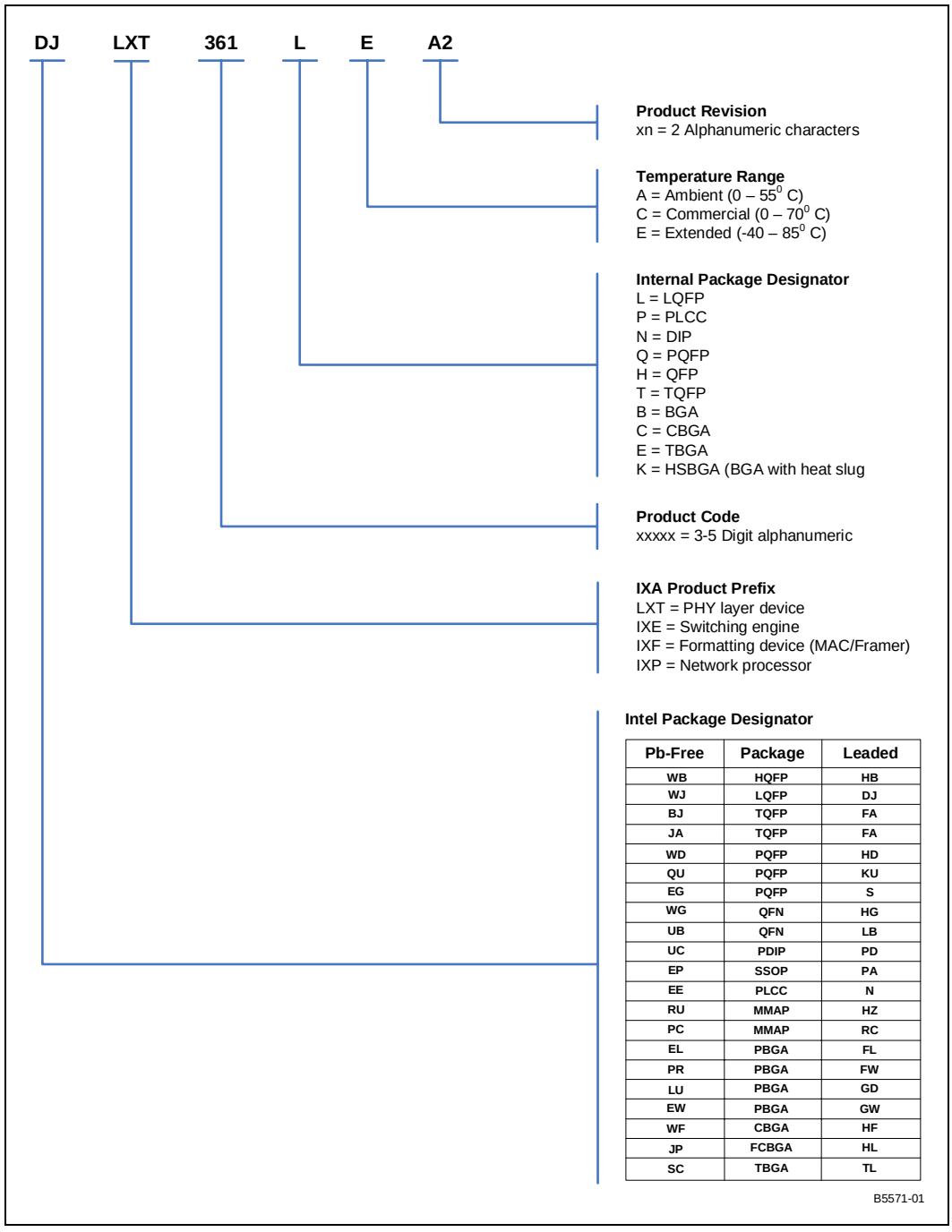
8.0 Product Ordering Information

Table 35 provides LXT361 Transceiver product ordering information.

Table 35. Product Ordering Information

Product Number	Revision	Package Type	Pin Count	RoHS Compliant
DJLXT361LE.A2	A2	LQFP	44	No
WJLXT361LE.A2	A2	LQFP	44	Yes
NLXT361PE.A2	A2	PLCC	28	No
EELXT361PE.A2	A2	PLCC	28	Yes

Figure 29. Ordering Information Matrix – Sample



Pb-Free	Package	Leaded
WB	HQFP	HB
WJ	LQFP	DJ
BJ	TQFP	FA
JA	TQFP	FA
WD	PQFP	HD
QU	PQFP	KU
EG	PQFP	S
WG	QFN	HG
UB	QFN	LB
UC	PDIP	PD
EP	SSOP	PA
EE	PLCC	N
RU	MMAP	HZ
PC	MMAP	RC
EL	PBGA	FL
PR	PBGA	FW
LU	PBGA	GD
EW	PBGA	GW
WF	CBGA	HF
JP	FCBGA	HL
SC	TBGA	TL