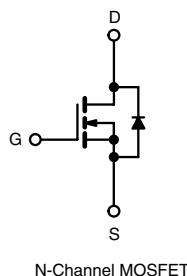
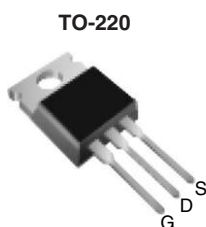


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	450	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.63
Q_g (Max.) (nC)	80	
Q_{gs} (nC)	12	
Q_{gd} (nC)	41	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRF744PbF SiHF744-E3
SnPb	IRF744 SiHF744

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	450	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	35	
Linear Derating Factor		1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	540	mJ
Repetitive Avalanche Current ^a	I_{AR}	8.8	A
Repetitive Avalanche Energy ^a	E_{AR}	13	mJ
Maximum Power Dissipation	P_D	125	W
Peak Diode Recovery dV/dt^c	dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10 1.1	

Notes

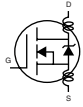
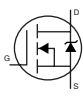
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 12\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 8.8\text{ A}$ (see fig. 12).
- $I_{SD} \leq 8.8\text{ A}$, $dV/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

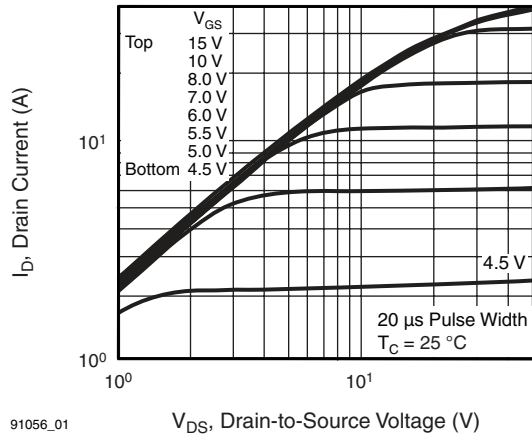
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

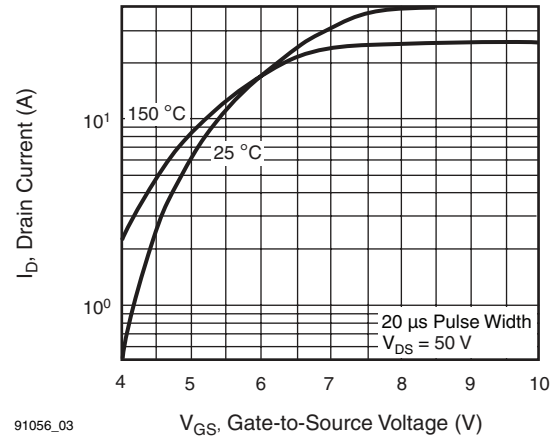
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		450	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.59	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 450 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 360 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 5.3 A ^b	-	-	0.63	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 5.3 A ^b		4.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V V _{DS} = 25 V f = 1.0 MHz, see fig. 5		-	1400	-	pF
Output Capacitance	C _{oss}			-	370	-	
Reverse Transfer Capacitance	C _{rss}			-	140	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 8.8 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	80	nC
Gate-Source Charge	Q _{gs}			-	-	12	
Gate-Drain Charge	Q _{gd}			-	-	41	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 225 V, I _D = 8.8 A R _G = 9.1 Ω, R _D = 25 Ω, see fig. 10 ^b		-	8.7	-	ns
Rise Time	t _r			-	28	-	
Turn-Off Delay Time	t _{d(off)}			-	58	-	
Fall Time	t _f			-	27	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8.8	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	35	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 8.8 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 8.8 A, dI/dt = 100 A/μs ^b		-	490	740	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.2	4.8	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

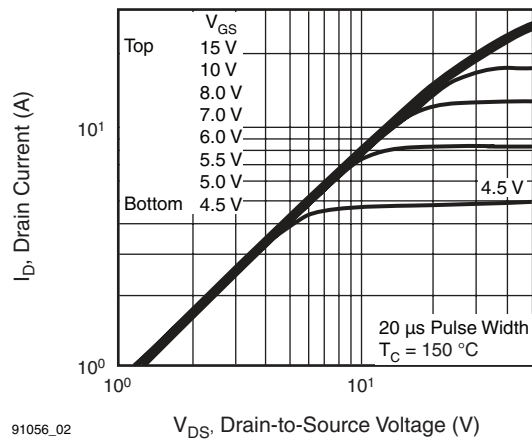
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


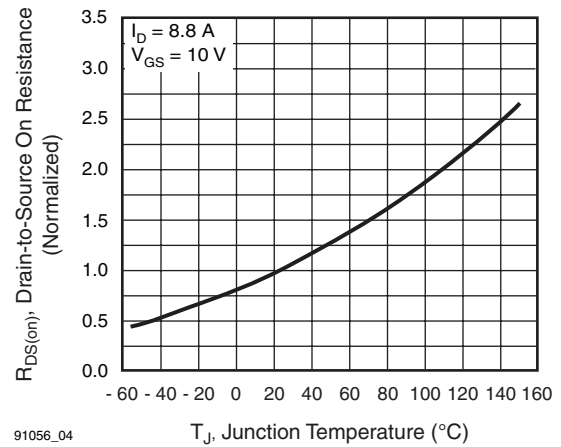
91056_01

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$


91056_03

Fig. 3 - Typical Transfer Characteristics


91056_02

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$


91056_04

Fig. 4 - Normalized On-Resistance vs. Temperature

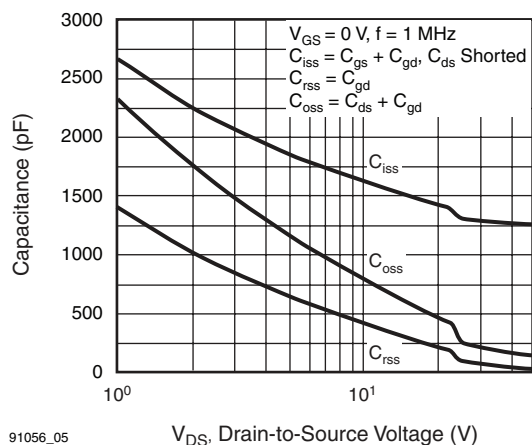


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

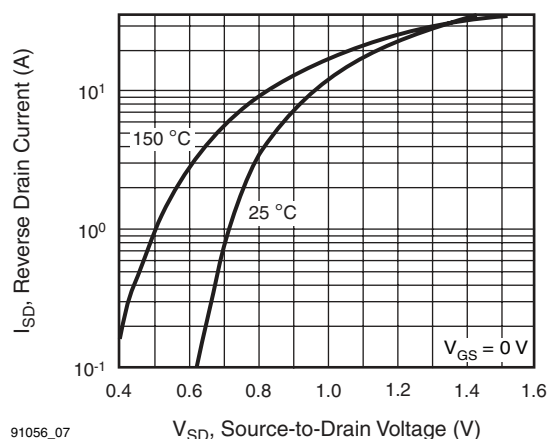


Fig. 7 - Typical Source-Drain Diode Forward Voltage

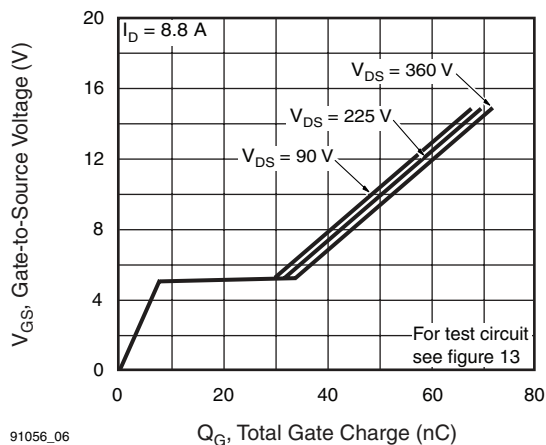


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

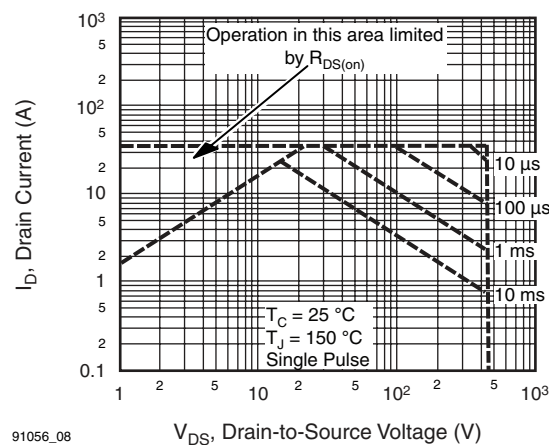


Fig. 8 - Maximum Safe Operating Area

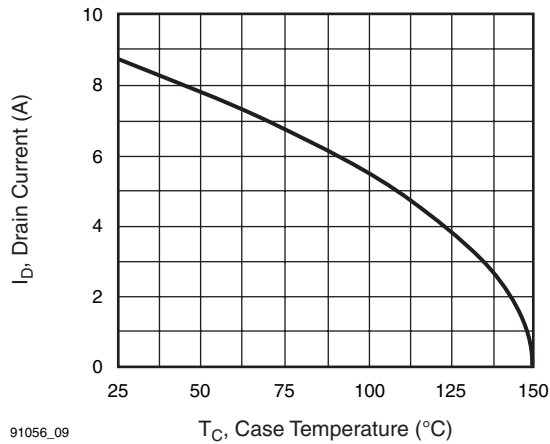


Fig. 9 - Maximum Drain Current vs. Case Temperature

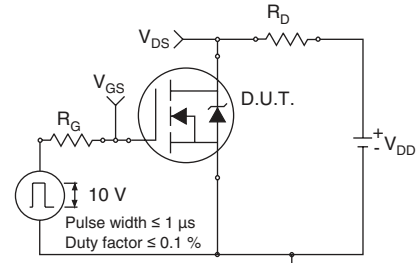


Fig. 10a - Switching Time Test Circuit

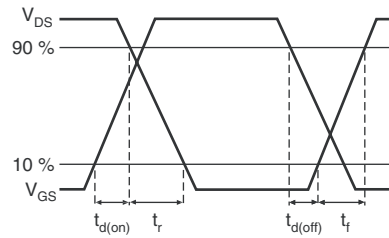


Fig. 10b - Switching Time Waveforms

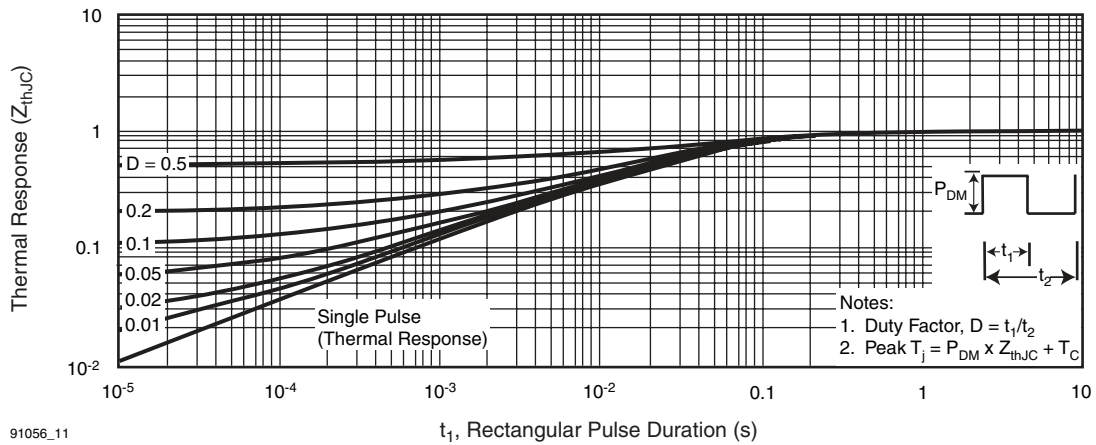


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

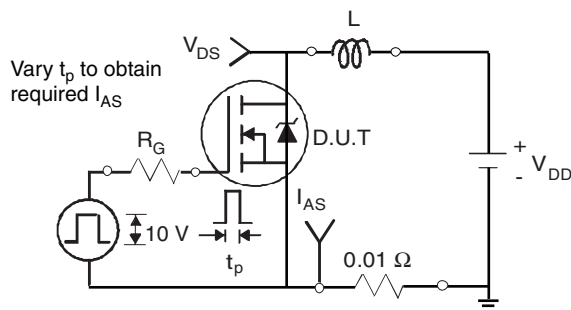


Fig. 12a - Unclamped Inductive Test Circuit

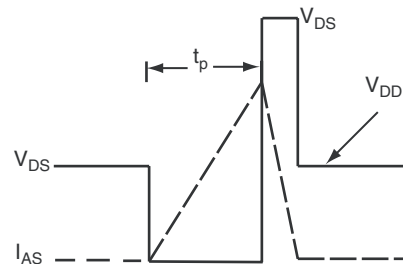


Fig. 12b - Unclamped Inductive Waveforms

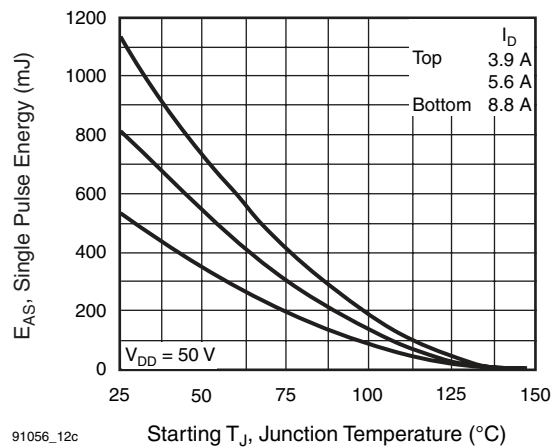


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

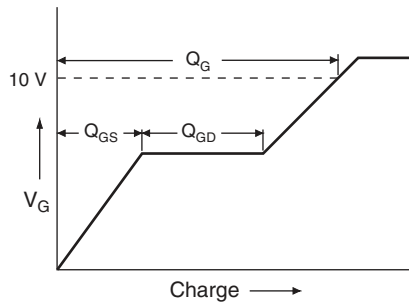


Fig. 13a - Basic Gate Charge Waveform

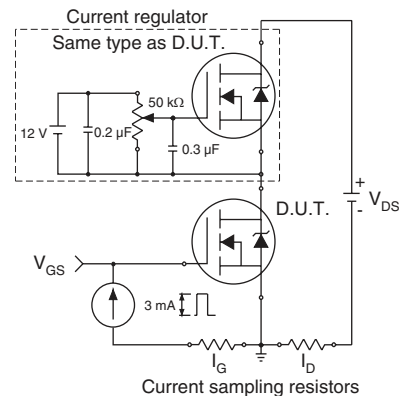
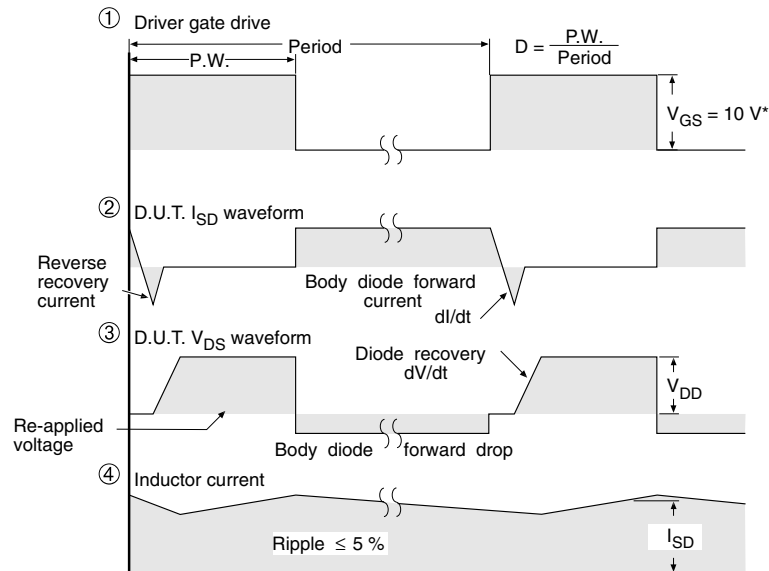
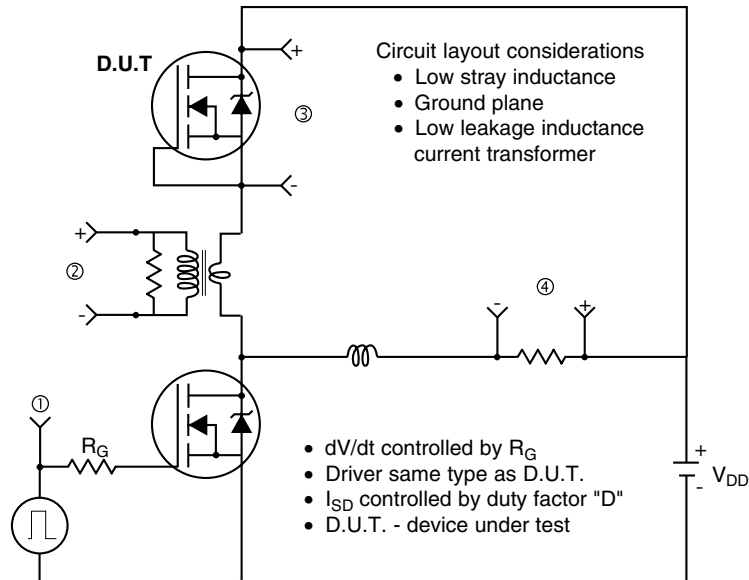


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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