

HAT1110R

Silicon P Channel Power MOS FET Power Switching

REJ03G0416-0200

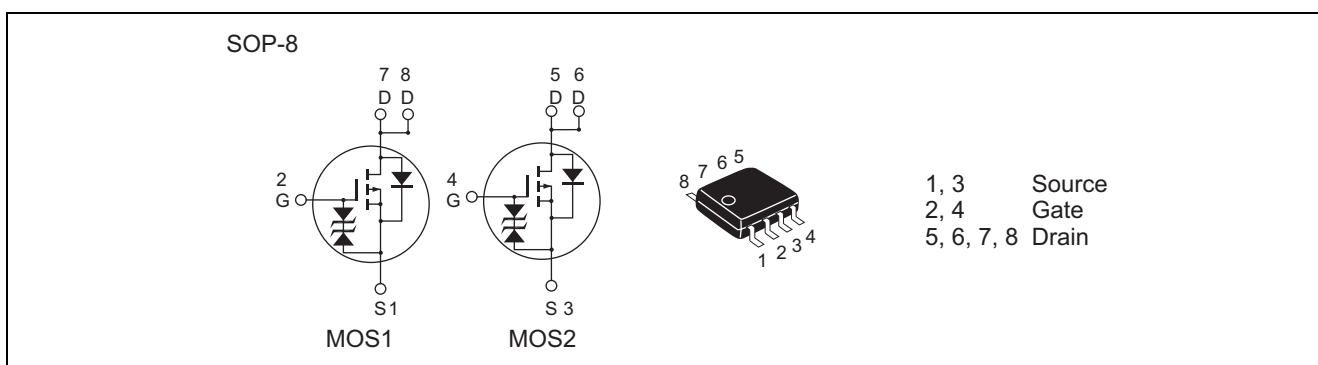
Rev.2.00

Oct.07.2004

Features

- Capable of -4.5 V gate drive
- Low drive current
- High density mounting

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	-80	V
Gate to source voltage	V_{GS}	± 20	V
Drain current	I_D	-1	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-6	A
Reverse drain current	I_{DR}	-1	A
Channel dissipation	P_{ch} ^{Note2}	1.2	W
Channel dissipation	P_{ch} ^{Note3}	1.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$

Notes: 1. $PW \leq 10\text{ }\mu\text{s}$, duty cycle $\leq 1\%$

2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{ s}$

3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{ s}$

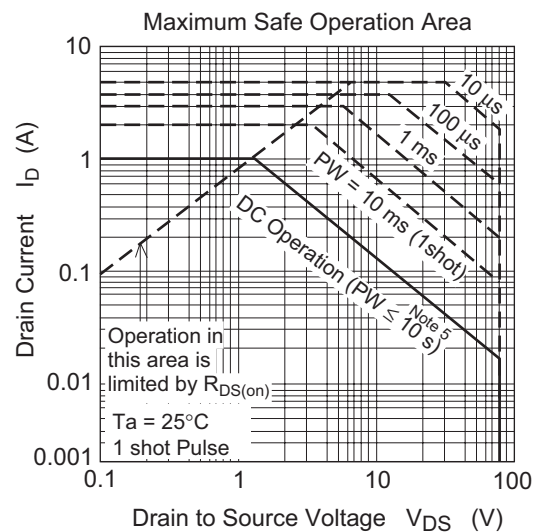
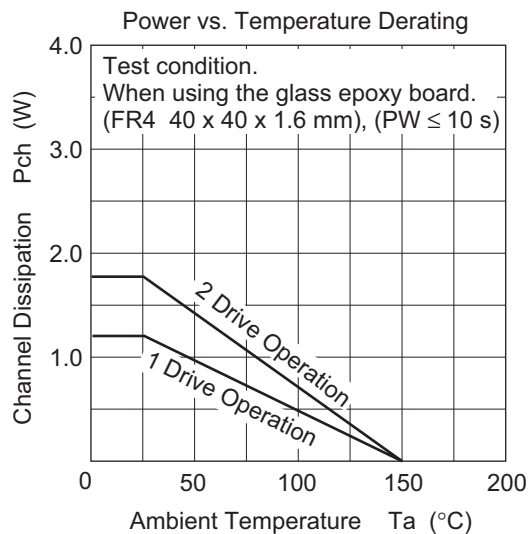
Electrical Characteristics

(Ta = 25°C)

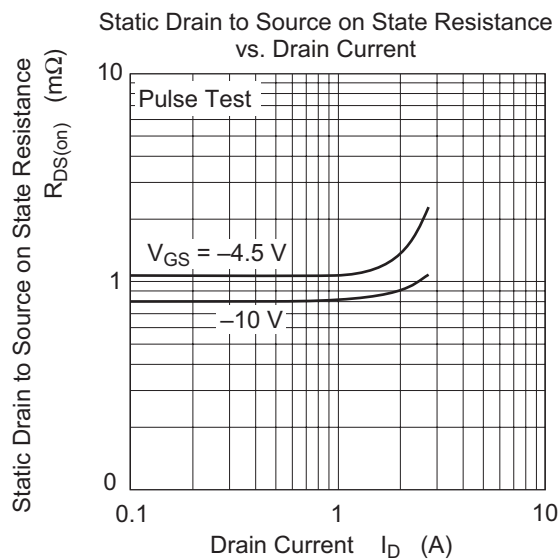
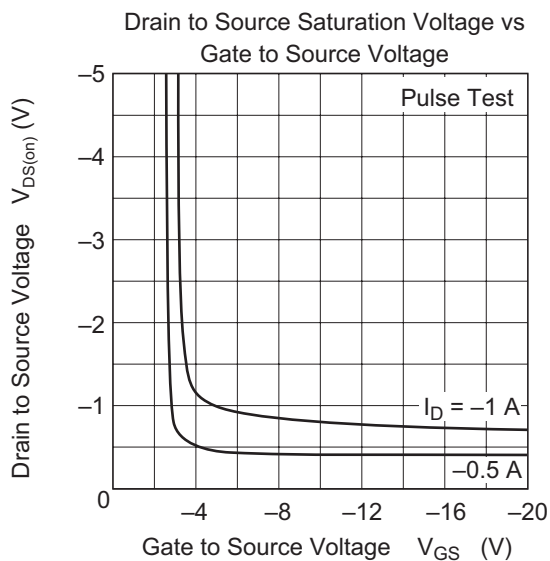
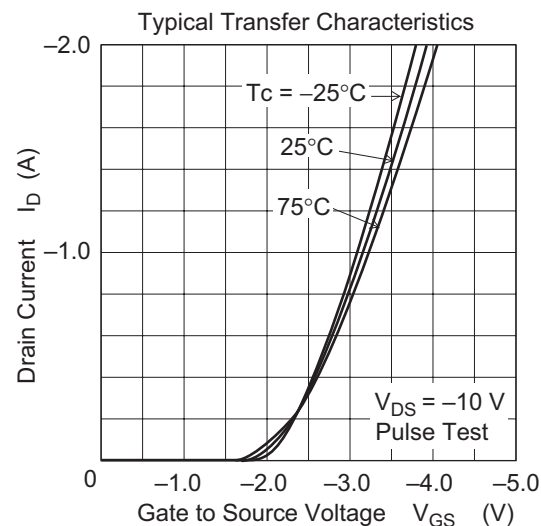
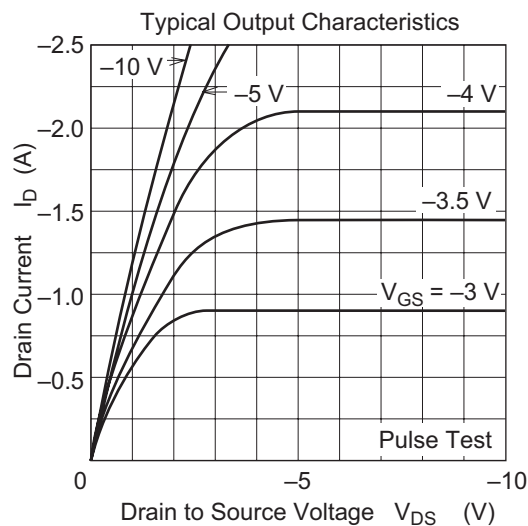
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-80	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -80 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.8	1.05	Ω	$I_D = -0.5 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	1.02	1.38	Ω	$I_D = -0.5 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	0.4	0.8	—	S	$I_D = -0.5 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	170	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	24	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	16	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	3.6	—	nC	$V_{DD} = -25 \text{ V}$
Gate to source charge	Q_{gs}	—	0.3	—	nC	$V_{GS} = -10 \text{ V}$
Gate to drain charge	Q_{gd}	—	0.7	—	nC	$I_D = -1.0 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -0.5 \text{ A}$
Rise time	t_r	—	12	—	ns	$V_{DD} \approx -30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	25	—	ns	$R_L = 60 \Omega$
Fall time	t_f	—	5.5	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	-0.86	-1.12	V	$I_F = -1.0 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	21	—	ns	$I_F = -1.0 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

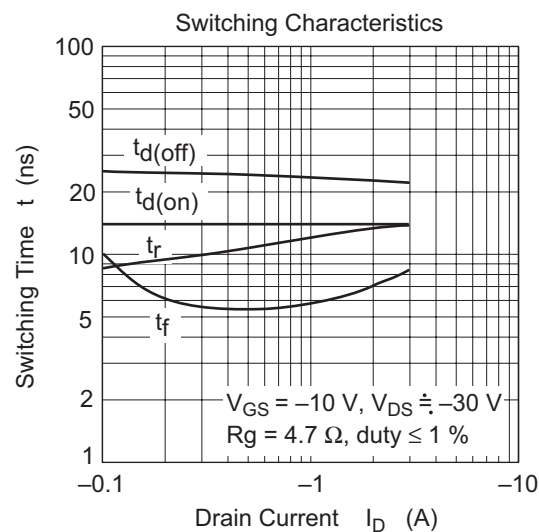
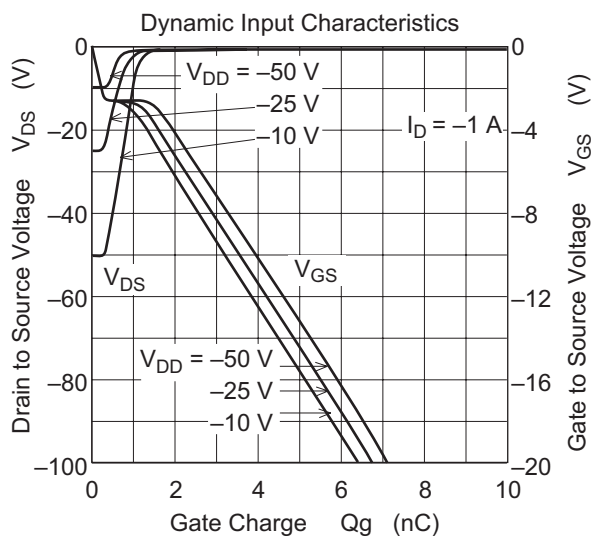
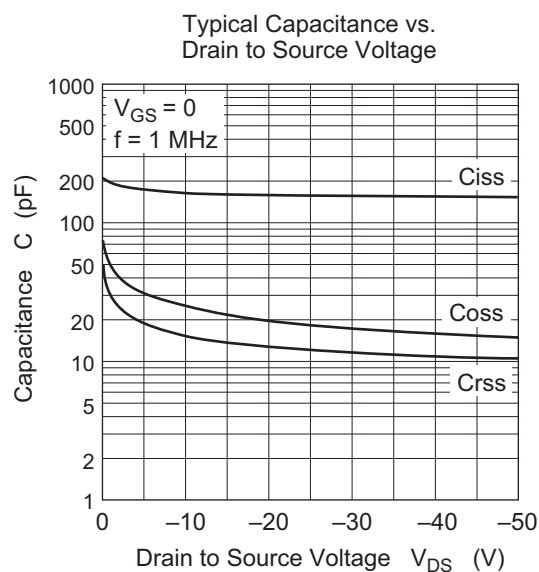
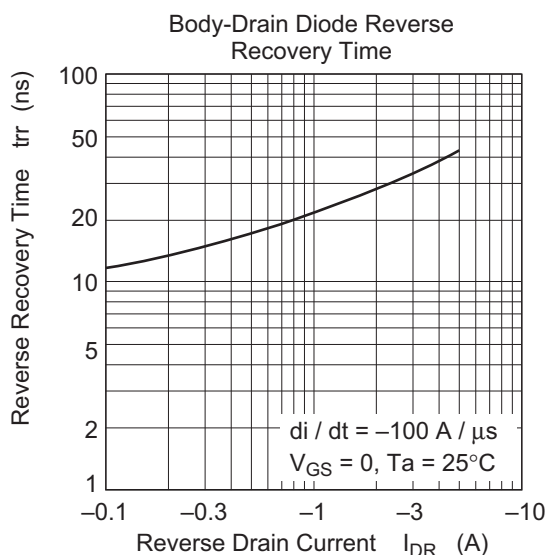
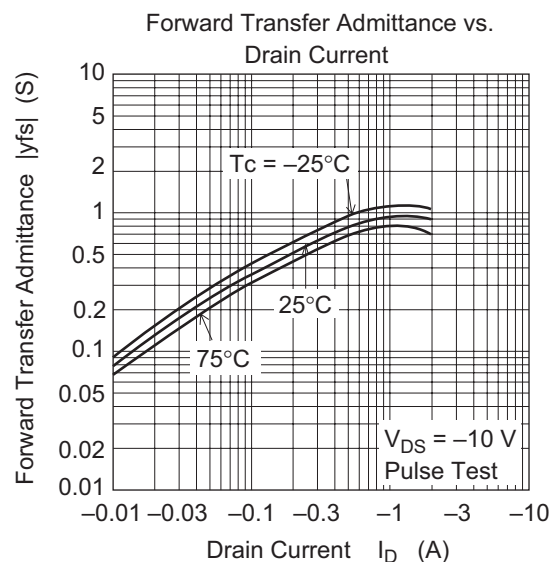
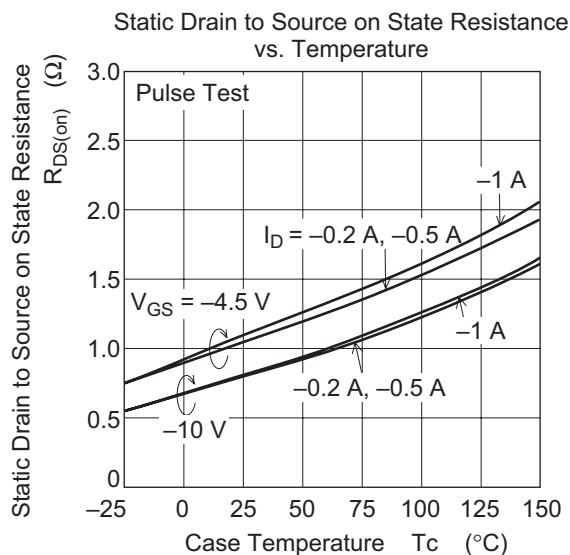
Notes: 4. Pulse test

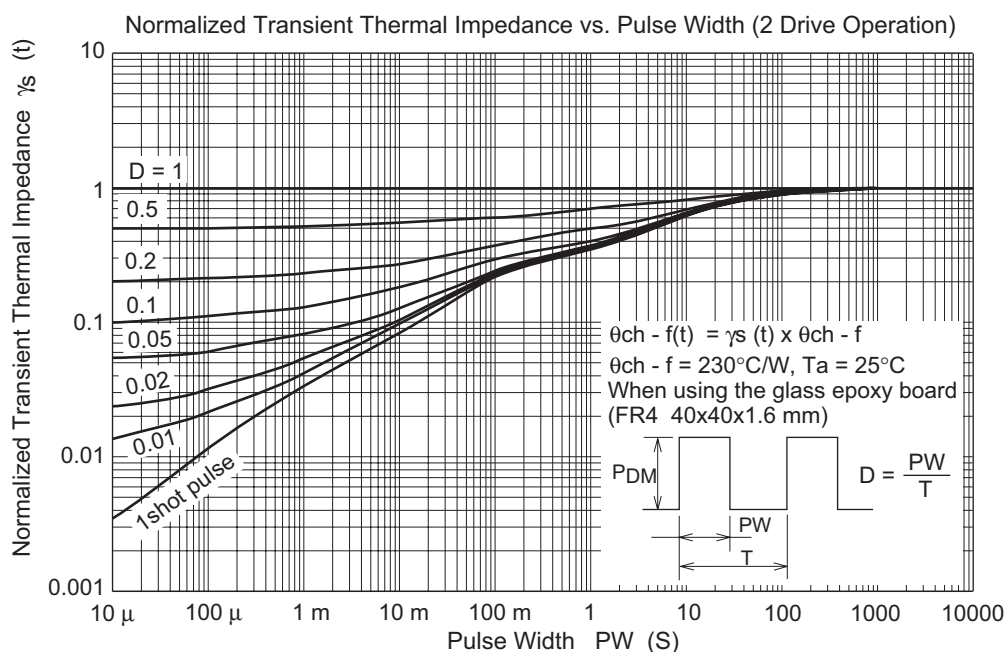
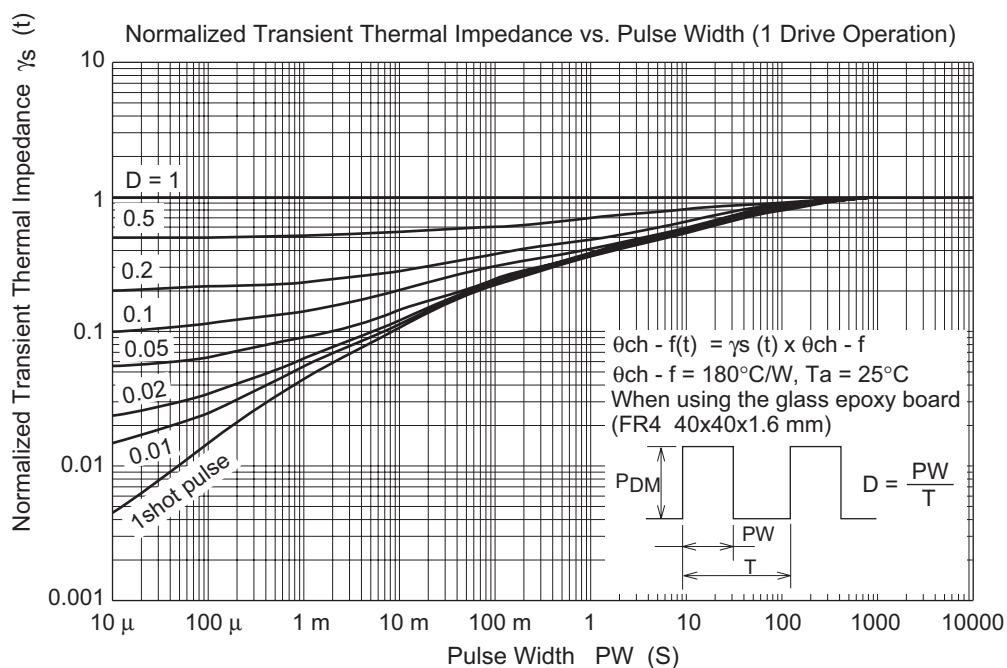
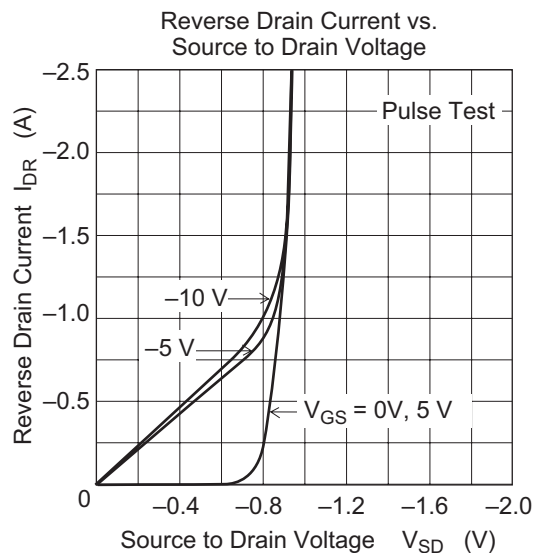
Main Characteristics

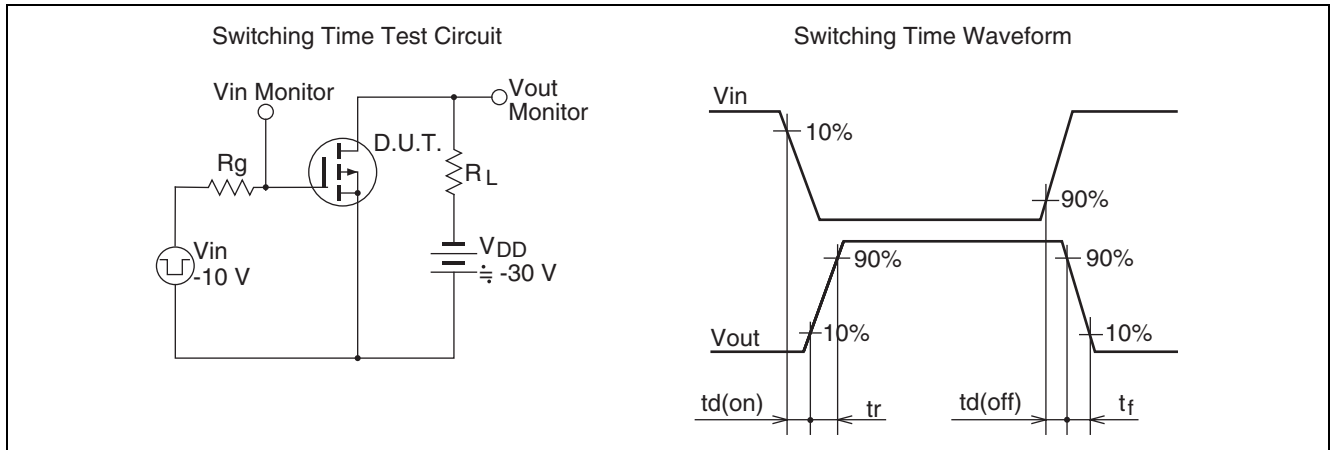


Note 5 :

When using the glass epoxy board
(FR4 40x40x1.6 mm)

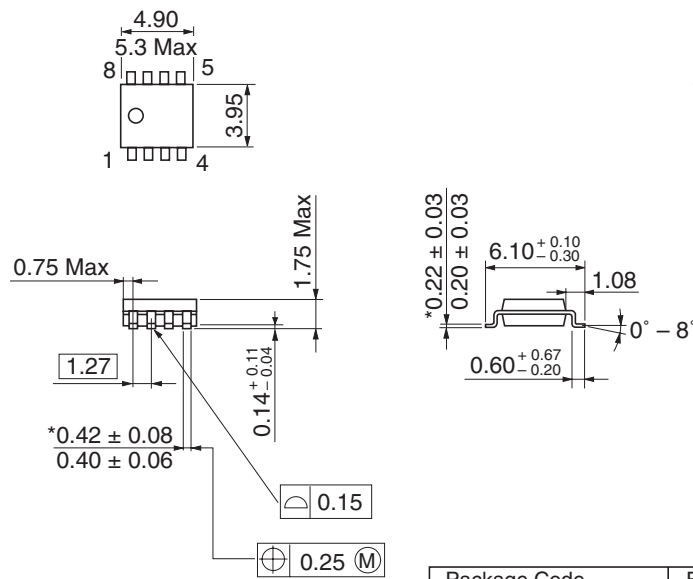






Package Dimensions

As of January, 2003
Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT1110R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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