



FDL100N50F

N-Channel UniFET™ FRFET® MOSFET

500 V, 100 A, 55 mΩ

Features

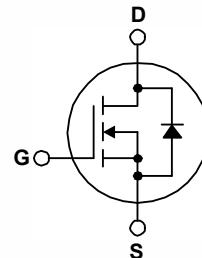
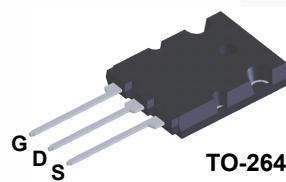
- $R_{DS(on)} = 43 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- Low Gate Charge (Typ. 238 nC)
- Low C_{rss} (Typ. 64 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FDL100N50F	Unit
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	100	A
		- Continuous ($T_C = 100^\circ\text{C}$)	60	
I_{DM}	Drain Current	- Pulsed	(Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy		5000	mJ
I_{AR}	Avalanche Current		(Note 1)	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	2500	W
		- Derate Above 25°C	20	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDL100N50F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.05	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	30	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDL100N50F	FDL100N50F	TO-264	Tube	N/A	N/A	25 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$, $T_C = 25^\circ\text{C}$	500	-	-	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.5	-	V°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	10	μA
		$V_{DS} = 400 \text{ V}$, $T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$	-	0.043	0.055	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 50 \text{ A}$	-	95	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	12000	-	pF
C_{oss}	Output Capacitance		-	1700	-	pF
C_{rss}	Reverse Transfer Capacitance		-	64	-	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V	$V_{DD} = 400 \text{ V}$, $I_D = 50 \text{ A}$,	-	238	-	nC
Q_{gs}	Gate to Source Gate Charge	$V_{GS} = 10 \text{ V}$	-	74	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	95	nC

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}$, $I_D = 50 \text{ A}$,	-	63	-	ns	
t_r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}$, $R_G = 4.7 \Omega$	-	186	-	ns	
$t_{d(\text{off})}$	Turn-Off Delay Time		-	202	-	ns	
t_f	Turn-Off Fall Time		(Note 4)	-	105	-	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	100	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	400	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 100 \text{ A}$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 100 \text{ A}$	-	250	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100 \text{ A}/\mu\text{s}$	-	1.5	-	uC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 1 \text{ mH}$, $I_{AS} = 100 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

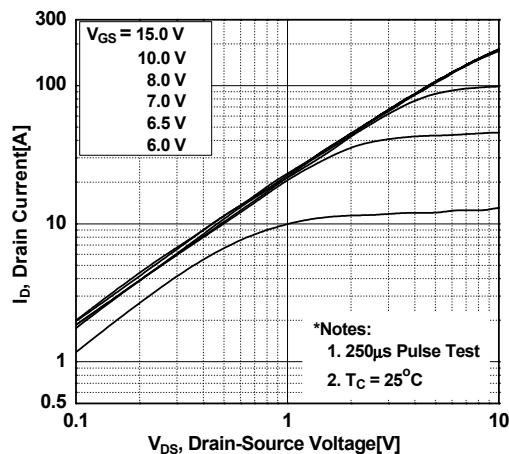


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

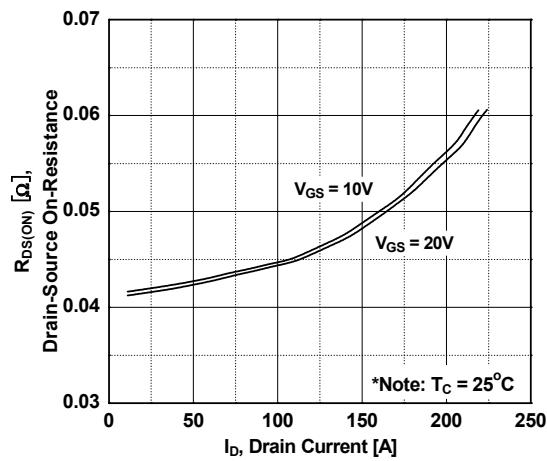


Figure 5. Capacitance Characteristics

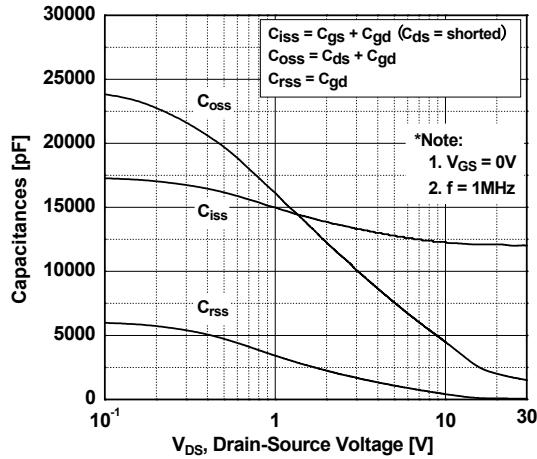


Figure 2. Transfer Characteristics

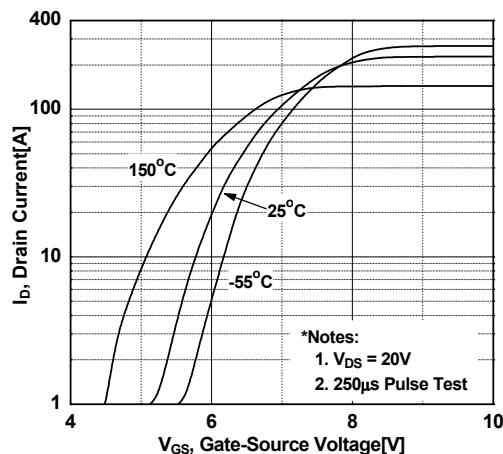


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

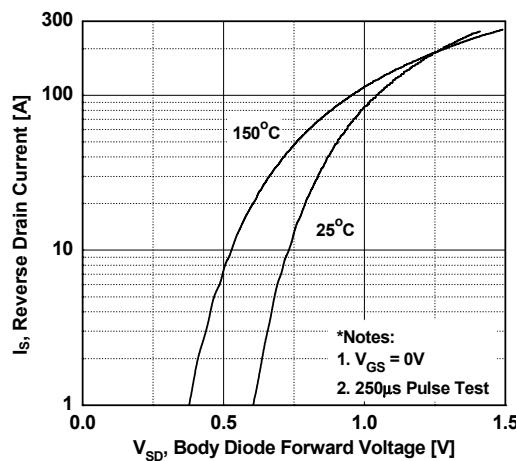
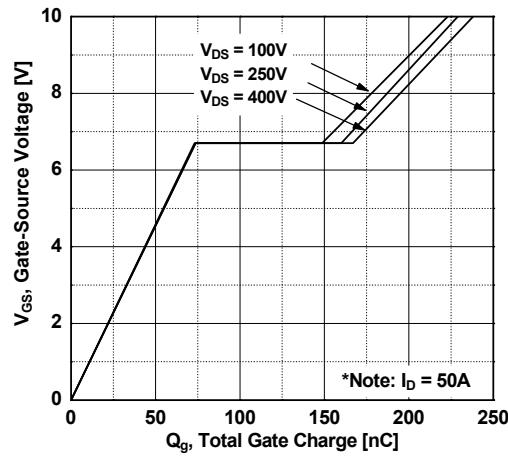


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

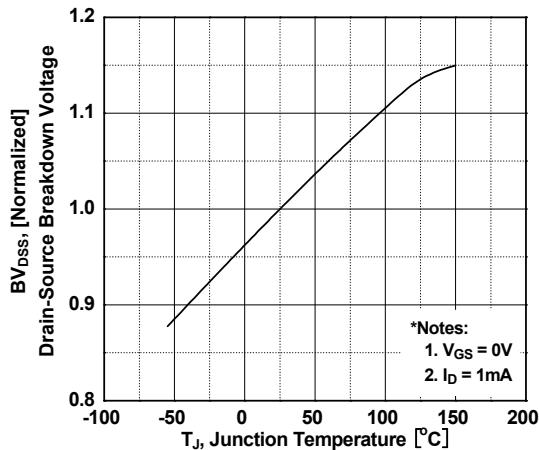


Figure 8. On-Resistance Variation vs. Temperature

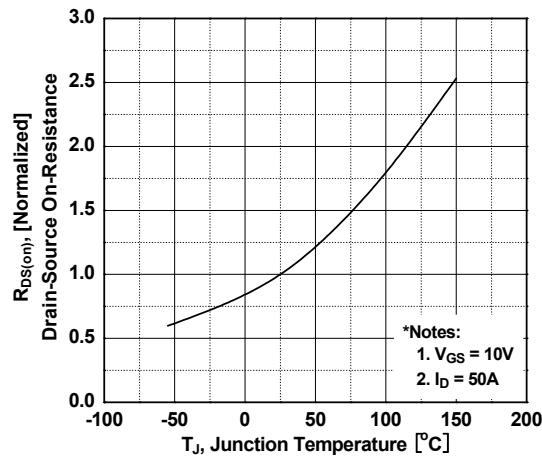


Figure 9. Maximum Safe Operating Area

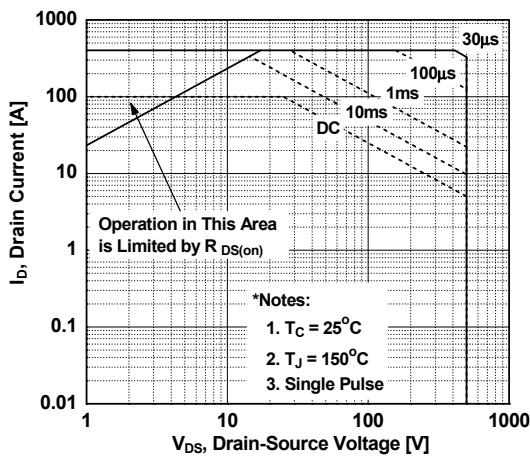


Figure 10. Maximum Drain Current vs. Case Temperature

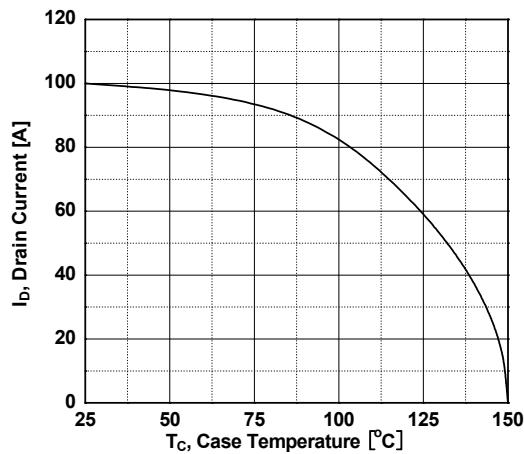
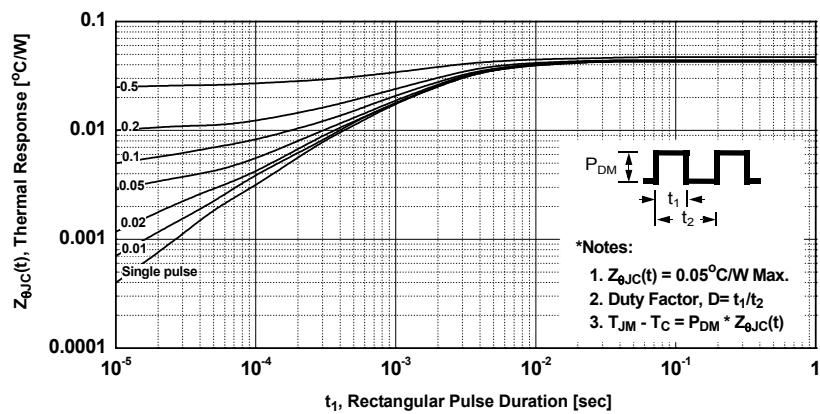


Figure 11. Transient Thermal Response Curve



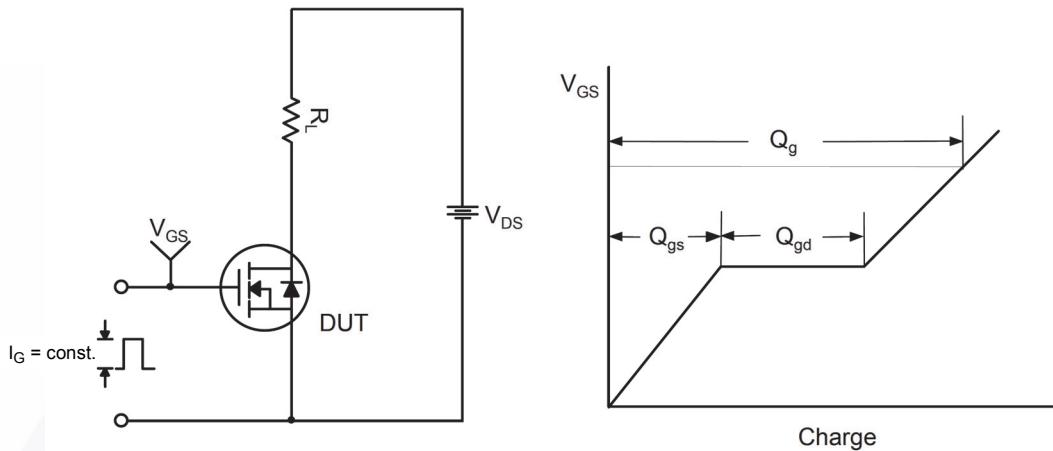


Figure 12. Gate Charge Test Circuit & Waveform

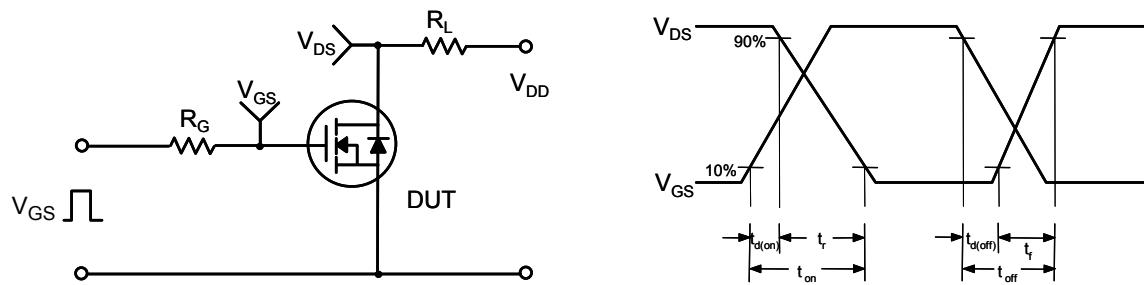


Figure 13. Resistive Switching Test Circuit & Waveforms

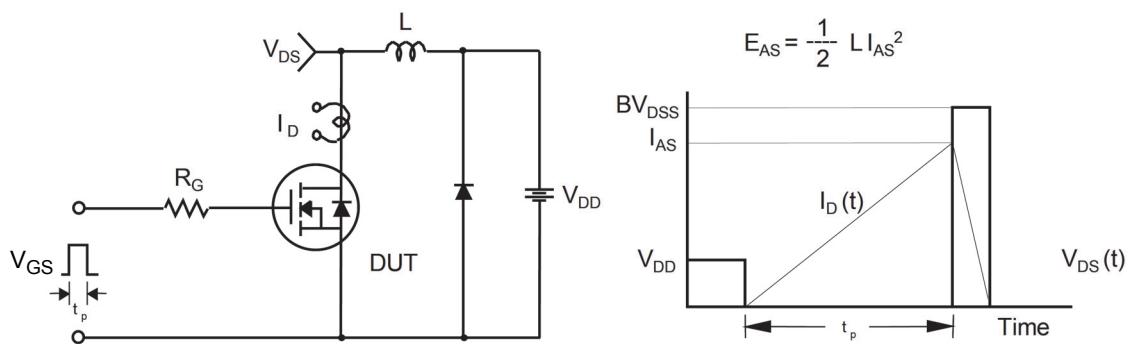


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

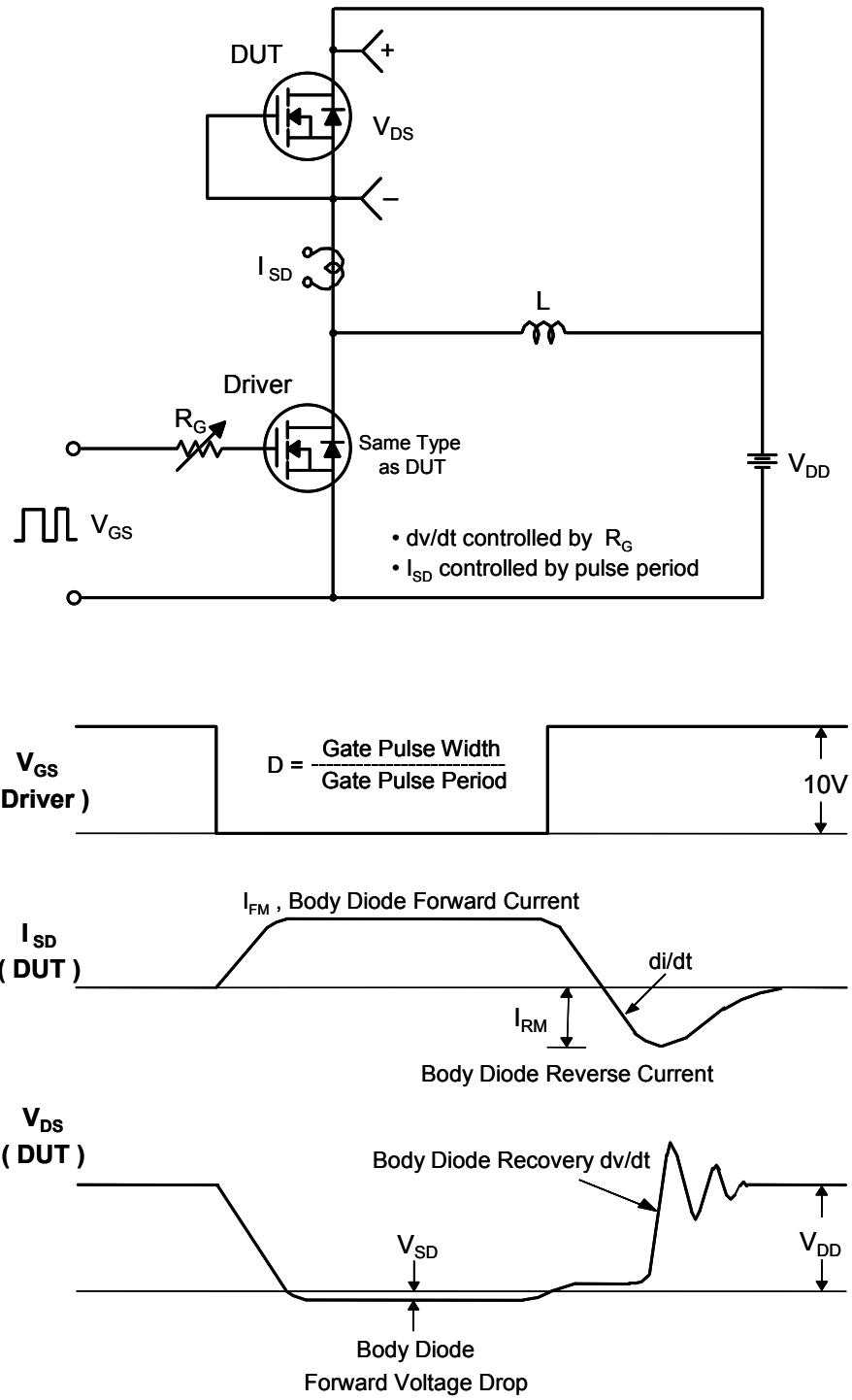


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

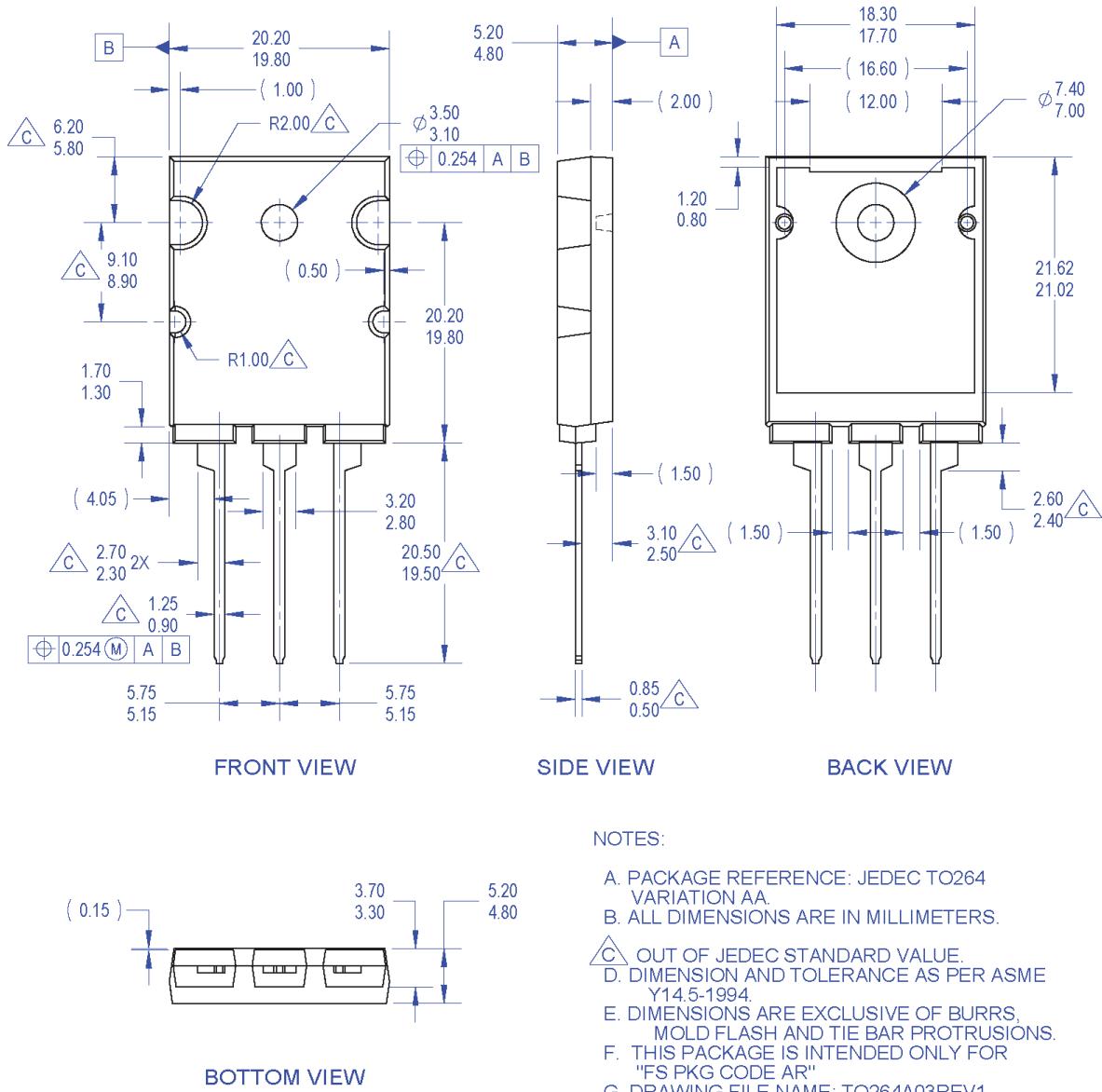


Figure 16. TO264, Molded, 3-Lead, Jedec Variation AA

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