Document Number: MC56F82348
Rev. 1, 10/2013

MC56F82348

MC56F82348

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. Each device combines, on a single chip, the processing power of a DSP and the functionality of an MCU with a flexible set of peripherals to support many target applications:
  - Industrial control
  - Home appliances
  - Smart sensors
  - Wireless charging
  - Power distribution systems
  - Motor control (ACIM, BLDC, PMSM, SR, stepper)
  - Photovoltaic systems
  - Circuit breaker
  - Medical device/equipment
  - Instrumentation

- DSC based on 32-bit 56800EX core
  - Up to 50 MIPS at 50 MHz core frequency
  - DSP and MCU functionality in a unified, C-efficient architecture

- On-chip memory
  - Up to 64 KB flash memory
  - Up to 8 KB data/program RAM
  - On-chip flash memory and RAM can be mapped into both program and data memory spaces

- Analog
  - Two high-speed, 8-channel, 12-bit ADCs with dynamic x1, x2, and x4 programmable amplifier
  - Four analog comparators with integrated 6-bit DAC references
  - Up to two 12-bit digital-to-analog converters (DAC)

- One FlexPWM module with up to 8 PWM outputs

- Communication interfaces
  - Up to two high-speed queued SCI (QSCI) modules with LIN slave functionality
  - Up to two queued SPI (QSPI) modules
  - One I2C/SMBus port
  - One Modular/Scalable Controller Area Network (MSCAN) module

- Timers
  - One 16-bit quad timer (1 x 4 16-bit timer)
  - Two Periodic Interval Timers (PITs)

- Security and integrity
  - Cyclic Redundancy Check (CRC) generator
  - Windowed Computer operating properly (COP) watchdog
  - External Watchdog Monitor (EWM)

- Clocks
  - Two on-chip relaxation oscillators: 8 MHz (400 kHz at standby mode) and 200 kHz
  - Crystal / resonator oscillator

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except for RESETB pin which is a 3.3 V pin only)

- 64-pin LQFP package

Table of Contents

1 Overview

1.1 MC56F82348MLH Product Features

The following table highlights features that differ among members of the family. Features not listed are shared in common by all members of the family.

Table 1. MC56F82348MLH features

	MC56F82348MLH
Core frequency (MHz)	50
Flash memory (KB)	64
RAM (KB)	8
Windowed Computer Operating Properly (WCOP)	1
Periodic Interrupt Timer (PIT)	1
Cyclic Redundancy Check (CRC)	1
Timer (TMR)	4
12-bit Cyclic ADC channels	2x8
PWMA with input capture: High-resolution channels Standard channels	 1x8 0
12-bit DAC	2
DMA	Yes
Analog Comparators (CMP)	4
QSCI	2
QSPI	2
I2C/SMBus	1
MSCAN	1
GPIO	54
Package pin count	64 LQFP

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses

  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 50 million instructions per second (MIPS) at 50 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 50 MHz operation at -40 °C to 125°C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access

- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 32 KB program/data flash memory
  - Up to 4 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- Up to 100 MHz operation clock with PWM Resolution as fine as 10 ns
- PWM module contains four identical submodules, with two outputs per submodule

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.
  - Channels not used for PWM generation can be used for input capture functions.
  - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
  - 2 x 5-channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency up to 10 MHz, having period as low as 100-ns
  - Single conversion time of 10 ADC clock cycles
  - Additional conversion time of 8 ADC clock cycles
- Support of analog inputs for single-ended and differential, including unipolar differential, conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported

- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for simultaneous triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, EWM, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.6 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.7 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.8 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard

- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.10 Modular/Scalable Controller Area Network (MSCAN) Module

- Clock source from PLL or oscillator.
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

1.6.11 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator
  - System bus (IPBus up to 50 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.12 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.13 Phase-locked loop

- Wide programmable output frequency: 200 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.6.14 Clock sources

1.6.14.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.14.2 Crystal oscillator (MC56F82316 only)

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.6.15 Cyclic Redundancy Check (CRC) Generator

- Hardware CRC generator circuit with 16-bit shift register
- High-speed hardware CRC calculation
- Programmable initial seed value
- CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
- Error detection for all single, double, odd, and most multibit errors
- Option to transpose input data or output data (CRC result) bitwise, which is required for certain CRC standards

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

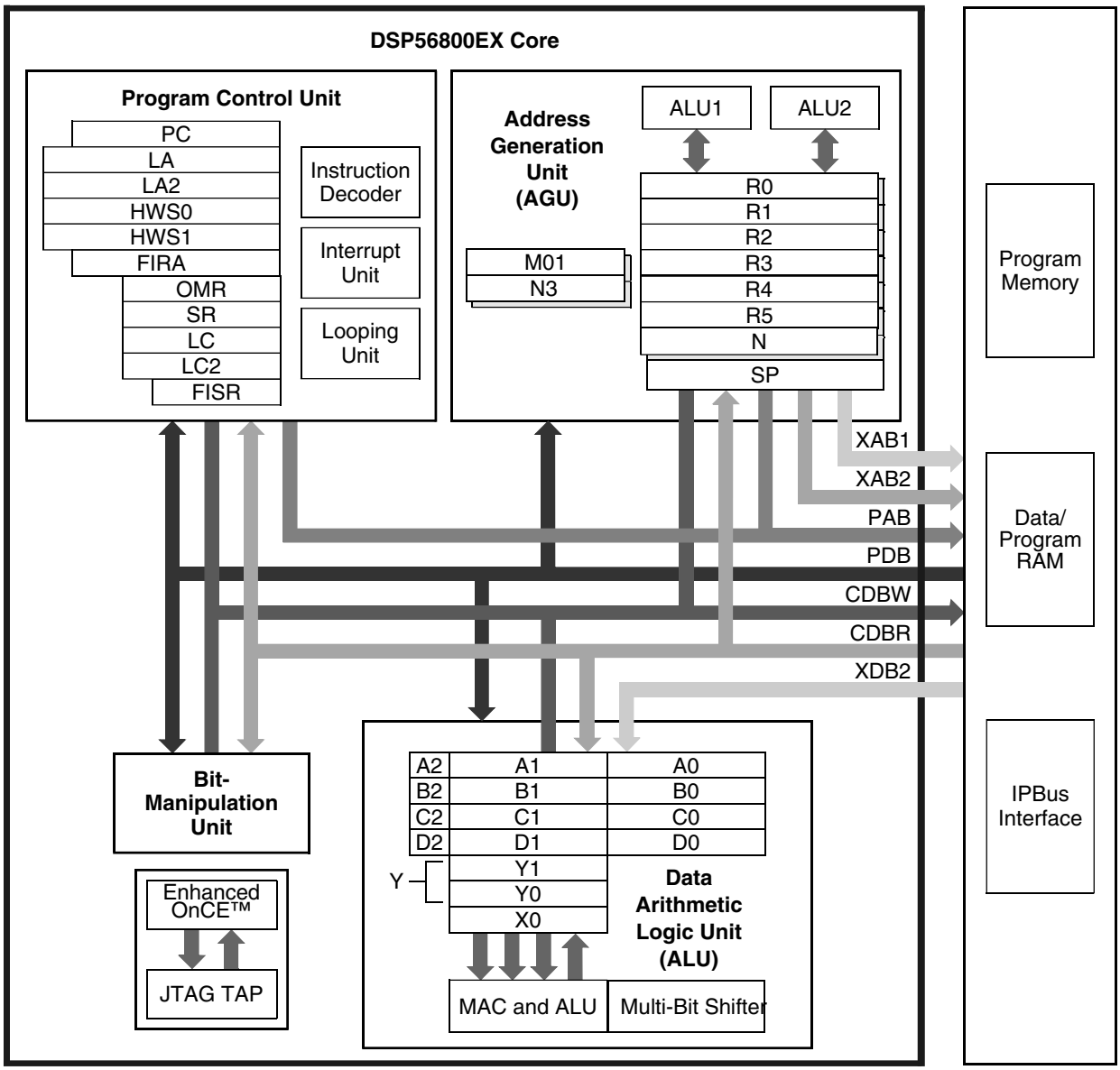


Figure 1. 56800EX basic block diagram

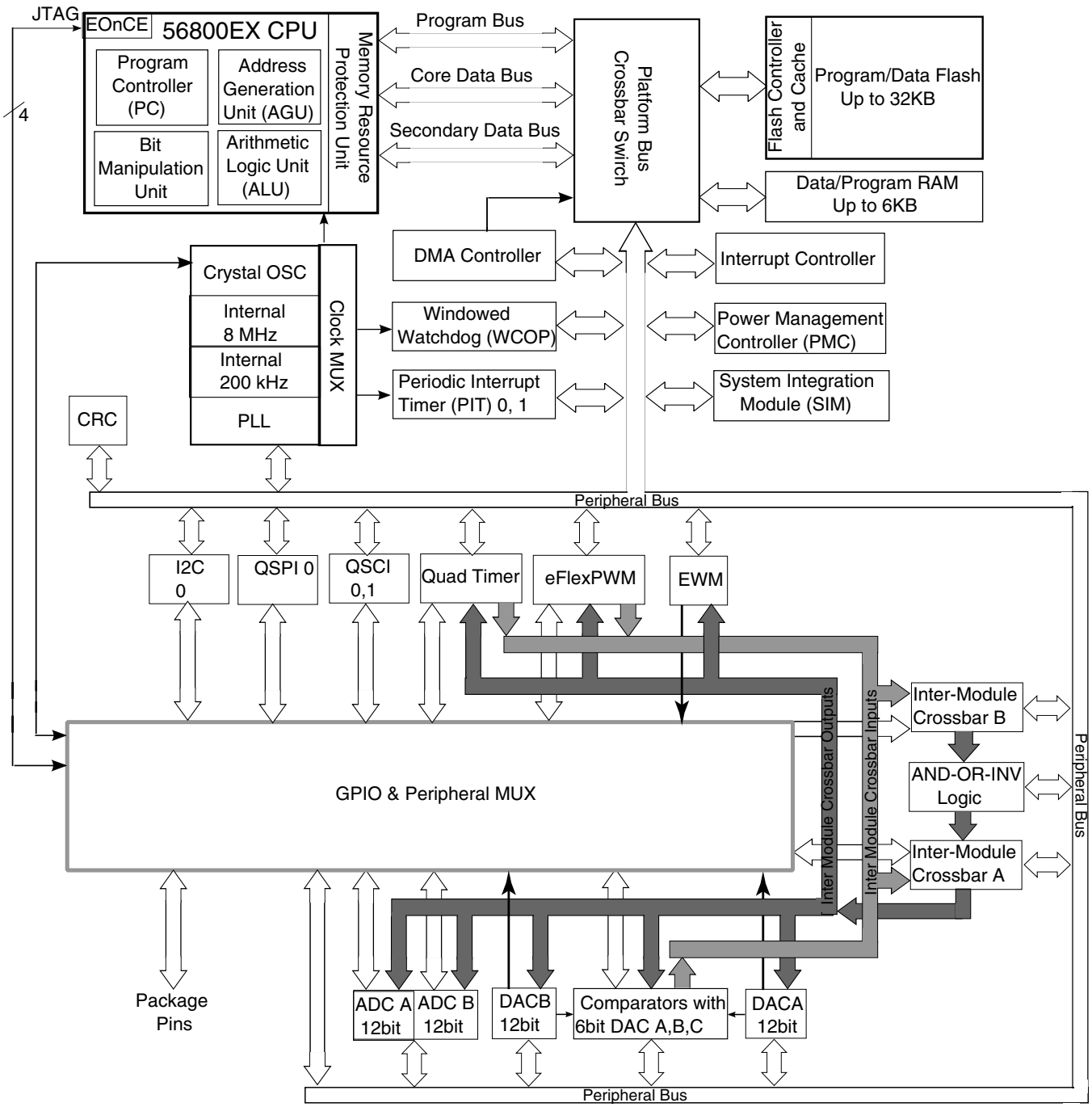


Figure 2. System diagram

2 MC56F82348MLH signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIOx_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA outputs, in cases where the fault conditions originate off-chip.

Table 2. Signal descriptions

Signal Name	64 LQFP	Type	State During Reset	Signal Description
V_{DD}	29	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
	44			
	60			
V_{SS}	30	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
	43			
	61			
V_{DDA}	22	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	23	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	26	On-chip regulator output	On-chip regulator output	Connect a 2.2 µF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation.
	57			
TDI	64	Input	Input, internal pullup enabled	Test Data Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)		Input/ Output		GPIO Port D0
TDO	62	Output	Output	Test Data Output — It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO
(GPIOD1)		Input/ Output	Output	GPIO Port D1
TCK	1	Input	Input, internal pullup enabled	Test Clock Input — The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK
(GPIOD2)		Input/ Output		GPIO Port D2

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
TMS	63	Input	Input, internal pullup enabled	Test Mode Select Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to V_{DD} through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to V_{DD}.
(GPIOD3)		Input/ Output		GPIO Port D3
$\overline{\text{RESET}}$ or RESETB	2	Input	Input, internal pullup enabled	Reset — A direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. After reset, the default state is $\overline{\text{RESET}}$. Recommended a capacitor of up to 0.1 µF for filtering noise.
(GPIOD4)		Input/ Opendrain Output		GPIO Port D4 $\overline{\text{RESET}}$ functionality is disabled in this mode and the device can be reset only through POR, COP reset, or software reset.
GPIOA0	13	Input/ Output	Input, internal pullup enabled	GPIO Port A0
(ANA0&CMPA_IN3)		Input		ANA0 is analog input to channel 0 of ADCA; CMPA_IN3 is positive input 3 of analog comparator A. After reset, the default state is GPIOA0.
(CMPC_O)		Output		Analog comparator C output
GPIOA1	14	Input/ Output	Input, internal pullup enabled	GPIO Port A1: After reset, the default state is GPIOA1.
(ANA1&CMPA_IN0)		Input		ANA1 is analog input to channel 1 of ADCA; CMPA_IN0 is negative input 0 of analog comparator A. When used as an analog input, the signal goes to ANA1 and CMPA_IN0. The ADC control register configures this input as ANA1 or CMPA_IN0.
GPIOA2	15	Input/ Output	Input, internal pullup enabled	GPIO Port A2: After reset, the default state is GPIOA2.
(ANA2&VREFHA&CMPA_IN1)		Input		ANA2 is analog input to channel 2 of ADCA; VREFHA is analog reference high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1.
GPIOA3	16	Input/ Output	Input, internal pullup enabled	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)		Input		ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A.
GPIOA4	12	Input/ Output	Input, internal pullup enabled	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&CMPD_IN0)		Input		ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOA5	11	Input/ Output	Input, internal pullup enabled	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&CMPD_IN1)		Input		ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D.
GPIOA6	10	Input/ Output	Input, internal pullup enabled	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&CMPD_IN2)		Input		ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D.
GPIOA7	9	Input/ Output	Input, internal pullup enabled	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&CMPD_IN3)		Input		ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D.
GPIOB0	24	Input/ Output	Input, internal pullup enabled	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)		Input		ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0.
GPIOB1	25	Input/ Output	Input, internal pullup enabled	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)		Input		ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. The ADC control register configures this input as ANB1.
GPIOB2	27	Input/ Output	Input, internal pullup enabled	GPIO Port B2: After reset, the default state is GPIOB2.
(ANB2&VERFHB&CMPC_IN3)		Input		ANB2 is analog input to channel 2 of ADCB; VREFHB is analog reference high of ADCB; CMPC_IN3 is positive input 3 of analog comparator C. When used as an analog input, the signal goes to both ANB2 and CMPC_IN3.
GPIOB3	28	Input/ Output	Input, internal pullup enabled	GPIO Port B3: After reset, the default state is GPIOB3.
(ANB3&VREFLB&CMPC_IN0)		Input		ANB3 is analog input to channel 3 of ADCB; VREFLB is analog reference low of ADCB; CMPC_IN0 is negative input 0 of analog comparator C.
GPIOB4	21	Input/ Output	Input, internal pullup enabled	GPIO Port B4: After reset, the default state is GPIOB4.
(ANB4&CMPC_IN1)		Input		ANB4 is analog input to channel 4 of ADCB; CMPC_IN1 is negative input 1 of analog comparator C.
GPIOB5	20	Input/ Output	Input, internal pullup enabled	GPIO Port B5: After reset, the default state is GPIOB5.
(ANB5&CMPC_IN2)		Input		ANB5 is analog input to channel 5 of ADCB; CMPC_IN2 is negative input 2 of analog comparator C.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOB6	19	Input/ Output	Input, internal pullup enabled	GPIO Port B6: After reset, the default state is GPIOB6.
(ANB6&CMPB_IN1)		Input		ANB6 is analog input to channel 6 of ADCB; CMPB_IN1 is negative input 1 of analog comparator B.
GPIOB7	17	Input/ Output	Input, internal pullup enabled	GPIO Port B7: After reset, the default state is GPIOB7.
(ANB7&CMPB_IN2)		Input		ANB7 is analog input to channel 7 of ADCB; CMPB_IN2 is negative input 2 of analog comparator B.
GPIOC0	3	Input/ Output	Input, internal pullup enabled	GPIO Port C0: After reset, the default state is GPIOC0.
(EXTAL)		Analog Input		The external crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator.
(CLKIN0)		Input		External clock input 0[1]
GPIOC1	4	Input/ Output	Input, internal pullup enabled	GPIO Port C1: After reset, the default state is GPIOC1.
(XTAL)		Input		The external crystal oscillator output (XTAL) connects the internal crystal oscillator output to an external crystal or ceramic resonator.
GPIOC2	5	Input/ Output	Input, internal pullup enabled	GPIO Port C2: After reset, the default state is GPIOC2.
(TXD0)		Output		SCI0 transmit data output or transmit/receive in single wire operation
(XB_OUT11)		Output		Crossbar module output 11
(XB_IN2)		Input		Crossbar module input 2
(CLKO0)		Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	7	Input/ Output	Input, internal pullup enabled	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)		Input/ Output		Quad timer module A channel 0 input/output
(CMPA_O)		Output		Analog comparator A output
(RXD0)		Input		SCI0 receive data input
(CLKIN1)		Input		External clock input 1
GPIOC4	8	Input/ Output	Input, internal pullup enabled	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)		Input/ Output		Quad timer module A channel 1 input/output
(CMPB_O)		Output		Analog comparator B output
(XB_IN6)		Input		Crossbar module input 6
(EWM_OUT_B)		Output		External Watchdog Module output
GPIOC5	18	Input/ Output	Input, internal pullup enabled	GPIO Port C5: After reset, the default state is GPIOC5.
(DACA_O)		Analog Output		12-bit digital-to-analog output
(XB_IN7)		Input		Crossbar module input 7

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOC6	31	Input/ Output	Input, internal pullup enabled	GPIO Port C6: After reset, the default state is GPIOC6.
(TA2)		Input/ Output		Quad timer module A channel 2 input/output
(XB_IN3)		Input		Crossbar module input 3
(CMP_REF)		Analog Input		Positive input 3 of analog comparator A and B and C.
($\overline{SS0\_B}$)		Input/ Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received.
GPIOC7	32	Input/ Output	Input, internal pullup enable	GPIO Port C7: After reset, the default state is GPIOC7.
($\overline{SS0\_B}$)		Input/ Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module 0 that the current transfer is to be received.
(TXD0)		Output		SCI0 transmit data output or transmit/receive in single wire operation
(XB_IN8)		Input		Crossbar module input 8
GPIOC8	33	Input/ Output	Input, internal pullup enabled	GPIO Port C8: After reset, the default state is GPIOC8.
(MISO0)		Input/ Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)		Input		SCI0 receive data input
(XB_IN9)		Input		Crossbar module input 9
(XB_OUT6)		Output		Crossbar module output 6
GPIOC9	34	Input/ Output	Input, internal pullup enabled	GPIO Port C9: After reset, the default state is GPIOC9.
(SCLK0)		Input/ Output		SPI0 serial clock. In master mode, SCLK0 pin is an output, clocking slaved listeners. In slave mode, SCLK0 pin is the data clock input.
(XB_IN4)		Input		Crossbar module input 4
(TXD0)		Output		SCI0 transmit data output or transmit/receive in single wire operation
(XB_OUT8)		Output		Crossbar module output 8
GPIOC10	35	Input/ Output	Input, internal pullup enabled	GPIO Port C10: After reset, the default state is GPIOC10.
(MOSI0)		Input/ Output		Master out/slave in for SPI0 — In master mode, MOSI0 pin is the data output. In slave mode, MOSI0 pin is the data input.
(XB_IN5)		Input		Crossbar module input 4
(MISO0)		Input/ Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(XB_OUT9)		Output		Crossbar module output 9

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOC11	37	Input/ Output	Input, internal pullup enabled	GPIO Port C11: After reset, the default state is GPIOC11.
(CANTX)		Open-drain Output		CAN transmit data output
(SCL0)		Input/ Open-drain Output		I^2C0 serial clock
(TXD1)		Output		SCI1 transmit data output or transmit/receive in single wire operation
GPIOC12	38	Input/ Output	Input, internal pullup enabled	GPIO Port C12: After reset, the default state is GPIOC12.
(CANRX)		Input		CAN receive data input
(SDA0)		Input/ Open-drain Output		I^2C0 serial data line
(RXD1)		Input		SCI1 receive data input
GPIOC13	49	Input/ Output	Input, internal pullup enabled	GPIO Port C13: After reset, the default state is GPIOC13.
(TA3)		Input/ Output		Quad timer module A channel 3 input/output
(XB_IN6)		Input		Crossbar module input 6
(EWM_OUT_B)		Output		External Watchdog Module output
GPIOC14	55	Input/ Output	Input, internal pullup enabled	GPIO Port C14: After reset, the default state is GPIOC14.
(SDA0)		Input/ Opendrain Output		I^2C0 serial data line
(XB_OUT4)		Output		Crossbar module output 4
(PWM_FAULT4)		Input		Disable PWMA output 4
GPIOC15	56	Input/ Output	Input, internal pullup enabled	GPIO Port C15: After reset, the default state is GPIOC15.
(SCL0)		Input/ Open-drain Output		I^2C0 serial clock
(XB_OUT5)		Output		Crossbar module output 5
(PWM_FAULT5)		Input		Disable PWMA output 5
GPIOE0	45	Input/ Output	Input, internal pullup enabled	GPIO Port E0: After reset, the default state is GPIOE0.
(PWM_0B)		Input/ Output		PWM module A (NanoEdge), submodule 0, output B or input capture B
GPIOE1	46	Input/ Output	Input, internal pullup enabled	GPIO Port E1: After reset, the default state is GPIOE1.
(PWM_0A)		Input/ Output		PWM module A (NanoEdge), submodule 0, output A or input capture A

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOE2	47	Input/ Output	Input, internal pullup enabled	GPIO Port E2: After reset, the default state is GPIOE2.
(PWMA_1B)		Input/ Output		PWM module A (NanoEdge), submodule 1, output B or input capture B
GPIOE3	48	Input/ Output	Input, internal pullup enabled	GPIO Port E3: After reset, the default state is GPIOE3.
(PWMA_1A)		Input/ Output		PWM module A (NanoEdge), submodule 1, output A or input capture A
GPIOE4	51	Input/ Output	Input, internal pullup enabled	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)		Input/ Output		PWM module A (NanoEdge), submodule 2, output B or input capture B
(XB_IN2)		Input		Crossbar module input 2
GPIOE5	52	Input/ Output	Input, internal pullup enabled	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)		Input/ Output		PWM module A (NanoEdge), submodule 2, output A or input capture A
(XB_IN3)		Input		Crossbar module input 3
GPIOE6	53	Input/ Output	Input, internal pullup enabled	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)		Input/ Output		PWM module A (NanoEdge), submodule 3, output B or input capture B
(XB_IN4)		Input		Crossbar module input 4
GPIOE7	54	Input/ Output	Input, internal pullup enabled	GPIO Port E7: After reset, the default state is GPIOE7.
(PWMA_3A)		Input/ Output		PWM module A (NanoEdge), submodule 3, output A or input capture A
(XB_IN5)		Input		Crossbar module input 5
GPIOF0	36	Input/ Output	Input, internal pullup enabled	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)		Input		Crossbar module input 6
(SCLK1)		Input/ Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	50	Input/ Output	Input, internal pullup enabled	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)		Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)		Input		Crossbar module input 7
(CMPD_O)		Output		Analog comparator D output

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOF2	39	Input/ Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)		Input/ Open-drain Output		I^2C0 serial clock
(XB_OUT6)		Output		Crossbar module output 6
(MISO1)		Input/ Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOF3	40	Input/ Output	Input, internal pullup enabled	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)		Input/ Open-drain Output		I^2C0 serial data line
(XB_OUT7)		Output		Crossbar module output 7
(MOSI1)		Input/ Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.
GPIOF4	41	Input/ Output	Input, internal pullup enabled	GPIO Port F4: After reset, the default state is GPIOF4.
(TXD1)		Output		SCI1 transmit data output or transmit/receive in single wire operation
(XB_OUT8)		Output		Crossbar module output 8
(PWMA_0X)		Input/ Output		PWM module A (NanoEdge), submodule 0, output X or input capture X
(PWMA_FAULT 6)		Input		Disable PWMA output 6
GPIOF5	42	Input/ Output	Input, internal pullup enabled	GPIO Port F5: After reset, the default state is GPIOF5.
(RXD1)		Input		SCI1 receive data input
(XB_OUT9)		Output		Crossbar module output 9
(PWMA_1X)		Input/ Output		PWM module A (NanoEdge), submodule 1, output X or input capture X
(PWMA_FAULT 7)		Input		Disable PWMA output 7
GPIOF6	58	Input/ Output	Input, internal pullup enabled	GPIO Port F6: After reset, the default state is GPIOF6.
(PWMA_3X)		Input/ Output		PWM module A (NanoEdge), submodule 3, output X or input capture X
(XB_IN2)		Input		Crossbar module input 2

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOF7	59	Input/ Output	Input, internal pullup enabled	GPIO Port F7: After reset, the default state is GPIOF7.
(CMPC_O)		Output		Analog comparator C output
(SS1_B)		Input/ Output		In slave mode, SS1_B indicates to the SPI1 module that the current transfer is to be received.
(XB_IN3)		Input		Crossbar module input 3
GPIOF8	6	Input/ Output	Input, internal pullup enabled	GPIO Port F8: After reset, the default state is GPIOF8.
(RXD0)		Input		SCI0 receive data input
(XB_OUT10)		Output		Crossbar module output 10
(CMPD_O)		Output		Analog comparator D output
(PWMA_2X)				PWM module A (NanoEdge), submodule 2, output X or input capture X

1. If CLKIN is selected as the device's external clock input, then both the GPS_C0 bit (in GPS1) and the EXT_SEL bit (in OCCS oscillator control register (OSCTL)) must be set. Also, the crystal oscillator should be powered down.

3 Signal groups

The input and output signals of the MC56F82348MLH are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 64LQFP
Power Inputs (V_{DD}, V_{DDA}), Power output(V_{CAP})	6
Ground (V_{SS}, V_{SSA})	4
Reset	1
eFlexPWM with NanoEdge ports not including fault pins (for 56F827xx)	8
eFlexPWM without NanoEdge ports not including fault pins	4
Queued Serial Peripheral Interface (QSPI0 and QSPI1) ports	9
Queued Serial Communications Interface (QSCI0 and QSCI1) ports	10
Inter-Integrated Circuit Interface (I^2C0) ports	6
12-bit Analog-to-Digital Converter inputs	16
Analog Comparator inputs/outputs	17/5
12-bit Digital-to-Analog output	2
Quad Timer Module (TMRA and TMRB) ports	4
Controller Area Network (MSCAN)	2

Table continues on the next page...

Table 3. Functional Group Pin Allocations (continued)

Functional Group	Number of Pins in 64LQFP
Inter-Module Crossbar inputs/outputs	17/11
Clock inputs/outputs	2/2
JTAG / Enhanced On-Chip Emulation (EOnCE)	4

4 Ordering parts

4.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: MC56F82

5 Part identification

5.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

5.2 Format

Part numbers for this device have the following format: Q 56F8 2 C F P T PP N

5.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
2	DSC subfamily	• 2
C	Maximum CPU frequency (MHz)	• 3 = 50 MHz
F	Primary program flash memory size	• 4 = 64 KB
P	Pin count	• 8 = 64
T	Temperature range (°C)	• M = –40 to 125
PP	Package identifier	• LH = 64LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

6 Terminology and guidelines

6.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

6.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

6.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

6.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

6.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

6.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

6.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

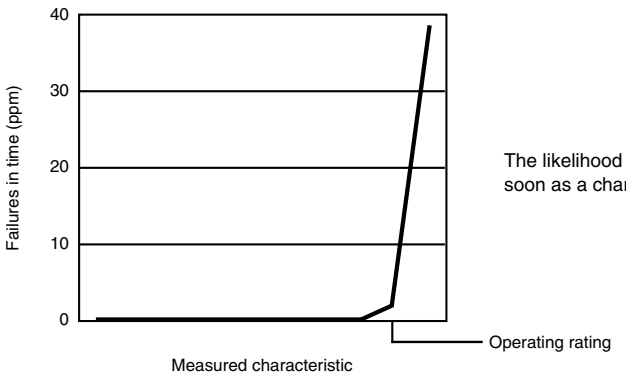
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

6.4.1 Example

This is an example of an operating rating:

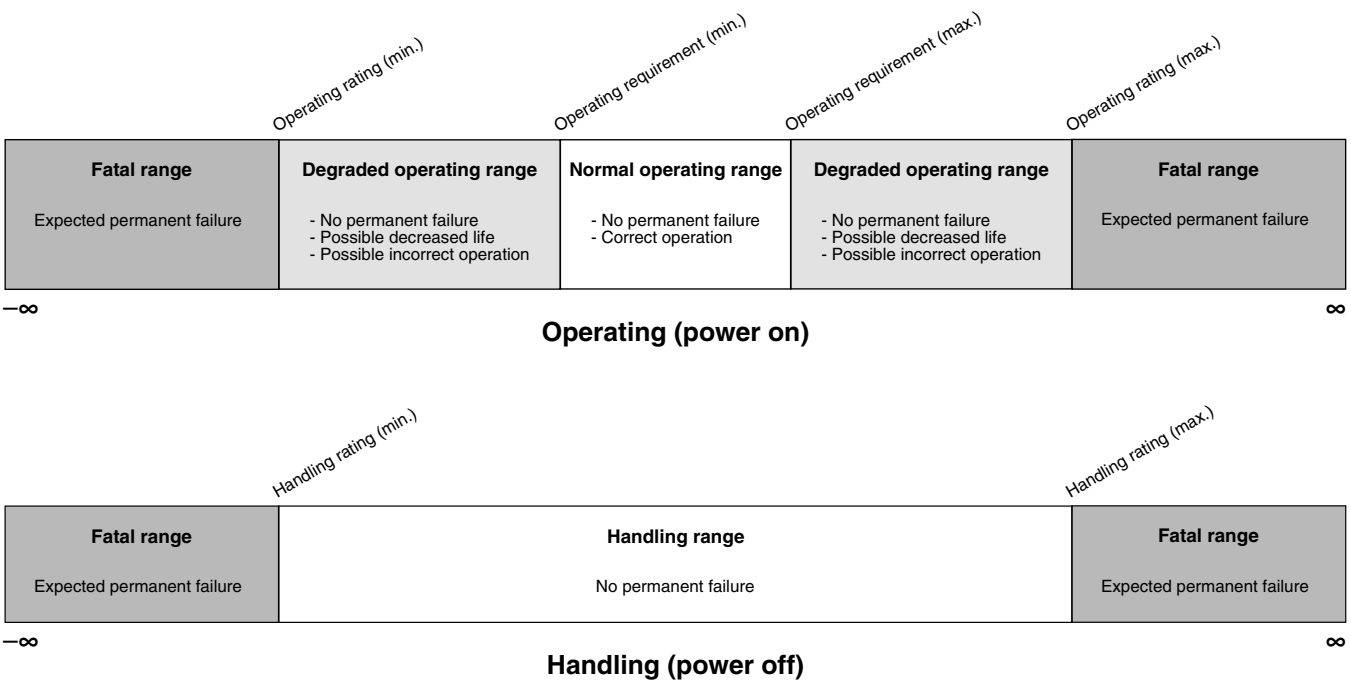
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

6.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

6.6 Relationship between ratings and operating requirements



6.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

6.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

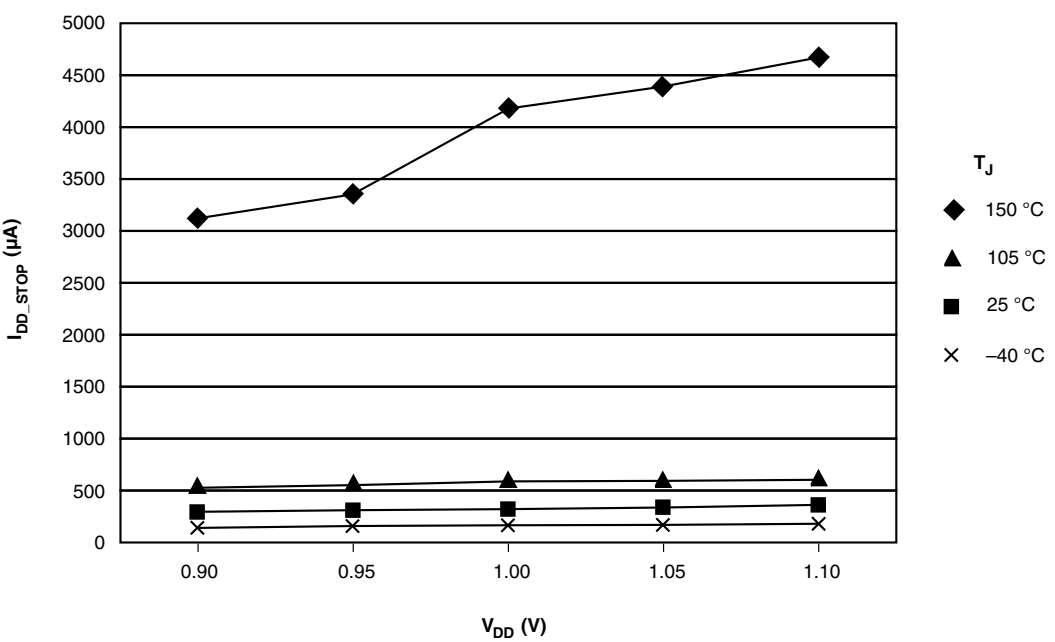
6.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

6.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



6.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

7 Ratings

7.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

7.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

7.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 4. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

7.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device.

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature Industrial	T_A		-40	125	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than VDIO_MIN (= V_{SS}–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

8 General

8.1 General characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except for the $\overline{\text{RESET}}$ pin which is 3.3V only. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum

voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 5 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: V_{SS}=V_{SSA}=0V, V_{DD}=V_{DDA}=3.0V to 3.6V, CL≤50 pF, f_{OP}=50MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

8.2 AC electrical characteristics

Tests are conducted using the input levels specified in Table 8. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

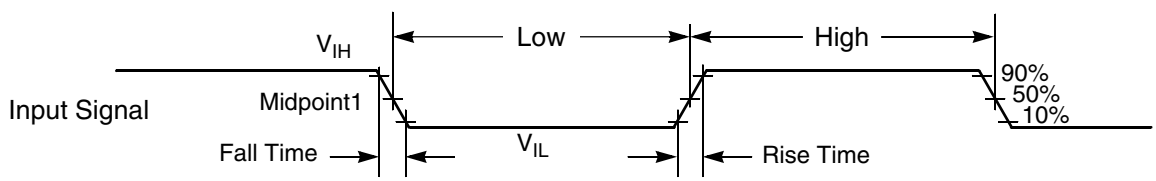


Figure 3. Input signal measurement references

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

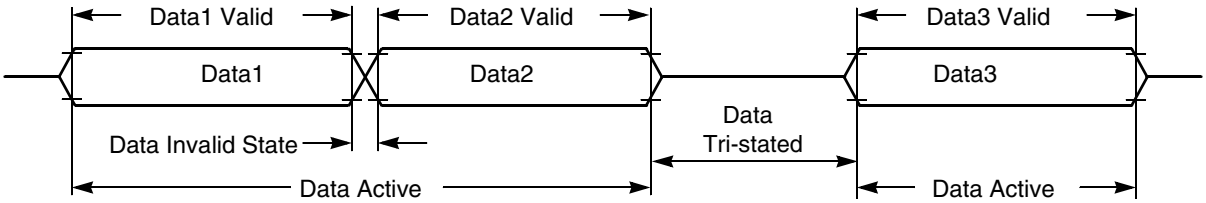


Figure 4. Signal states

8.3 Nonswitching electrical specifications

8.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA}-0.6		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output

2. ADC (Cyclic) specifications are not guaranteed when V_{DDA} is below 3.0 V.
3. When ambient temperature is below 105°C, total IO sink current and total IO source current are limited to 75 mA each

   When ambient temperature is above 105°C, total IO sink current and total IO source current are limited to 36 mA combined
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

8.3.2 LVD and POR operating requirements

Table 7. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

8.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

Table 8. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High	I_{IH}	Pin Group 1	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
pull-up enabled or disabled		Pin Group 2					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	—	50	kΩ	—
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	—	50	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V

Table continues on the next page...

Table 8. DC Electrical Characteristics at Recommended Operating Conditions (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ || C_{LD} = 400 pF
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

8.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 9. Reset, stop, wait, and interrupt timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 µF on $\overline{\text{RESET}}$.

NOTE

In Table 9, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 50MHz, T=20 ns. At 4 MHz (used coming out of reset and stop modes), T=250 ns.

Table 10. Power mode transition behavior

Symbol	Description	Min	Max	Unit	Notes[1]
T_{POR}	After a POR event, the amount of delay from when V_{DD} reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
	STOP mode to RUN mode	6.81		µs	2
	LPS mode to LPRUN mode	240.9	810	µs	3
	VLPS mode to VLPRUN mode	1424	1459	µs	4
	WAIT mode to RUN mode	0.570	0.620	µs	5
	LPWAIT mode to LPRUN mode	237.2	810	µs	3
	VLPWAIT mode to VLPRUN mode	1413	1500	µs	4

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is 8 MHz IRC in normal mode.
3. CPU clock = 200 KHz and 8 MHz IRC on standby. Exit by an interrupt on PORTC GPIO.
4. Using 64 KHz external clock; CPU Clock = 32KHz. Exit by an interrupt on PortC GPIO.
5. Clock configuration: CPU and system clocks= 50 MHz. Bus Clock = 50 MHz. .Exit by interrupt on PORTC GPIO

8.3.5 Power consumption operating behaviors

Table 11. Current Consumption

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25 °C		Maximum at 3.6 V, 125 °C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	50 MHz	• 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock • ADC/DAC (only one 12 bit DAC and all 6 bit DAC) powered on and clocked • Comparator powered on	27.6 mA	9.9 mA	43.5 mA	14 mA
WAIT	50 MHz	• 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 2X clock • ADC/DAC (single 12 bit DAC, all 6 bit DAC), Comparator powered off	24.0 mA	—	41.3 mA	—

Table continues on the next page...

Table 11. Current Consumption (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25 °C		Maximum at 3.6 V, 125 °C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
STOP	4 MHz	• 4 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/DAC/Comparator powered off	6.3 mA	—	19.4 mA	—
LPRUN (LsRUN)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • Repeat NOP instructions • All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12 bit DAC and all 6 bit DAC enabled. [2] • Simple loop with running from platform instruction buffer	2.8 mA	3.1 mA	13 mA	4 mA
LPWAIT (LsWAIT)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12 bit DAC and all 6 bit DAC enabled.[2] • Processor core in wait mode	2.7 mA	3.1 mA	13 mA	4 mA
LPSTOP (LsSTOP)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock • ROSC in standby mode • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off[2] • Processor core in stop mode	1.2 mA	—	12 mA	—
VLPRUN	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer	0.7 mA	—	10 mA	—

Table continues on the next page...

Table 11. Current Consumption (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25 °C		Maximum at 3.6 V, 125 °C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
VLPWAIT	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode	0.7 mA	—	10 mA	—
VLPSTOP	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby. • Small regulator is disabled. • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode	0.7 mA	—	10 mA	—

1. No output switching, all ports configured as inputs, all inputs low, no DC loads
2. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:2 between the CPU clock and the flash clock when running with 2 MHz external clock input and CPU running at 1 MHz.

8.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

8.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

8.4 Switching specifications

8.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 50 50	MHz	
f_{BUS}	Bus clock	—	50	MHz	

8.4.2 General switching timing

Table 14. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	2
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	3
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	3
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	4
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	4

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. The greater synchronous and asynchronous timing must be met.
3. 75 pF load
4. 15 pF load

8.5 Thermal specifications

8.5.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	135	°C
T_A	Ambient temperature (extended industrial)	–40	125	°C

8.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See Thermal design considerations for more detail on thermal design considerations.

Board type	Symbol	Description	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	64	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	39	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	°C/W	5

Table continues on the next page...

Board type	Symbol	Description	64 LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

9 Peripheral operating requirements and behaviors

9.1 Core modules

9.1.1 JTAG timing

Table 16. JTAG timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/8	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

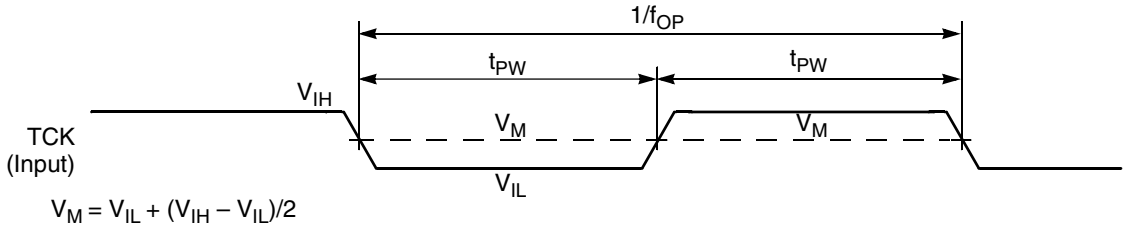


Figure 5. Test clock input timing diagram

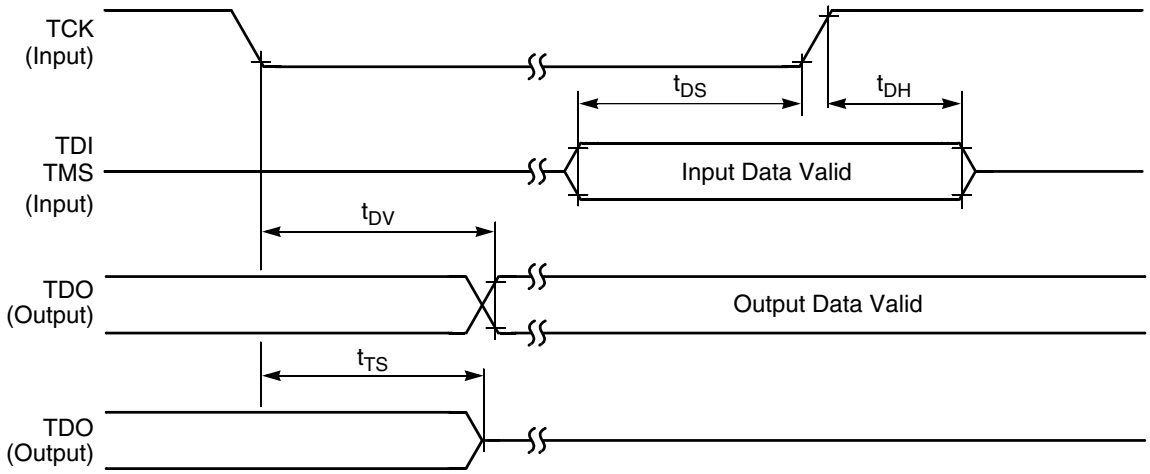


Figure 6. Test access port timing diagram

9.2 System modules

9.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the MC56F82xxx's core logic. For proper operations, the voltage regulator requires an external 2.2 µF capacitor on each V_{CAP} pin. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 17.

Table 17. Regulator 1.2 V parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600		mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 18. Bandgap electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

9.3 Clock modules

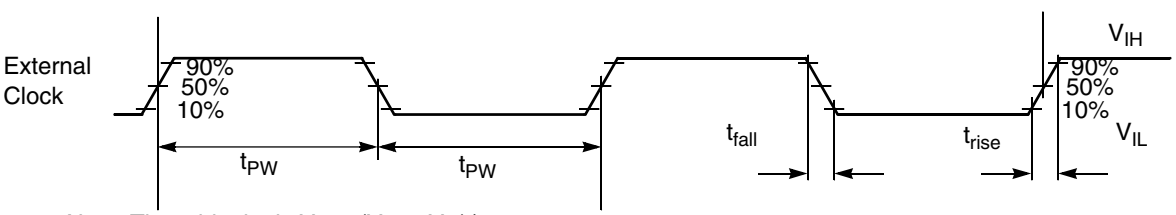
9.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 19. External clock operation timing requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

1. See Figure 7 for detail on using the recommended connection of an external clock driver.
2. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 7. External clock timing

9.3.2 Phase-Locked Loop timing

Table 20. Phase-Locked Loop timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	8	8	16	MHz
PLL output frequency[2]	f_{op}	200	—	400	MHz
PLL lock time[3]	t_{plls}	35.5		73.2	µs

Table continues on the next page...

Table 20. Phase-Locked Loop timing (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Allowed Duty Cycle of input reference	t_{dc}	40	50	60	%

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
2. The frequency of the core system clock cannot exceed 50 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
3. This is the time required *after the PLL is enabled* to ensure reliable operation.

9.3.3 External crystal or resonator requirement

Table 21. Crystal or resonator requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

9.3.4 Relaxation Oscillator Timing

Table 22. Relaxation Oscillator Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1]					
RUN Mode					
• 0°C to 105°C		7.84	8	8.16	MHz
• -40°C to 125°C		7.70	8	8.26	
Standby Mode (IRC trimmed @ 8 MHz)					
• -40°C to 125°C		195	200	390	kHz
8 MHz Frequency Variation over 25°C					
RUN Mode					
Due to temperature					
• 0°C to 105°C			+/-1.5	+/-2	%
• -40°C to 125°C			—	+/-3.6	
200 kHz Output Frequency[2]					
RUN Mode					
• -40°C to 125°C		194	200	206	kHz

Table continues on the next page...

Table 22. Relaxation Oscillator Electrical Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
200 kHz Output Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 85°C • -40°C to 125°C			 +/-1.5 +/-1.5	 +/-2 +/-3	 %
Stabilization Time • 8 MHz output[3] • 200 kHz output[4]	tstab		 0.12 10		 µs
Output Duty Cycle		48	50	52	%

1. Frequency after application of 8 MHz trim
2. Frequency after application of 200 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

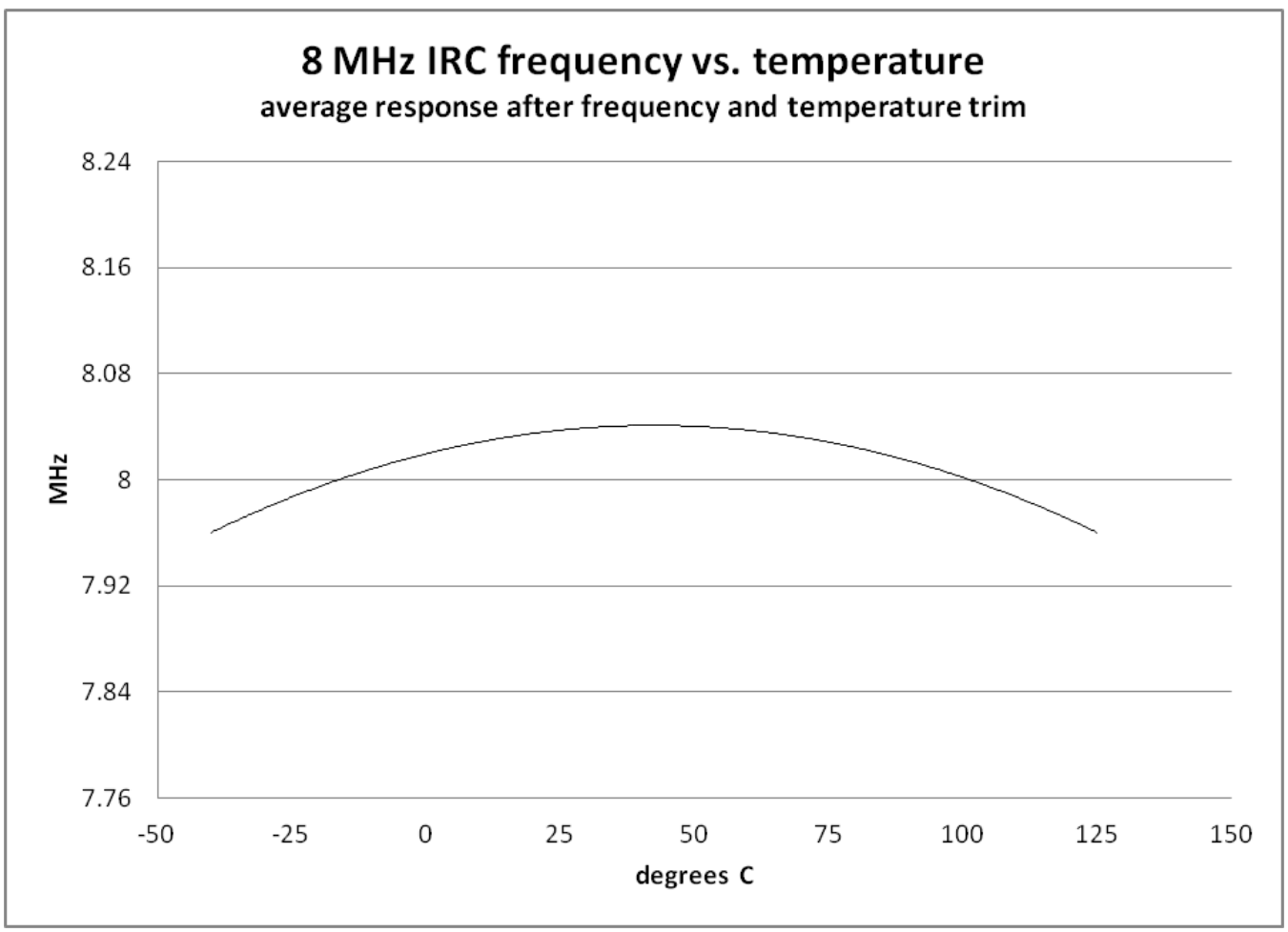


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

9.4 Memories and memory interfaces

9.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

9.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

9.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

9.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

9.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

9.5 Analog

9.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 27. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	VDDA	3	3.3	3.6	V
VREFH (in external reference mode)	Vrefhx	VDDA-0.6		VDDA	V
ADC Conversion Clock[2]	f_{ADCCLK}	0.1		10	MHz
Conversion Range[3] Fully Differential Single Ended/Unipolar	R_{AD}	 $-(V_{REFH} - V_{REFL})$ V_{REFL}		 $V_{REFH} - V_{REFL}$ V_{REFH}	V
Input Voltage Range (per input)[4] External Reference Internal Reference	V_{ADIN}	V_{REFL} 0		V_{REFH} V_{DDA}	V
Timing and Power					

Table continues on the next page...

Table 27. 12-bit ADC Electrical Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Conversion Time[5]	t_{ADC}		8		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block)	I_{ADRUN}		1.8		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.1		µA
V_{REFH} Current (in external mode)	I_{VREFH}		190	225	µA
Accuracy (DC or Absolute)					
Integral non-Linearity[6]	INL		+/- 1.5	+/- 2.5	LSB[7]
Differential non-Linearity	DNL		+/- 0.5	+/- 0.8	LSB
Monotonicity			GUARANTEED		
Offset[8] Fully Differential Single Ended/Unipolar	V_{OFFSET}		 +/- 8 +/- 12		mV
Gain Error	E_{GAIN}		0.996 to1.004	0.99 to 1.101	
AC Specifications[9]					
Signal to Noise Ratio	SNR		66		dB
Total Harmonic Distortion	THD		75		dB
Spurious Free Dynamic Range	SFDR		77		dB
Signal to Noise plus Distortion	SINAD		66		dB
Effective Number of Bits Gain = 1x (Fully Differential/Unipolar) Gain = 2x (Fully Differential/Unipolar) Gain = 4x (Fully Differential/Unipolar) Gain = 1x (Single Ended) Gain = 2x (Single Ended) Gain = 4x (Single Ended) Variation across channels[10]	ENOB		10.6 — 10.3 10.6 10.4 10.2 0.1		bits
ADC Inputs					
Input Leakage Current	I_{IN}		1		nA
Temperature sensor slope	T_{SLOPE}		1.7		mV/°C
Temperature sensor voltage at 25 °C	V_{TEMP25}		0.82		V
Disturbance					
Input Injection Current [11]	I_{INJ}			+/-3	mA
Channel to Channel Crosstalk[12]	ISOXTLK		-82		dB
Memory Crosstalk[13]	MEMXTLK		-71		dB
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

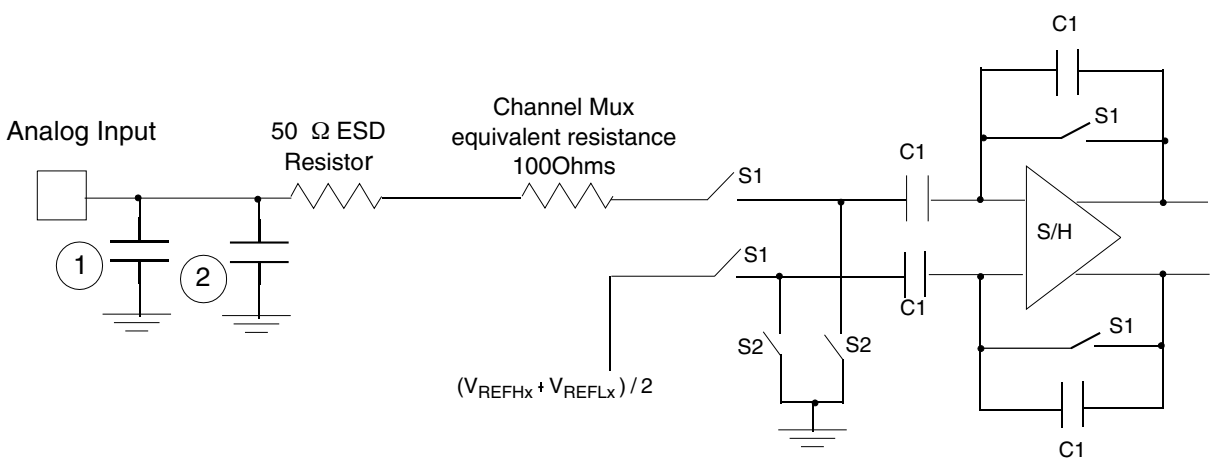
1. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed

2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA}, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

9.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 4.8 \times 10^{-12}} + 100\ ohm + 50\ ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

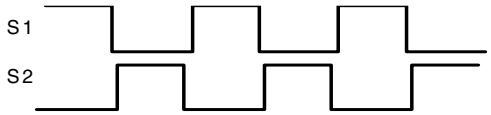


Figure 9. Equivalent circuit for A/D loading

9.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

Table 28. DAC parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pF		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 4	LSB
Differential non-linearity	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+ /- 47	mV
Gain error	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806 mV

9.5.3 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	300	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	36	—	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis				
	• CR0[HYSTCTR] = 00[1]	—	5	13	mV
	• CR0[HYSTCTR] = 01[2]	—	25	48	mV
	• CR0[HYSTCTR] = 10[2]	—	55	105	mV
	• CR0[HYSTCTR] = 11[2]	—	80	148	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)[3]	—	25	50	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)[3]	—	60	200	ns
	Analog comparator initialization delay[4]	—	40	—	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
	6-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	V_{DDA}	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Measured with input voltage range limited to 0 to V_{DD}
2. Measured with input voltage range limited to $0.7 \le Vin \le V_{DD}-0.8$
3. Input voltage range: $0.1V_{DD} \le Vin \le 0.9V_{DD}$, step = ±100mV, across all temperature. Does not include PCB and PAD delay.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

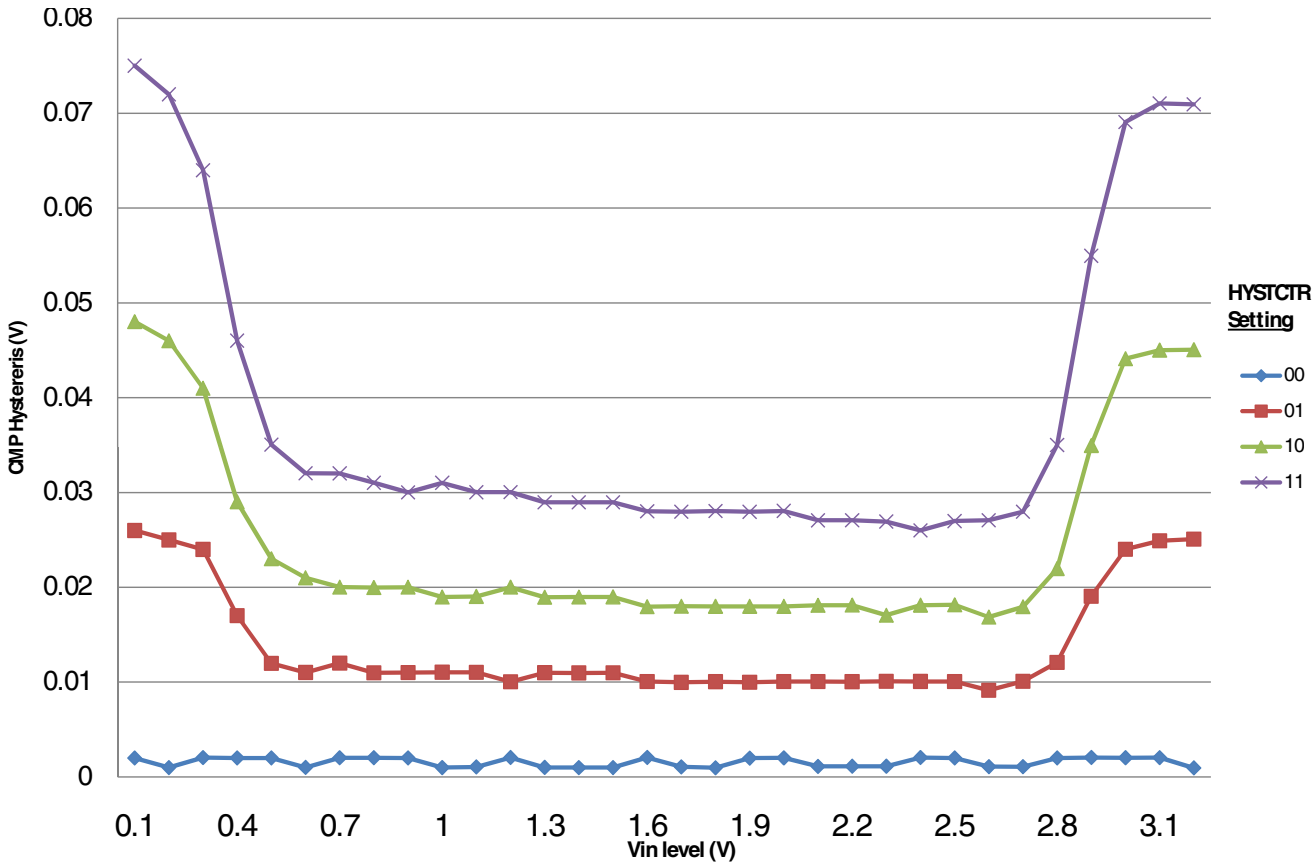


Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

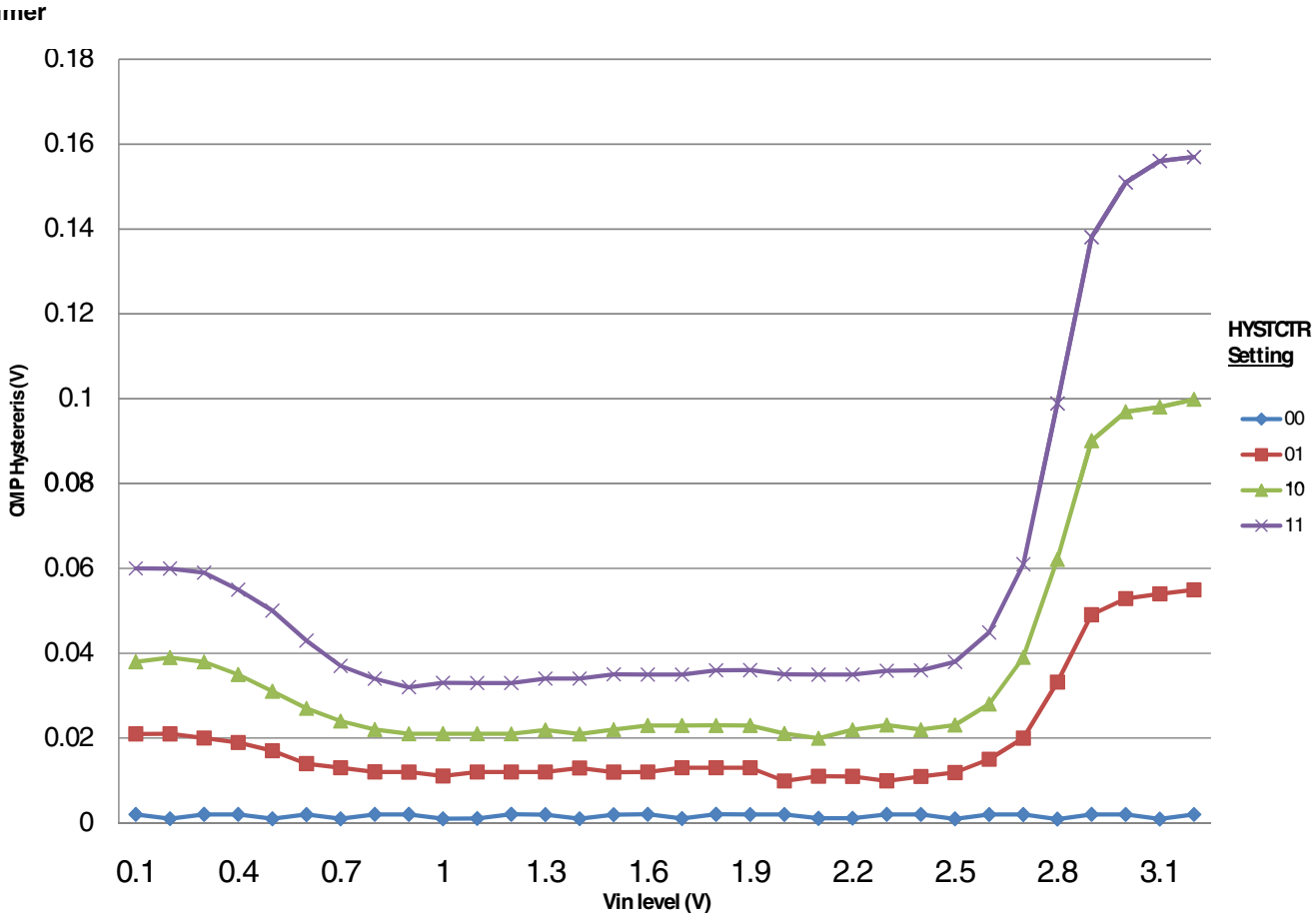


Figure 11. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

9.6 Timer

9.6.1 Quad Timer timing

Parameters listed are guaranteed by design.

Table 30. Timer timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 10	—	ns	Figure 12
Timer input high/low period	P_{INHL}	1T + 5	—	ns	Figure 12
Timer output period	P_{OUT}	2T-2	—	ns	Figure 12
Timer output high/low period	P_{OUTHL}	1T-2	—	ns	Figure 12

1. T = clock cycle. For 50 MHz operation, T = 20 ns.

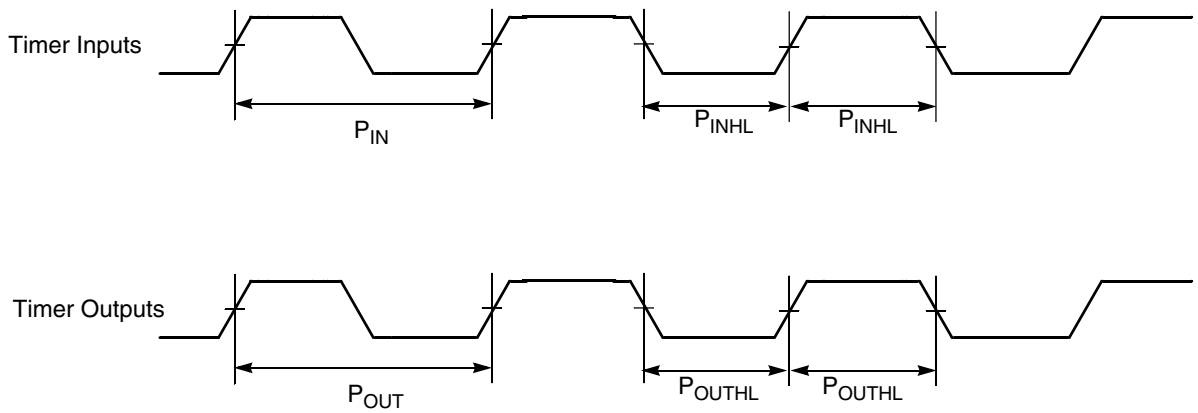


Figure 12. Timer timing

9.7 Communication interfaces

9.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 31. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	60 60	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Enable lead time Master Slave	t_{ELD}	— 20	— —	ns ns	Figure 16
Enable lag time Master Slave	t_{ELG}	— 20	— —	ns ns	Figure 16
Clock (SCK) high time Master Slave	t_{CH}		— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Clock (SCK) low time Master Slave	t_{CL}	28 28	— —	ns ns	Figure 16

Table continues on the next page...

Table 31. SPI timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Data set-up time required for inputs	t_{DS}	20	—	ns	Figure 13
Master		1	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Data hold time required for inputs	t_{DH}	1	—	ns	Figure 13
Master		3	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Access time (time to data active from high-impedance state)	t_A	5	—	ns	Figure 16
Slave					
Disable time (hold time to high-impedance state)	t_D	5	—	ns	Figure 16
Slave					
Data valid for outputs	t_{DV}	—		ns	Figure 13
Master		—		ns	Figure 14
Slave (after enable edge)					Figure 15
					Figure 16
Data invalid	t_{DI}	0	—	ns	Figure 13
Master		0	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Rise time	t_R	—	1	ns	Figure 13
Master		—	1	ns	Figure 14
Slave					Figure 15
					Figure 16
Fall time	t_F	—	1	ns	Figure 13
Master		—	1	ns	Figure 14
Slave					Figure 15
					Figure 16

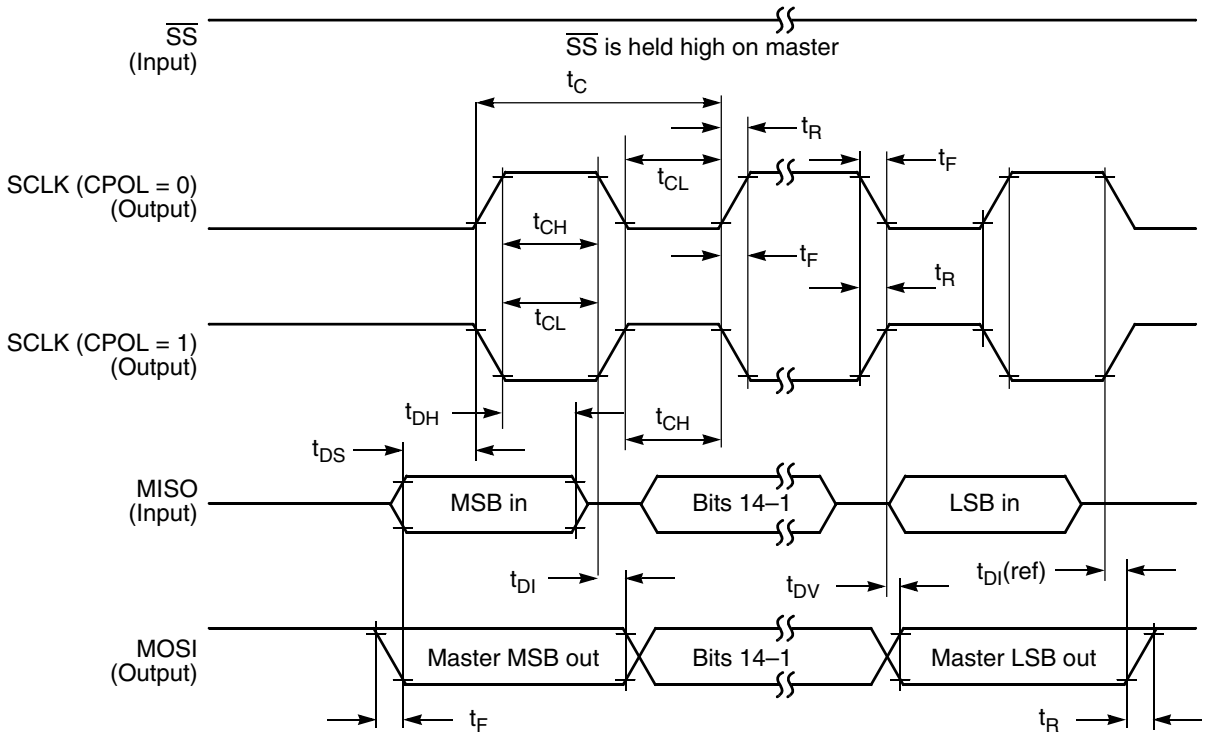


Figure 13. SPI master timing (CPHA = 0)

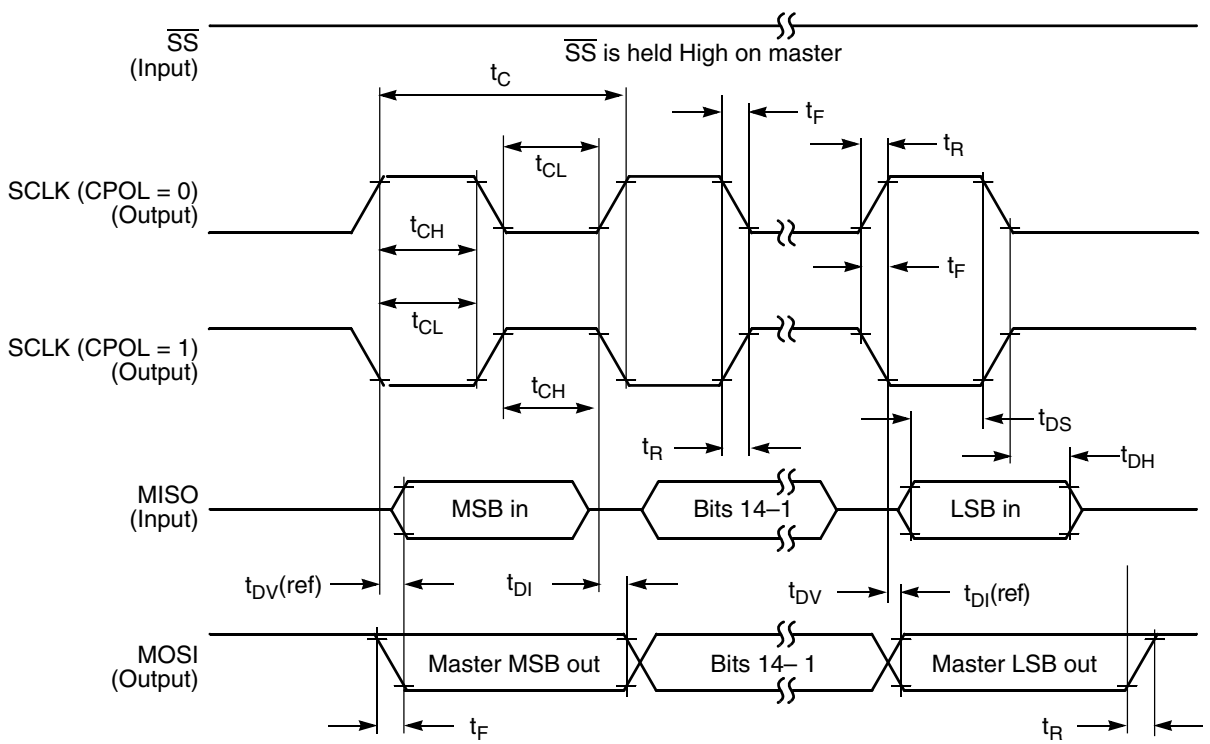


Figure 14. SPI master timing (CPHA = 1)

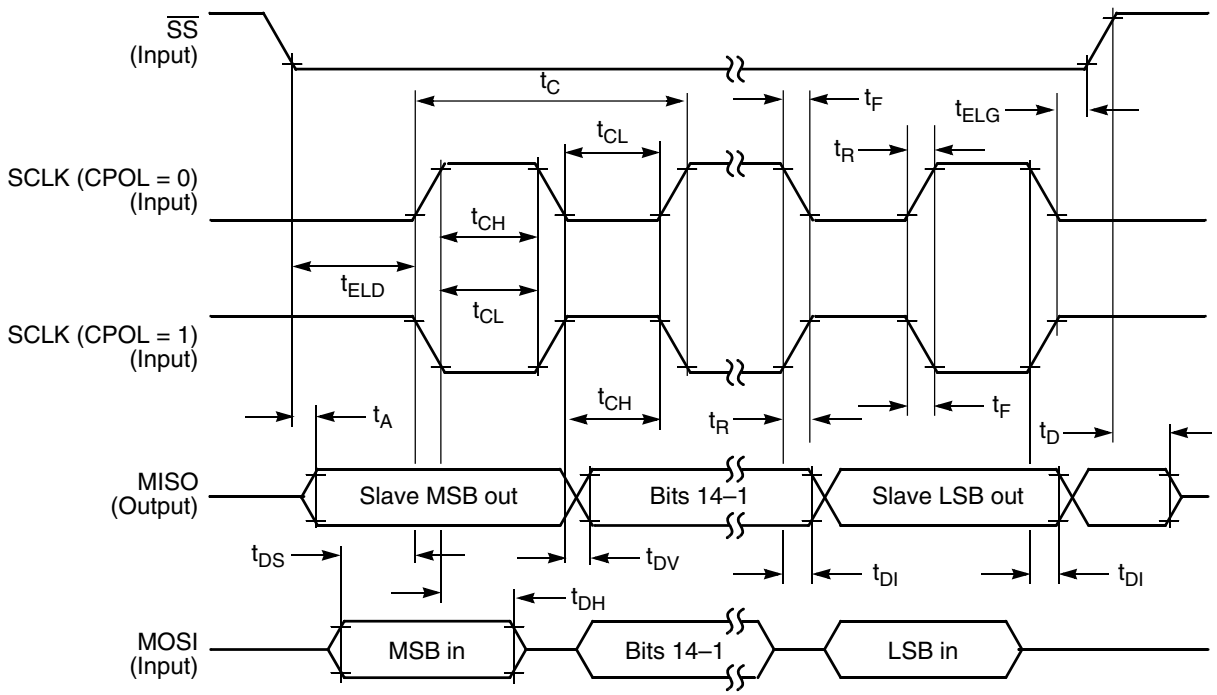


Figure 15. SPI slave timing (CPHA = 0)

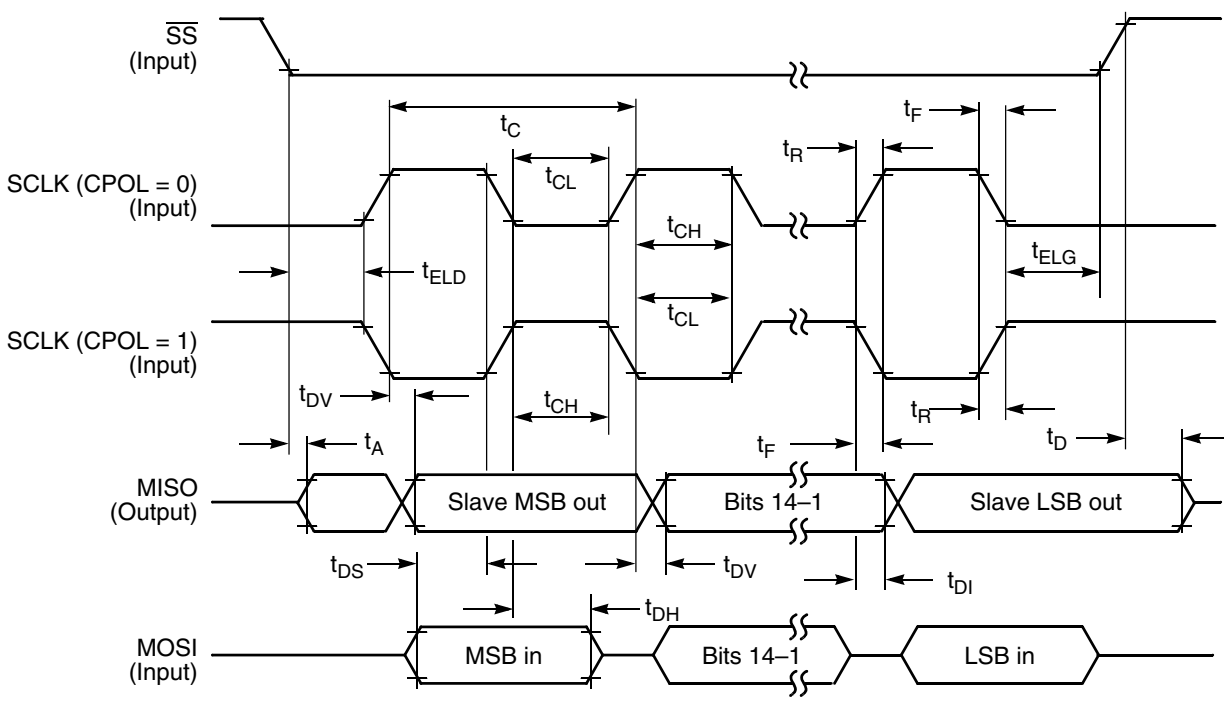


Figure 16. SPI slave timing (CPHA = 1)

9.7.2 Queued Serial Communication Interface (SCI) timing

Parameters listed are guaranteed by design.

Table 32. SCI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbit/s	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 17
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 18
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max.)50 MHz.

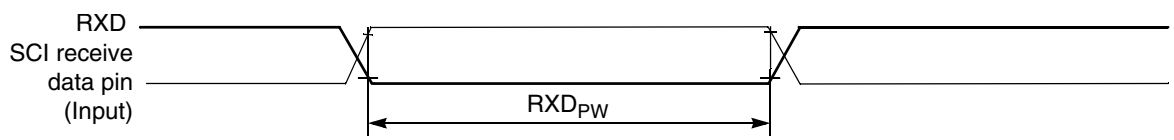


Figure 17. RXD pulse width

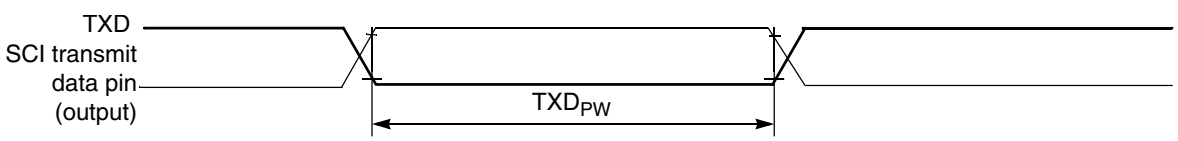


Figure 18. TXD pulse width

9.7.3 Modular/Scalable Controller Area Network (MSCAN)

Table 33. MSCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbit/s
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	1.5	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

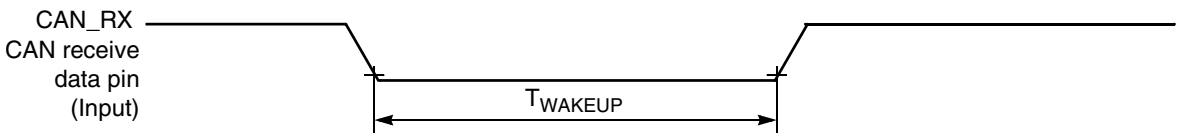


Figure 19. Bus Wake-up Detection

NOTE

CAN wakeup is not supported when ROSC_8M is in standby mode.

9.7.4 Inter-Integrated Circuit Interface (I^2C) timing

Table 34. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\,DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\,DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

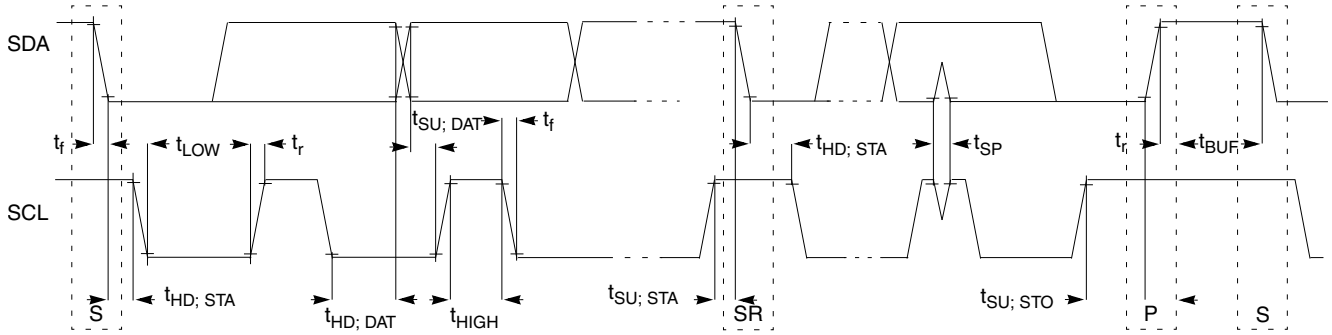


Figure 20. Timing definition for fast and standard mode devices on the I²C bus

10 Design Considerations

10.1 Thermal design considerations

An estimate of the chip junction temperature (TJ) can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which TJ value is closer to the application depends on the power dissipated by other components on the board.

- The TJ value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The TJ value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

10.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA}. Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.

- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

11 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
64-pin LQFP	98ASS23234W

12 Pinout

12.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

The RESETB pin is a 3.3 V pin only.

NOTE

If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	TCK	TCK	GPIOD2			
2	RESETB	RESETB	GPIOD4			
3	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	GPIOC1	GPIOC1	XTAL			

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
5	GPIOC2	GPIOC2	TXD0	XB_OUT11	XB_IN2	CLKO0
6	GPIOF8	GPIOF8	RXD0	XB_OUT10		PWM_2X
7	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
8	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN6	EWM_OUT_B
9	GPIOA7	GPIOA7	ANA7			
10	GPIOA6	GPIOA6	ANA6			
11	GPIOA5	GPIOA5	ANA5			
12	GPIOA4	GPIOA4	ANA4			
13	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
14	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
15	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
16	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
17	GPIOB7	GPIOB7	ANB7&CMPB_IN2			
18	GPIOC5	GPIOC5	DACA_O	XB_IN7		
19	GPIOB6	GPIOB6	ANB6&CMPB_IN1			
20	GPIOB5	GPIOB5	ANB5&CMPC_IN2			
21	GPIOB4	GPIOB4	ANB4&CMPC_IN1			
22	VDDA	VDDA				
23	VSSA	VSSA				
24	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
25	GPIOB1	GPIOB1	ANB1&CMPB_IN0	DACB_O		
26	VCAP	VCAP				
27	GPIOB2	GPIOB2	ANB2&VERFHB&CMPC_IN3			
28	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
29	VDD	VDD				
30	VSS	VSS				
31	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	SS0_B
32	GPIOC7	GPIOC7	SS0_B	TXD0	XB_IN8	
33	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	XB_OUT6
34	GPIOC9	GPIOC9	SCLK0	XB_IN4	TXD0	XB_OUT8
35	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	XB_OUT9
36	GPIOF0	GPIOF0	XB_IN6			
37	GPIOC11	GPIOC11		SCL0	TXD1	
38	GPIOC12	GPIOC12		SDA0	RXD1	
39	GPIOF2	GPIOF2	SCL0	XB_OUT6		
40	GPIOF3	GPIOF3	SDA0	XB_OUT7		
41	GPIOF4	GPIOF4	TXD1	XB_OUT8	PWM_0X	PWM_FAULT6
42	GPIOF5	GPIOF5	RXD1	XB_OUT9	PWM_1X	PWM_FAULT7
43	VSS	VSS				
44	VDD	VDD				
45	GPIOE0	GPIOE0	PWM_0B			

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
46	GPIOE1	GPIOE1	PWM_0A			
47	GPIOE2	GPIOE2	PWM_1B			
48	GPIOE3	GPIOE3	PWM_1A			
49	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
50	GPIOF1	GPIOF1	CLKO1	XB_IN7		
51	GPIOE4	GPIOE4	PWM_2B	XB_IN2		
52	GPIOE5	GPIOE5	PWM_2A	XB_IN3		
53	GPIOE6	GPIOE6	PWM_3B	XB_IN4		
54	GPIOE7	GPIOE7	PWM_3A	XB_IN5		
55	GPIOC14	GPIOC14	SDA0	XB_OUT4	PWM_FAULT4	
56	GPIOC15	GPIOC15	SCL0	XB_OUT5	PWM_FAULT5	
57	VCAP	VCAP				
58	GPIOF6	GPIOF6		PWM_3X		XB_IN2
59	GPIOF7	GPIOF7		CMPC_O		XB_IN3
60	VDD	VDD				
61	VSS	VSS				
62	TDO	TDO	GPIOD1			
63	TMS	TMS	GPIOD3			
64	TDI	TDI	GPIOD0			

12.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

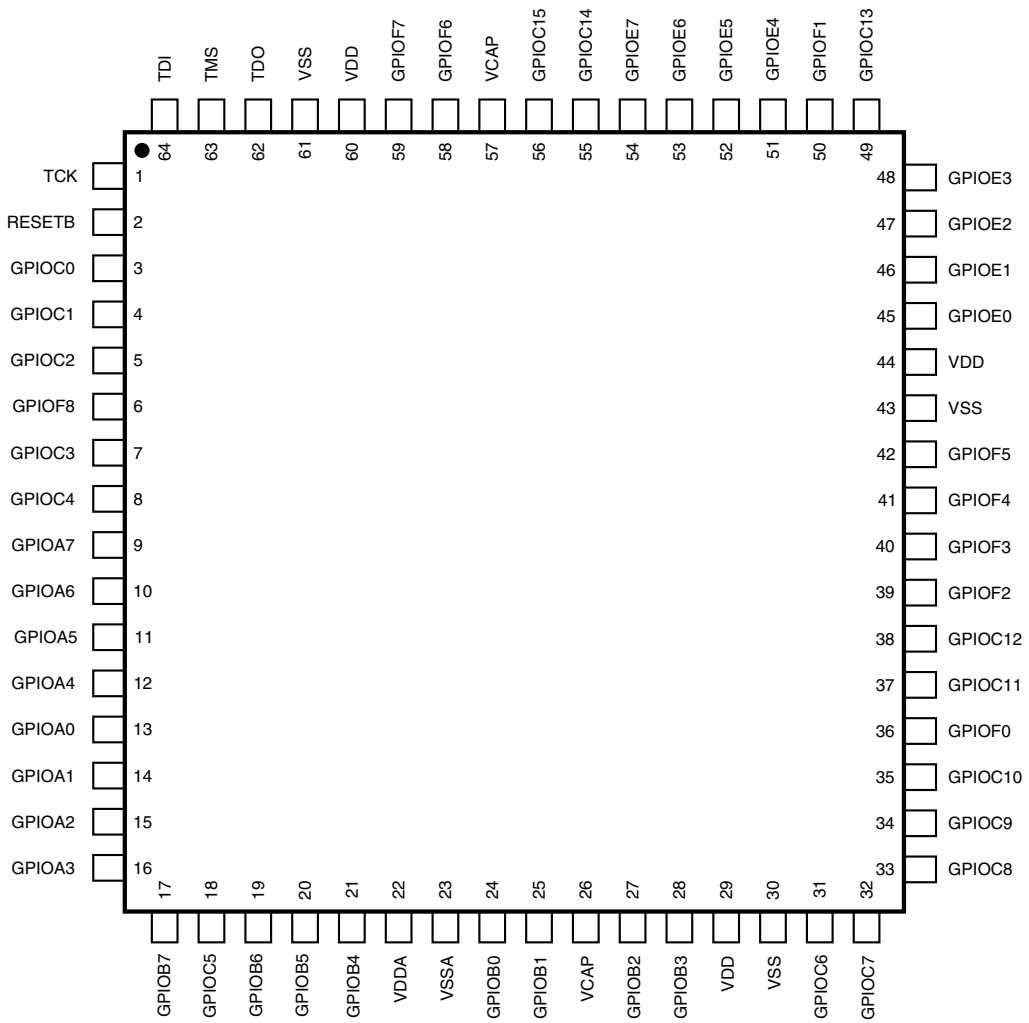


Figure 21. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

13 Product documentation

The documents listed in Table 35 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at **freescale.com**.

Table 35. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
Reference Manual	Detailed functional description and programming model	MC56F827XXRM

Table continues on the next page...

Table 35. Device documentation (continued)

Topic	Description	Document Number
MC56F82348MLH Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F82348
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata

14 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 36. Revision History

Rev. No.	Date	Substantial Changes
1	10/2013	First public release

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number MC56F82348
Revision 1, 10/2013