MCP2140A

IrDA® Standard Protocol Stack Controller With Fixed 9600 Baud Communication Rate

Features

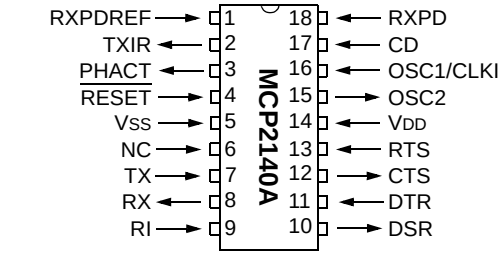
- Implements the IrDA® standard, including:
  - IrLAP
  - IrLMP
  - IAS
  - TinyTP
  - IrCOMM (9-wire “cooked” service class)
- Provides IrDA standard physical signal layer support including:
  - Bidirectional communication
  - CRC implementation
  - Fixed Data communication rate of 9600 baud
- Includes UART-to-IrDA standard encoder/decoder functionality:
  - Easily interfaces with industry standard UARTs and infrared transceivers
- Easily communicates with 16-bit PIC Microcontroller IrDA Standard Stack Library
- UART interface for connecting to Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) systems
- Transmit/Receive formats (bit width) supported:
  - 1.63 µs (Transmit & Receive)
  - 3/16 bit time (Receive Only)
- Hardware UART Support:
  - 9.6 kbaud baud rate
  - 60 Byte Data Buffer Size (64 Byte Packet)
- Infrared Supported:
  - 9.6 kbaud baud rate
  - 64 Byte Packet Size (60 Data Bytes)
- Operates as Secondary Device
- Wide Operating Voltage: 2.0V to 5.5V
- Automatic Low Power mode:
  - < 23 µA (maximum) @ 2.0V, when no IR activity present (PHACT = L)
- Footprint Compatibility with MCP2140

CMOS Technology

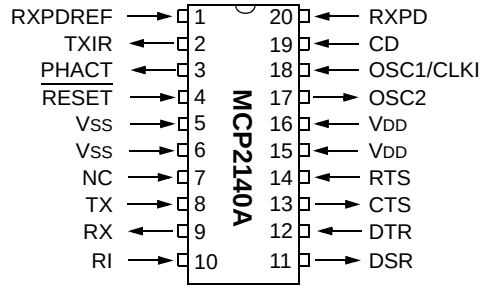
- Low power, high-speed CMOS technology
- Low voltage operation
- Industrial temperature range
- Low power consumption:
  - < 407 µA (maximum) @ 2.0V, 3.6864 MHz

Package Types

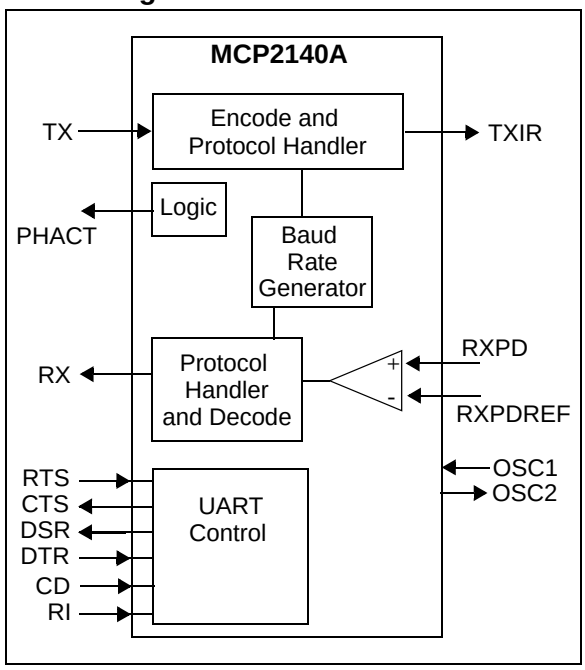
PDIP, SOIC



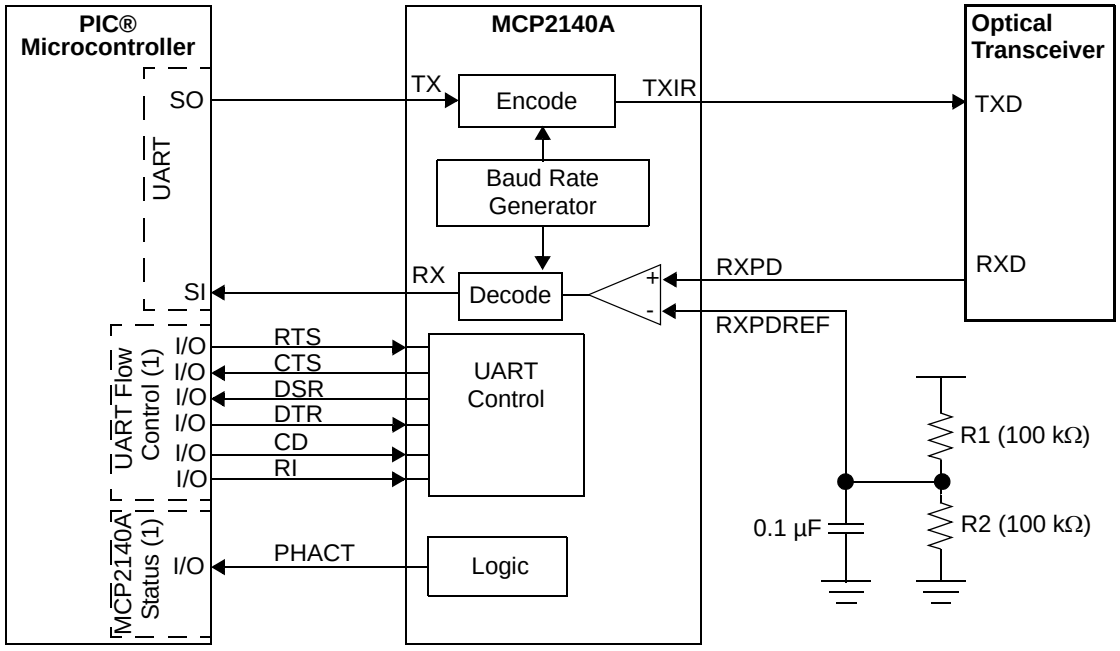
SSOP



Block Diagram



MCP2140A System Block Diagram



Note 1: Not all microcontroller I/O pins are required to be connected to the MCP2140A.

1.0 DEVICE OVERVIEW

The MCP2140A is a cost-effective, low pin count (18-pin), easy-to-use device for implementing IrDA standard wireless connectivity. The MCP2140A provides support for the IrDA standard protocol “stack”, bit encoding/decoding and low cost, discrete IR receiver circuitry. The MCP2140A is footprint compatible with the MCP2140. For migration assistance, please refer to **Section 2.14 “Migrating from the MCP2140 to the MCP2140A”**.

The serial and IR interface baud rates are fixed at 9600 baud. The serial interface and IR interface baud rates are dependent on the device frequency, but IrDA standard operation requires a device frequency of 3.6864 MHz.

The MCP2140A will specify the IR baud rate to the Primary Device during the Discover phase.

The MCP2140A can operate in Data Communication Equipment (DCE) and Data Terminal Equipment (DTE) applications, and resides between a UART and an infrared optical transceiver.

The MCP2140A encodes an asynchronous serial data stream, converting each data bit to the corresponding infrared (IR) formatted pulse. IR pulses received are decoded and then handled by the protocol handler state machine. The protocol handler sends the appropriate data bytes to the Host Controller in UART-formatted serial data.

The MCP2140A supports “point-to-point” applications, that is, one Primary device and one Secondary device. The MCP2140A operates as a Secondary device and does not support “multi-point” applications.

Sending data using IR light requires some hardware and the use of specialized communication protocols. These protocol and hardware requirements are described, in detail, by the IrDA standard specifications. The encoding/decoding functionality of the MCP2140A is designed to be compatible with the physical layer component of the IrDA standard. This part of the standard is often referred to as “IrPHY”.

Some of the devices that the MCP2140A is compatible with include:

- PCs with IR ports
- PDAs
- 16-bit PIC Microcontroller IrDA Standard Stack Library

The complete IrDA standard specification is available for download from the IrDA web site at www.IrDA.org.

1.1 Applications

The MCP2140A Infrared Communications Controller, supporting the IrDA standard, provides embedded system designers the easiest way to implement IrDA standard wireless connectivity. Figure 1-1 shows a typical application block diagram, while Table 1-1 shows the pin definitions.

TABLE 1-1: OVERVIEW OF FEATURES

Features	MCP2140A
Serial Communications	UART, IR
Baud Rate Selection	Fixed
Low Power Mode	Yes - Automatic
Resets (and Delays)	$\overline{\text{RESET}}$, POR (PWRT and OST)
Packages	18-pin DIP, SOIC, 20-pin SSOP

Infrared communication is a wireless, two-way data connection using infrared light generated by low-cost transceiver signaling technology. This provides reliable communication between two devices.

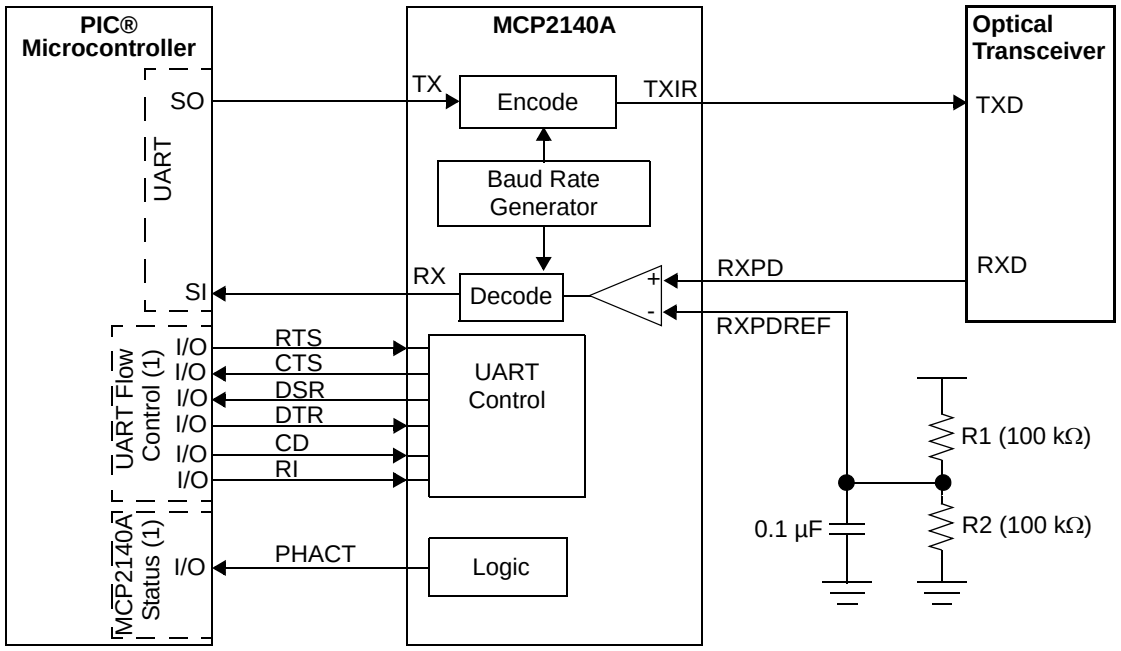
Infrared technology offers:

- Universal standard for connecting portable computing devices
- Easy, effortless implementation
- Economical alternative to other connectivity solutions
- Reliable, high-speed connections
- Safe to use in any environment (can even be used during air travel)
- No emissions testing needed (FCC, Part 15)
- Eliminates the hassle of cables
- Allows PCs and other electronic devices (such as PDAs, cell phones, etc.) to communicate with each other
- Enhances mobility by allowing users to easily connect

The MCP2140A allows the easy addition of IrDA standard wireless connectivity to any embedded application that uses serial data. Figure 1-1 shows typical implementation of the MCP2140A in an embedded system.

The IrDA protocol for printer support is not included in the IrCOMM 9-wire “cooked” service class.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



Note 1: Not all microcontroller I/O pins are required to be connected to the MCP2140A.

TABLE 1-1: MCP2140A PIN DESCRIPTION NORMAL OPERATION (DCE)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	SOIC	SSOP			
RXPDREF	1	1	1	I	A	IR Receive Photo Detect Diode reference voltage. This voltage will typically be in the range of $V_{DD}/2$.
TXIR	2	2	2	O	—	Asynchronous transmit to IrDA transceiver.
PHACT	3	3	3	OC	—	Protocol Handler Active. Indicates the state of the MCP2140A Protocol Handler. This output is an open collector, so an external pull-up resistor may be required. 1 = Protocol Handler is in the Discovery or NRM state 0 = Protocol Handler is in NDM state or the MCP2140A is in Low Power mode
$\overline{\text{RESET}}$	4	4	4	I	ST	Resets the Device
V_{SS}	5	5	5, 6	—	P	Ground reference for logic and I/O pins
NC	6	6	7	I	—	No connect
TX	7	7	8	I	TTL	Asynchronous receive; from Host Controller UART
RX	8	8	9	O	—	Asynchronous transmit; to Host Controller UART
RI	9	9	10	I	TTL	Ring Indicator. The state of this bit is communicated to the IrDA Primary Device. 1 = No Ring Indicate Present 0 = Ring Indicate Present
DSR	10	10	11	O	—	Data Set Ready. Indicates that the MCP2140A has established a valid IrDA link with a Primary Device(1). This signal is locally emulated and not related to the DTR bit of the IrDA Primary Device. 1 = An IR link has not been established (No IR Link) 0 = An IR link has been established (IR Link)
DTR	11	11	12	I	TTL	Data Terminal Ready. Indicates that the Embedded device connected to the MCP2140A is ready for IR data. The state of this bit is communicated to the IrDA Primary Device via the IrDA DSR bit carried by IrCOMM. 1 = Embedded device not ready 0 = Embedded device ready
CTS	12	12	13	O	—	Clear to Send. Indicates that the MCP2140A is ready to receive data from the Host Controller. This signal is locally emulated and not related to the CTS/RTS bit of the IrDA Primary Device. 1 = Host Controller should not send data 0 = Host Controller may send data

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels
A = Analog; P = Power
CMOS = CMOS compatible input; OC = Open collector output
I = Input; O = Output

Note 1: The state of the DSR output pin does not reflect the state of the DTR bit of the IrDA Primary Device.

TABLE 1-1: MCP2140A PIN DESCRIPTION NORMAL OPERATION (DCE) (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	SOIC	SSOP			
RTS	13	13	14	I	TTL	Request to Send. Indicates that a Host Controller is ready to receive data from the MCP2140A. This signal is locally emulated and not related to the CTS/RTS bit of the IrDA Primary device. 1 = Host Controller not ready to receive data 0 = Host Controller ready to receive data
VDD	14	14	15, 16	—	P	Positive supply for logic and I/O pins.
OSC2	15	15	17	O	—	Oscillator crystal output.
OSC1/CLKIN	16	16	18	I	CMOS	Oscillator crystal input/external clock source input.
CD	17	17	19	I	ST	Carrier Detect. The state of this bit is communicated to the IrDA Primary device via the IrDA CD bit. 1 = No Carrier Present 0 = Carrier Present
RXPD	18	18	20	I	A	IR RX Photo Detect Diode input. This input signal is required to be a pulse to indicate an IR bit. When the amplitude of the signal crosses the amplitude threshold set by the RXPDREF pin, the IR bit is detected.

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels
A = Analog; P = Power
CMOS = CMOS compatible input; OC = Open collector output
I = Input; O = Output

Note 1: The state of the DSR output pin does not reflect the state of the DTR bit of the IrDA Primary Device.

2.0 DEVICE OPERATION

The MCP2140A serial interface and IR baud rates are fixed at 9600 baud, given a 3.6864 MHz device clock.

2.1 Power-Up

Any time the device is powered up (Parameter D003), the Power-Up Timer delay (Parameter 33) occurs, followed by an Oscillator Start-up Timer (OST) delay (Parameter 32). Once these delays complete, communication with the device may be initiated. This communication is from both the infrared transceiver's side and the controller's UART interface.

2.1.1 POWER-ON AND BROWN-OUT CONDITIONS

When any state machine is operated outside of its' specified operating conditions, undesired operation may occur. Application validation should be done to determine when the system exits from either a power-on or a brown-out conditions if the MCP2140A requires the use of an external voltage supervisory circuit to ensure proper system operation.

2.2 Device Reset

The MCP2140A is forced into the reset state when the $\overline{\text{RESET}}$ pin is in the low state. Once the $\overline{\text{RESET}}$ pin is brought to a high state, the Device Reset sequence occurs. Once the sequence completes, functional operation begins.

2.3 Device Clocks

The MCP2140A requires a clock source to operate. This clock source is used to eystablish the device timing, including the device "Bit Clock".

2.3.1 CLOCK SOURCE

The clock source can be supplied by one of the following:

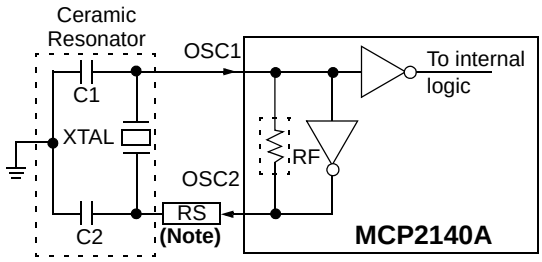
- Crystal
- Resonator
- External clock

The frequency of this clock source must be 3.6864 MHz (electrical specification Parameter 1A) for device communication at 9600 baud.

2.3.1.1 Crystal Oscillator / Ceramic Resonators

A crystal or ceramic resonator can be connected to the OSC1 and OSC2 pins to establish oscillation (refer to Figure 2-1). The MCP2140A oscillator design requires the use of a parallel-cut crystal. Use of a series cut crystals may give a frequency outside of the crystal manufacturers specifications.

FIGURE 2-1: CRYSTAL OPERATION (CERAMIC RESONATOR)



See Table 2-1 and Table 2-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Freq	OSC1 (C1)	OSC2 (C2)
3.6864 MHz	10 - 22 pF	10 - 22 pF

Note: Higher capacitance increases the stability of the oscillator, but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

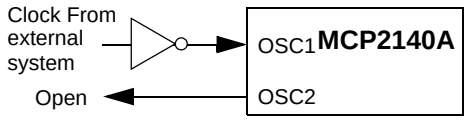
Freq	OSC1 (C1)	OSC2 (C2)
3.6864 MHz	15 - 30 pF	15 - 30 pF

Note: Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. RS may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

2.3.1.2 External Clock

For applications where a clock is already available elsewhere, users may directly drive the MCP2140A provided that this external clock source meets the AC/DC timing requirements listed in **Section 4.3 "Timing Diagrams and Specifications"**. Figure 2-2 shows how an external clock circuit should be configured.

FIGURE 2-2: EXTERNAL CLOCK



2.3.2 BIT CLOCK

The device crystal is used to derive the communication bit clock (BITCLK). There are 16 BITCLKs for each bit time. The BITCLKs are used for the generation of the start bit and the eight data bits. The stop bit uses the BITCLK when the data is transmitted (not for reception).

This clock is a fixed-frequency and has minimal variation in frequency (specified by the crystal manufacturer).

2.4 Host UART Interface

The Host UART interface communicates with the Host Controller. This interface has eight signals associated with it: TX, RX, RTS, CTS, DSR, DTR, CD and RI. Several of these signals are locally generated (not passed over the IR interface). The Host UART is a full-duplex interface, meaning that the system can transmit and receive simultaneously.

Note 1:	The MCP2140A generates several non-data signals locally.
2:	The MCP2140A emulates a 3-wire serial connection (TXD, RXD and GND). The transceiver's Transmit Data (TXD), Receive Data (RXD) signals, and the state of the CD. RI and DTR input pins are carried back and forth to the Primary device.
3:	The RTS and CTS signals are local emulations.

2.4.1 BAUD RATE

The baud rate for the MCP2140A serial port (the TX and RX pins) is fixed at 9600 baud when the device frequency is 3.6864 MHz.

2.4.2 TRANSMITTING

When the Host Controller sends serial data to the MCP2140A, the Host Controller's baud rate is required to match the baud rate of the MCP2140A's serial port.

2.4.3 RECEIVING

When the Host Controller receives serial data from the MCP2140A, the Host Controller's baud rate is required to match the baud rate of the MCP2140A's serial port.

2.4.4 HARDWARE HANDSHAKING

There are three Host UART signals used to control the handshaking operation between the Host Controller and the MCP2140A. They are:

- DSR
- RTS
- CTS

2.4.4.1 DSR

The DSR signal indicates that the MCP2140A has established a link between the MCP2140A and the Primary Device. Please refer to **Appendix B: "How Devices Connect"** for more information.

2.4.4.2 RTS

The RTS signal indicates to the MCP2140A that the Host Controller is ready to receive serial data.

Once an IR packet with "data" has been received by the MCP2140A, the RTS signal will need to be low for the received data to be transferred to the Host Controller. If the RTS signal remains high, an IR link timeout will occur and the MCP2140A will disconnect from the Primary Device.

2.4.4.3 CTS

The CTS signal indicates that the MCP2140A UART Receive Buffer is full. The MCP2140A generates the CTS signal locally.

The MCP2140A UART Receive Buffer is 60 bytes and the CTS signal will be driven high once 59 bytes have been received.

After the MCP2140A UART has received a byte, there is a latency before the CTS signal is driven high, if the UART Receive Buffer has 59 bytes. The MCP2140A then supports the reception of another byte (the 60th byte). This allows a byte was being received when CTS was driven high not to be lost. The MCP2140A UART Receive Buffer supports 60 bytes, regardless if the last byte started transmission before or after the CTS signal was driven high.

Note:	When the CTS output signal goes high, the UART FIFO will store up to 1 additional byte, for a maximum of 60 bytes.

The MCP2140A has a buffer for incoming data from the IR Host. This buffer supports the 60-byte data payload plus the memory overhead of the packet. Another 60 byte buffer is provided to buffer data from the UART serial port. The MCP2140A can handle IR data and Host UART serial port data simultaneously. A hardware handshaking pin (CTS) is provided to inhibit the Host Controller from sending serial data when the Host UART buffer is not available. Figure 2-3 shows CTS states while Figure 2-4 shows an example of the CTS signal when the Host controller streams 250 bytes to the MCP2140A. Figure 2-5 shows a flow chart for Host UART flow control using the CTS signal.

FIGURE 2-3: HOST UART CTS SIGNAL AND THE RECEIVE BUFFER

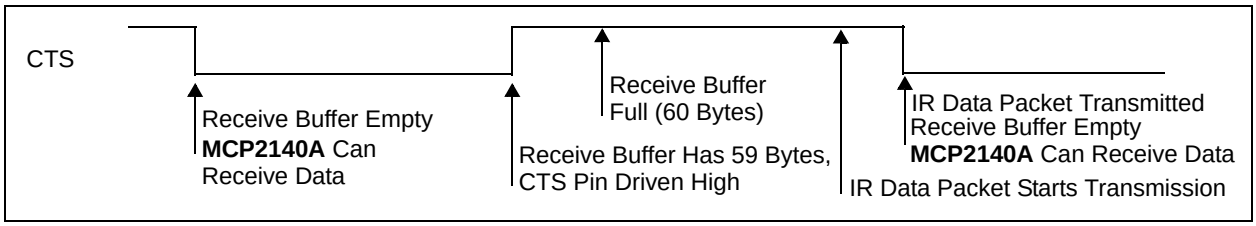


FIGURE 2-4: CTS WAVEFORM FROM HOST CONTROLLER STREAMING OF 250 BYTES TO THE MCP2140A

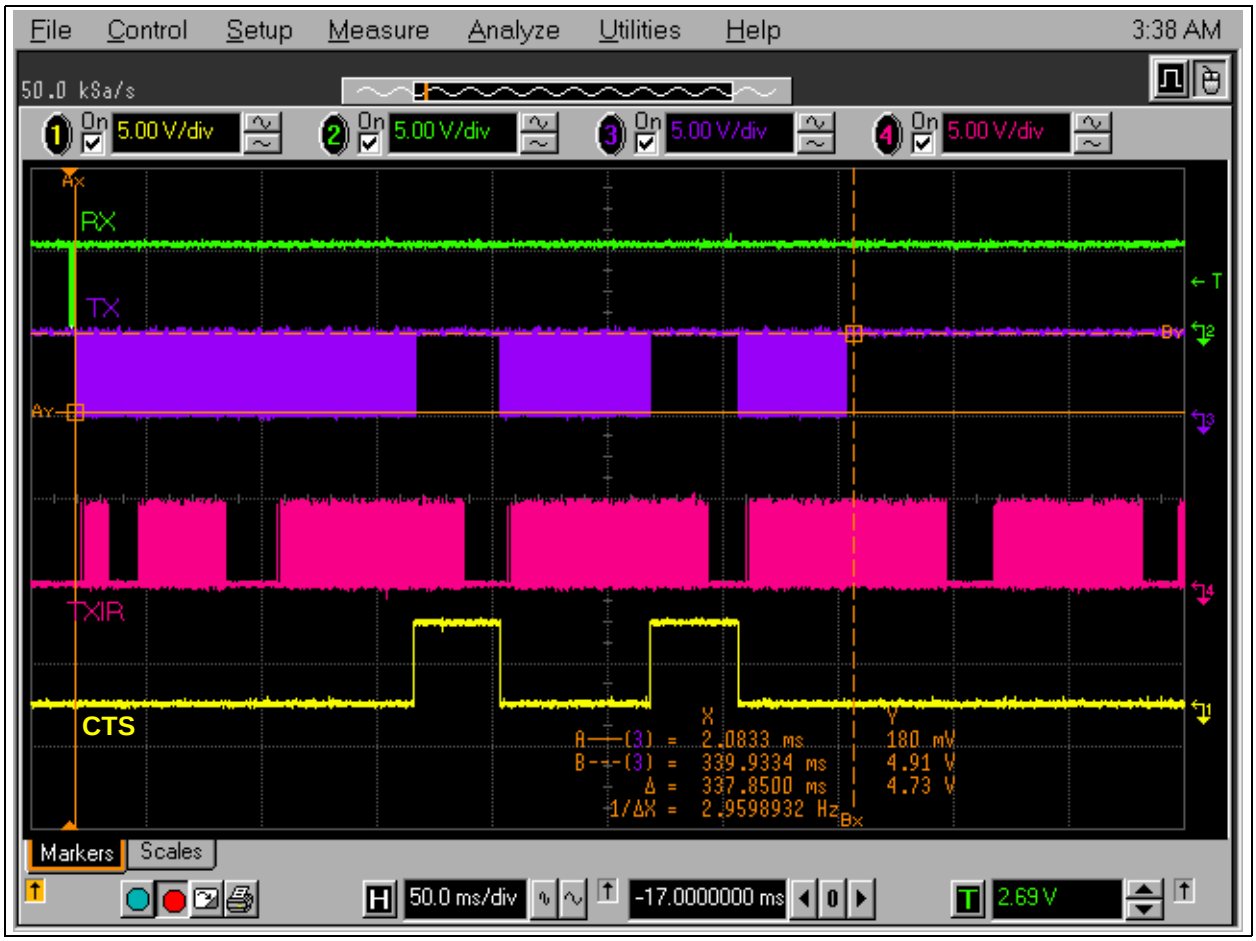
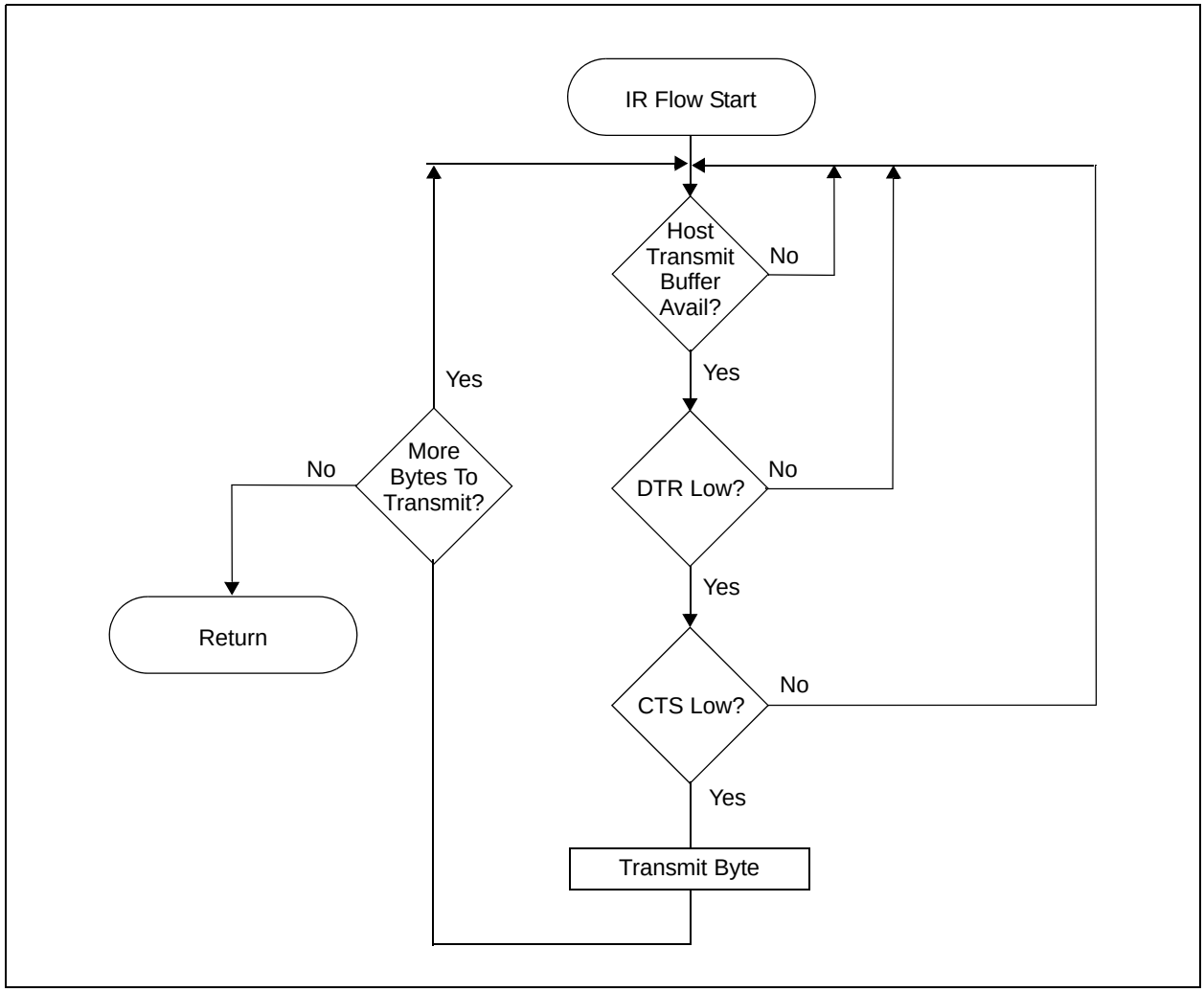


FIGURE 2-5: HOST UART CTS FLOW CONTROL FLOWCHART



2.5 Encoder/Decoder

The encoder converts the UART format data into the IrDA Standard format data and the decoder converts IrDA Standard format data into UART format data.

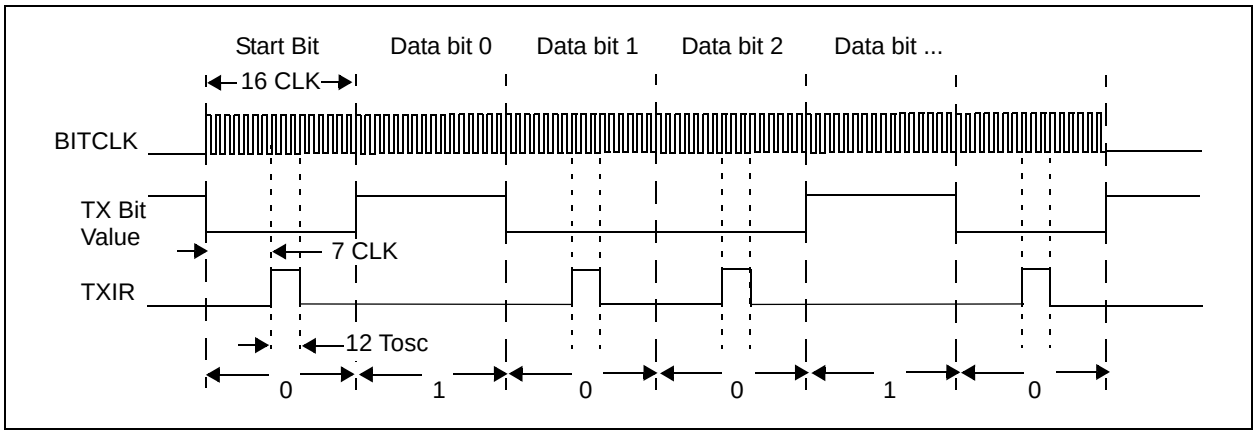
2.5.1 ENCODER (MODULATION)

The data that the MCP2140A UART received (on the TX pin) that needs to be transmitted (on the TXIR pin) is modulated. This modulated signal drives the IR transceiver module. Figure 2-6 shows the encoding of the modulated signal.

Note:	The signal on the TXIR pin does not actually line up in time with the bit value that was transmitted on the TX pin, as shown in Figure 2-6. The TX bit value is shown to represent the value to be transmitted on the TXIR pin.

Each bit time is comprised of 16-bit clocks. If the value to be transmitted (as determined by the TX pin) is a logic-low, the TXIR pin will output a low level for 7-bit clock cycles, a logic high level for 3-bit clock cycles or a minimum of 1.6 µs (see Parameter IR121). The remaining 6-bit clock cycles will be low. If the value to transmit is a logic-high, the TXIR pin will output a low level for the entire 16-bit clock cycles.

FIGURE 2-6: ENCODING



2.5.2 DECODER (DEMODULATION)

The modulated signal (data) from the IR transceiver module (on RXIR pin) is demodulated to form the received data (on RX pin). Once demodulation of the data byte occurs, the data that is received is transmitted by the MCP2140A UART (on the RX pin). Figure 2-7 shows the decoding of the modulated signal.

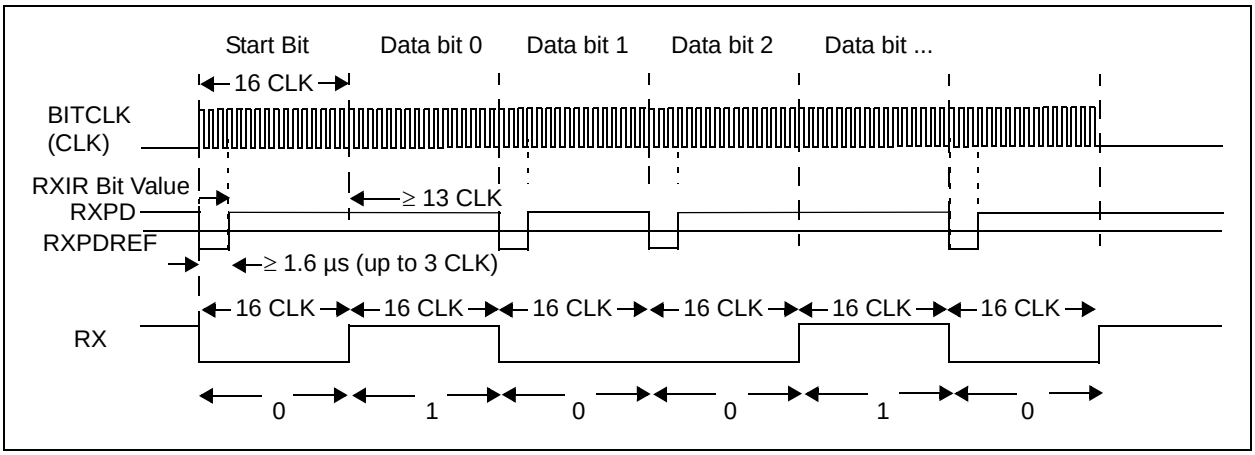
Note:	The signal on the RX pin does not actually line up in time with the bit value that was received on the RXIR pin, as shown in Figure 2-7. The RXIR bit value is shown to represent the value to be transmitted on the RX pin.

Each bit time is comprised of 16-bit clocks. If the value to be received is a logic-low, the RXIR pin will be a low level for the first 3-bit clock cycles, or a minimum of 1.6 µs. The remaining 13-bit clock cycles (or difference up to the 16-bit clock time) will be high. If the value to be received is a logic-high, the RXIR pin will be a high level for the entire 16-bit clock cycles. The level on the RX pin will be in the appropriate state for the entire 16 clock cycles.

2.6 IR Port Baud Rate

The baud rate for the MCP2140A IR port (the TXIR and RXIR pins) is fixed at the default rate of 9600 baud. The Primary device will be informed of this parameter during NDM. The Host UART baud rate and the IR port baud rate are the same.

FIGURE 2-7: DECODING



2.7 IrDA DATA PROTOCOLS SUPPORTED BY MCP2140A

The MCP2140A supports these required IrDA standard protocols:

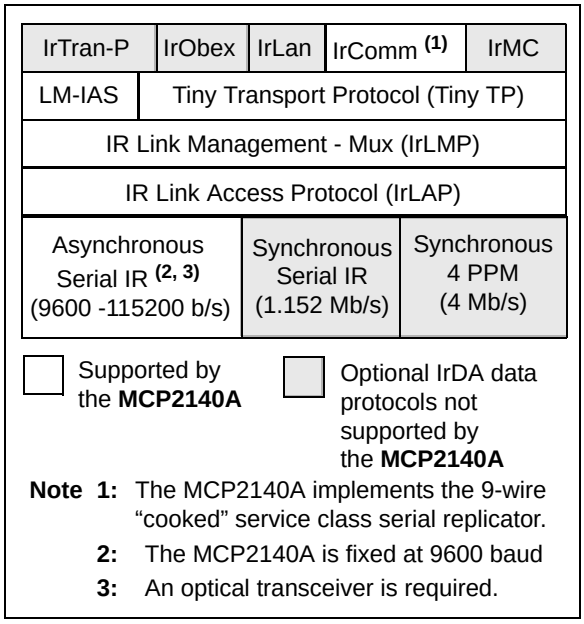
- Physical Signaling Layer (PHY)
- Link Access Protocol (IrLAP)
- Link Management Protocol/Information Access Service (IrLMP/IAS)

The MCP2140A also supports some of the optional protocols for IrDA standard data. The optional protocols implemented by the MCP2140A are:

- Tiny TP
- IrCOMM

Figure 2-8 shows the IrDA data protocol stack and those components implemented by the MCP2140A.

FIGURE 2-8: IrDA DATA - PROTOCOL STACKS



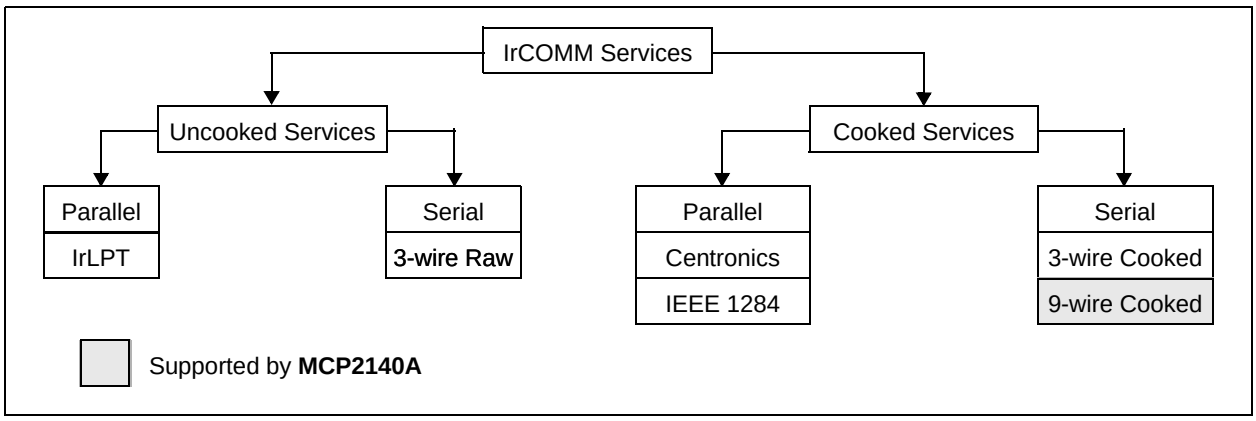
2.7.1 IRCOMM

IrCOMM provides the method to support serial and parallel port emulation. This is useful for legacy COM applications, such as printers and modem devices.

The IrCOMM standard is a syntax that allows the Primary device to consider the Secondary device a serial device. IrCOMM allows for emulation of serial or parallel (printer) connections of various capabilities. The MCP2140A supports the 9-wire "cooked" service class of IrCOMM. Other service classes supported by IrCOMM are shown in Figure 2-9.

The IrDA protocol for printer support is not included in the IrCOMM 9-wire "cooked" service class.

FIGURE 2-9: IRCOMM SERVICE CLASSES



2.8 Minimizing Power

During IR communication between a Primary Device and the MCP2140A, the MCP2140A is in an operational mode. In this mode, the MCP2140A consumes the operational current (Parameter D010A).

For many applications, the time that IR communication is occurring is a small percentage of the applications operational time. The ability for the IR controller to be in a low power mode during this time will save on the applications power consumption. The MCP2140A will automatically enter a low power mode once IR activity has stopped and will return to operational mode once IR activity is detected on the RXPD and RXPDREF pins. The PHACT pin indicates if the Protocol Handler is Active or inactive (low power mode).

Another way to minimize system power is to use an I/O pin of the Host Controller to enable power to the IR circuity

2.8.1 AUTOMATIC LOW POWER MODE

The Automatic Low Power mode allows the system to achieve the lowest possible operating current.

When the IR link has been “closed”, the protocol handler state machine returns to the Normal Disconnect Mode (NDM). During NDM, if no IR activity occurs for about 10 seconds, the device is disabled and enters into Low Power mode. In this mode, the device oscillator is shut down and the PHACT pin will be low (Parameter D010B).

Table 2-3 shows the MCP2140A current. These are specified in Parameter D010A and Parameter D010B.

TABLE 2-3: DEVICE MAXIMUM OPERATING CURRENT

Mode	Current	Comment
PHACT = H	407 µA	IR communications is occurring (or waiting for timeout).
PHACT = L	23 µA	No IR communications.

Note: Additional system current is from the Receiver/Transmitter and the RXPDREF voltage reference circuitry.

2.8.2 RETURNING TO DEVICE OPERATION

The device will exit the Low Power mode when the RXPD pin voltage crosses the REPDREF pin reference voltage.

A device reset will also cause the MCP2140A to exit Low Power mode. After device initialization, if no IR activity occurs for about 10 seconds, the device returns to the Low Power mode.

Note: For proper operation, the device oscillator must be within oscillator specification in the time frame specified in Parameter IR140.

2.9 PHACT Signal

The PHACT signal indicates that the MCP2140 Protocol Handler is active. This output pin is an open collector, so when interfacing to the Host Controller, a pull-up resistor is required.

2.10 Buffers and Throughput

The IR data rate of the MCP2140A is fixed at 9.6 kbaud. The actual throughput will be less due to several factors. Many significant factors are under the control of the developer. One factor beyond the control of the designer is the overhead associated with the IrDA standard.

Depending on the application, throughput may be an issue in one or both directions.

2.10.1 THROUGHPUT

Throughput is dependant on the direction that the data is streaming and the characteristics of the Primary Device and Secondary Device. Streaming throughput from the Secondary Device may be different with different Primary Devices. Also streaming throughput from the Secondary Device may be different than streaming throughput to the Secondary Device, with the same Primary Device. Throughput examples are shown in Table 2-4. These examples are based on actual observed data communications.

Note:	IrDA throughput is based on many factors associated with characteristics of the Primary and Secondary devices. These characteristics may cause your throughput to be more or less than is shown in Table 2-4.

Figure 2-11 shows an example communications sequence between a Primary Device and a Secondary Device (MCP2140A). In this example after the “Primary Device Sends Open Link Frame”, the time for the Secondary Devices response is fixed by the operation of the MCP2140A. After the “Primary Device Decodes Secondary Device Response” the “Primary Device Responds to Secondary Device”. Throughput may be improved if the application program can be written so that the Primary Device response as fast as possible. Also when the “Secondary Device Sends Data”, the frame should have the maximum number of data bytes.

Figure 2-12 shows the screen-capture of a Host Controller (and MCP2140A) streaming (transmitting) 250 bytes to a Primary Device (PIC24 + IrDA Standard Stack Library).

Figure 2-13 shows the screen-capture of a MCP2140A (and Host Controller) receiving 250 streamed bytes from a Primary Device (PIC24 + IrDA Standard Stack Library).

Figure 2-14 shows a second screen-capture of a Host Controller (and MCP2140A) streaming (transmitting) 250 bytes to a Primary Device (Notebook PC with IR port).

TABLE 2-4: THROUGHPUT EXAMPLES - 250 BYTES (3)

Primary Device	Secondary Device	Data Streaming Direction	250 Byte Transmit Time (ms) (1)	Effective Baud Rate (2)	Comment
PC (6)	MCP2140A (5)	S -> P	354	7062	Figure 2-14
	MCP2140	S -> P	650 (7)	3692	Note 7
PIC IrDA Standard Stack (4)	MCP2140A (5)	S -> P	337	7418	Figure 2-12
PIC IrDA Standard Stack (4)	MCP2140A (5)	P -> S	549	4553	Figure 2-13
PDA (HP iPAQ hx2495b)	MCP2140A (5)	S -> P	332	7530	Figure 2-15

Note 1: Measured from Figure. (see comment)
2: Interpolated from Figure. (see comment)
3: 10 bits transferred for each byte.
4: Using the PIC24 Explorer 16 Development Board with IR Transceiver Board
5: Using the MCP215X/40 Data Logger Demo Board and Board Firmware V1.4
6: IBM 600X Thinkpad (notebook computer) running Windows XP Professional (SP1)
7: MCP2140 Data Sheet, DS21790, Table 2-4, MCP2140 transmitted 240 bytes in this transmit time.

FIGURE 2-10: HOST UART RECEIVE BUFFER AND CTS WAVEFORM

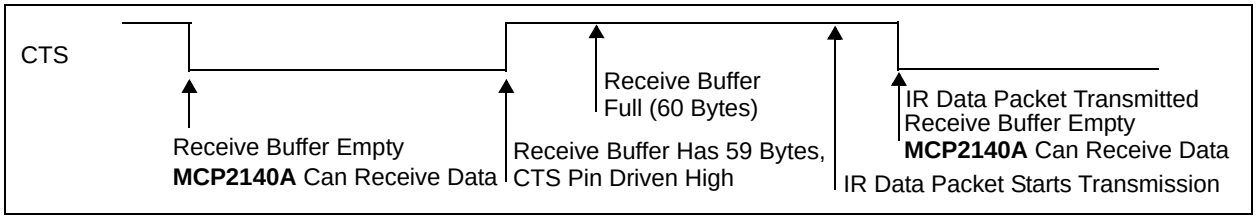


FIGURE 2-11: EXAMPLE IR COMMUNICATION SEQUENCE

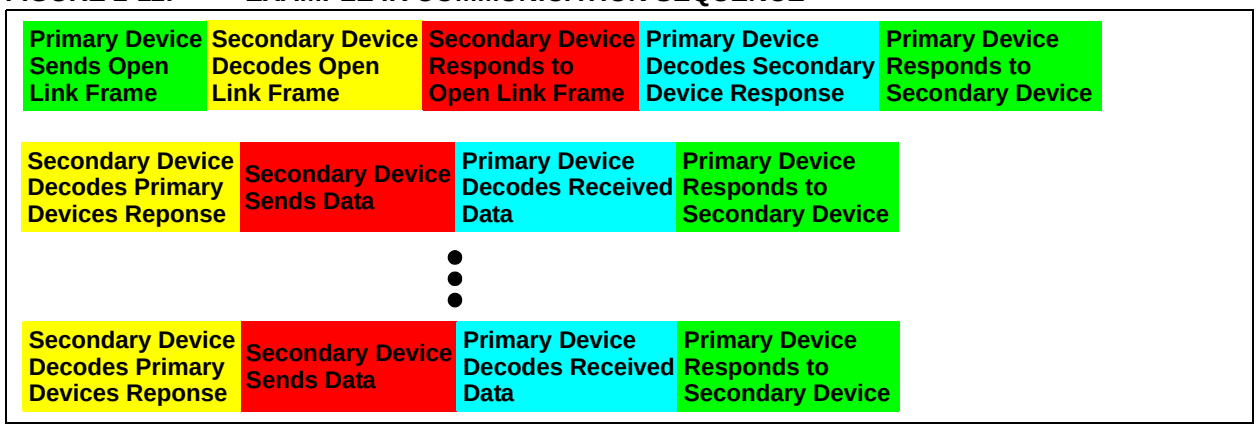
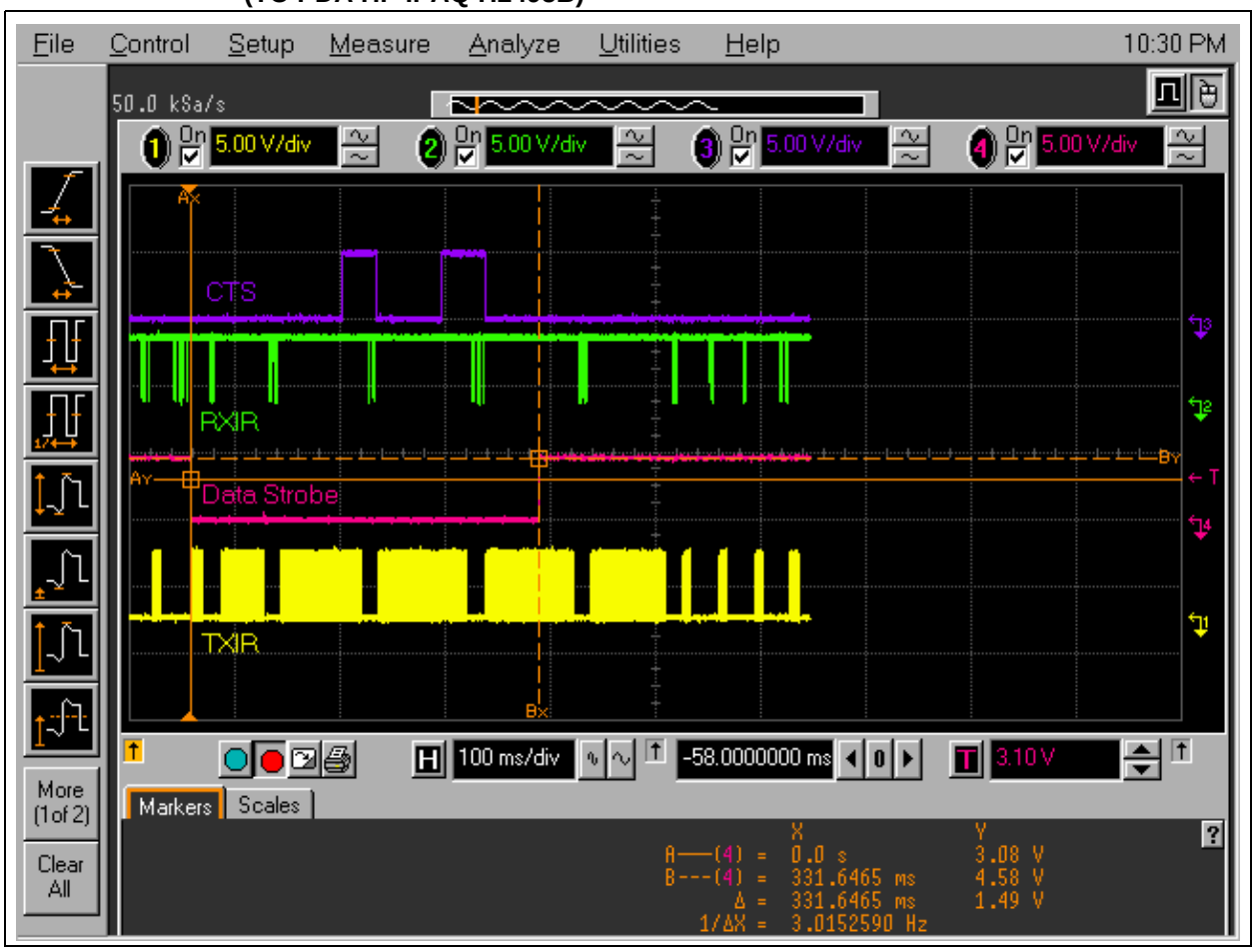


FIGURE 2-12: HOST CONTROLLER TRANSMISSION (S → P) OF A 250 BYTE PACKET (TO PIC IrDA STANDARD STACK)

FIGURE 2-13: HOST CONTROLLER RECEPTION (P → S) OF A 250 BYTE PACKET (FROM PIC IRDA STANDARD STACK)

FIGURE 2-14: HOST CONTROLLER TRANSMISSION (S → P) OF A 250 BYTE PACKET (TO PC WITH IRDA PORT)

FIGURE 2-15: HOST CONTROLLER TRANSMISSION (S → P) OF A 250 BYTE PACKET (TO PDA HP IPAQ H2495B)



2.10.2 IMPROVING THROUGHPUT

Actual maximum throughput is dependent on several factors, including:

- Characteristics of the Primary device
- Characteristics of the MCP2140A
- IrDA standard protocol overhead
- Direction of Data Transmitted

2.10.2.1 Characteristics of the Primary Device and the MCP2140A

While the characteristics of the MCP2140A are fixed, the characteristics of the Primary Device may be made better, or worse, depending on the implementation of the Primary Device's application program.

IrDA Standard protocol overhead limits the maximum throughput to much less then the 9600 baud bit rate.

2.10.2.2 IrDA Standard Protocol Overhead

The IrDA standard specifies how the data is passed between the Primary device and Secondary device. In IrCOMM, an additional 8 bytes are used by the protocol for each packet transfer. In the IrCOMM 9-wire "cooked" service class, 4 bytes of the 64 byte payload are overhead bytes. That leaves a maximum of 60 bytes that can be transferred per "frame".

The most significant factor in data throughput is how well the data frames are filled. If only 1 byte is sent at a time, the throughput overhead of the IrCOMM protocol is 89% (see Table 2-1). The best way to maximize throughput is to align the amounts of data with the receive buffer (IR and Host UART) packet size of the MCP2140A.

TABLE 2-1: IRCOMM OVERHEAD %

MCP2140A	Data Packet Size (Bytes)	IrCOMM Overhead (Bytes)	IrCOMM Overhead % (1)	Comment
IR Receive	60	8	12 %	**Note 2**
	1	8	89 %	
Host UART Receive	60	8	12 %	**Note 3, Note 4**
	1	8	89 %	

Note 1: Overhead % = Overhead/(Overhead + Data).

2: The maximum number of data bytes in the IR Receive frame.

3: The maximum number of bytes of the Host UART Receive buffer.

4: The CTS signal is driven high after the 59 byte.

2.10.2.3 Direction of Data Transmitted

Due to the different characteristics of the Primary Device and the Secondary Device, the data throughput between two devices may be substantially different depending on the direction the data is being transferred. This is shown in Table 2-4.

MCP2140A to Primary Device

One of the factors to improve throughput is to ensure the Host Controller keeps the MCP2140A UART Receive Buffer full (60 bytes) to maximize the data bytes sent per IR frame. Figure 2-10 shows the CTS waveform, what the state of the buffers can be and the operation of the Host UART and IR interfaces.

A second is to minimize the turn around response time from the Primary device, if possible.

Primary Device to MCP2140A

In this case, ensure that the Host Controller can receive data as fast as possible from the MCP2140A without requiring to force the RTS high and delay the data from being received by the Host Controller.

2.10.2.4 From the Primary Device

The MCP2140A uses a fixed IR Receiver data block size of 64 bytes.

The minimum size frame the Primary device can respond with is 6 bytes.

2.10.2.5 From the MCP2140A

The MCP2140A uses a fixed Host UART Receiver data block size of 60 bytes.

2.11 Turnaround Latency

An IR link can be compared to a one-wire data connection. The IR transceiver can transmit or receive, but not both at the same time. A delay of one bit time is recommended between the time a byte is received and another byte is transmitted.

2.12 Device ID

The MCP2140A has a fixed Device ID. This Device ID is "MCP2140A XX", with the xx indicating the silicon revision of the device.

2.13 Optical Interface

The MCP2140A requires an infrared transceiver for the optical interface. This transceiver can be a single-chip solution (integrated) or be implemented with discrete devices.

The MCP2140A was designed to interface to a integrated Optical Transceiver, although it can interface to a discrete solution as long as the MCP2140A specifications are meet.

The MCP2140 required a wave shaping circuit to interface to typical integrated optical transceivers. An Example circuit is shown in the user guides of the MCP2140 Demo and evaluation boards. This circuit is shown in Figure 2-16. This circuit inverts the optical transceivers RXD signal.

The MCP2140A requires that the RXD signal is not inverted. Figure 2-17 shows how the Microchip example wave shaping circuit can be modified with simple component replacement to support the MCP2140A. Figure 2-19 shows the RXD signal characteristics before and after the modified wave shaping circuit (Figure 2-17).

Table 2-2 shows the schematic symbols for the example MCP2140 wave shaping circuit, and the component changes required to make the PCB layout compatible with the MCP2140A. The layout is not required to be changed since the BAT54 is a Schottky Diode in a SOT-23-3 package with the desired pin connections, the capacitor footprint can easily be replaced by a resistor (0Ω), and the R16 resistor can be removed since it is not involved with the circuit.

Figure 2-18 shows a simple “Blue Wire” modification that can be done.

TABLE 2-2: EXAMPLE MCP2140 WAVE SHAPING CIRCUIT TO MCP2140A COMPONENT CHANGES

Component		
Symbol	**MCP2140 Device (value)**	**MCP2140A Device (value)**
C19	Capacitor (47pF)	Resistor (0 Ω) **(1)**
R11	—	—
R13	—	—
R16	Resistor (100Ω)	—
R20	Resistor (4.7 kΩ)	Resistor (4.7 KΩ) **(1)**
Q1 (SOT-23-3)	PNP Transistor (MMUN2111LT1)	Schottky Diode (BAT54) **(1)**

Note 1: This device is changed from MCP2140 Wave Shaping Circuit implementation.

Table 2-4 shows a list of common manufacturers of integrated optical transceivers.

FIGURE 2-16: MCP2140 WAVE SHAPING CIRCUIT FOR INTEGRATED OPTICAL TRANSCEIVER

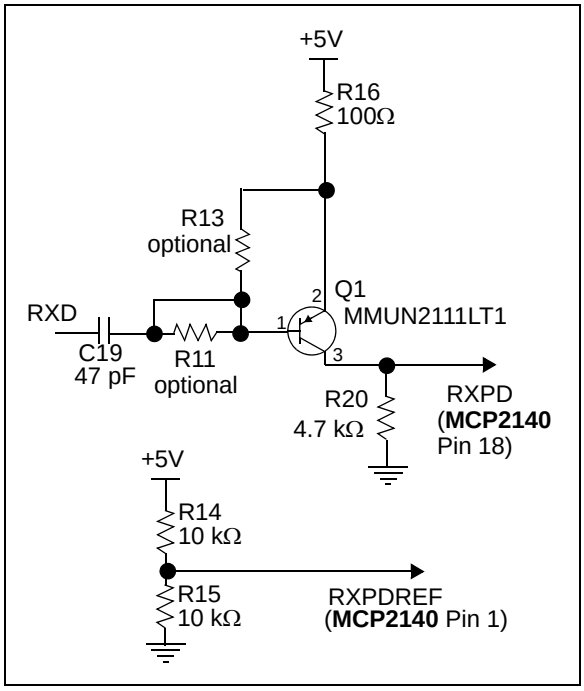


FIGURE 2-17: MCP2140A MODIFICATIONS OF MCP2140 WAVE SHAPING CIRCUIT

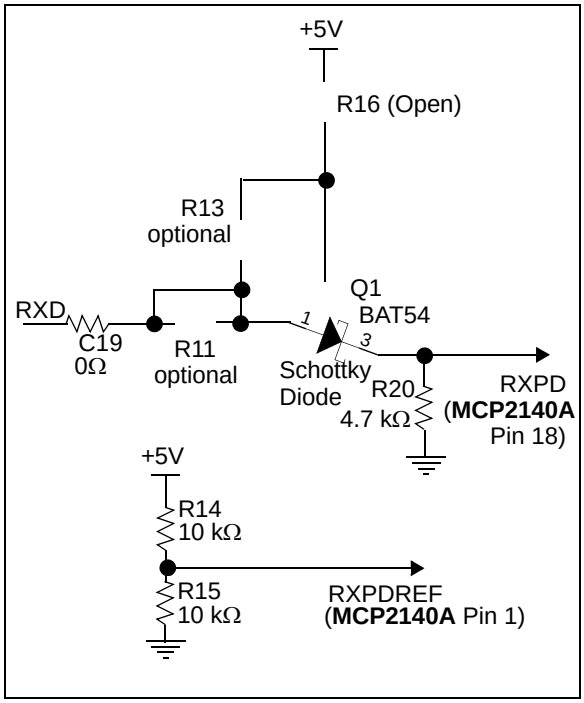


FIGURE 2-18: MCP2140A "BLUE WIRE" MODIFICATIONS OF MCP2140 WAVE SHAPING CIRCUIT

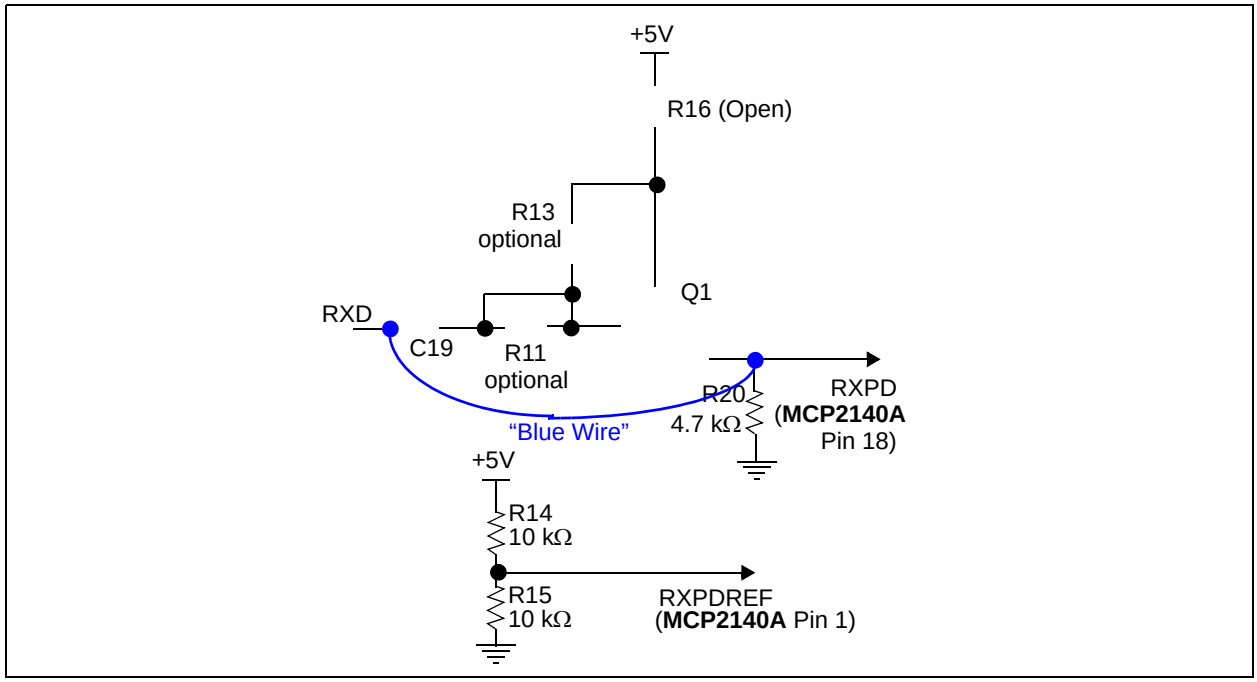
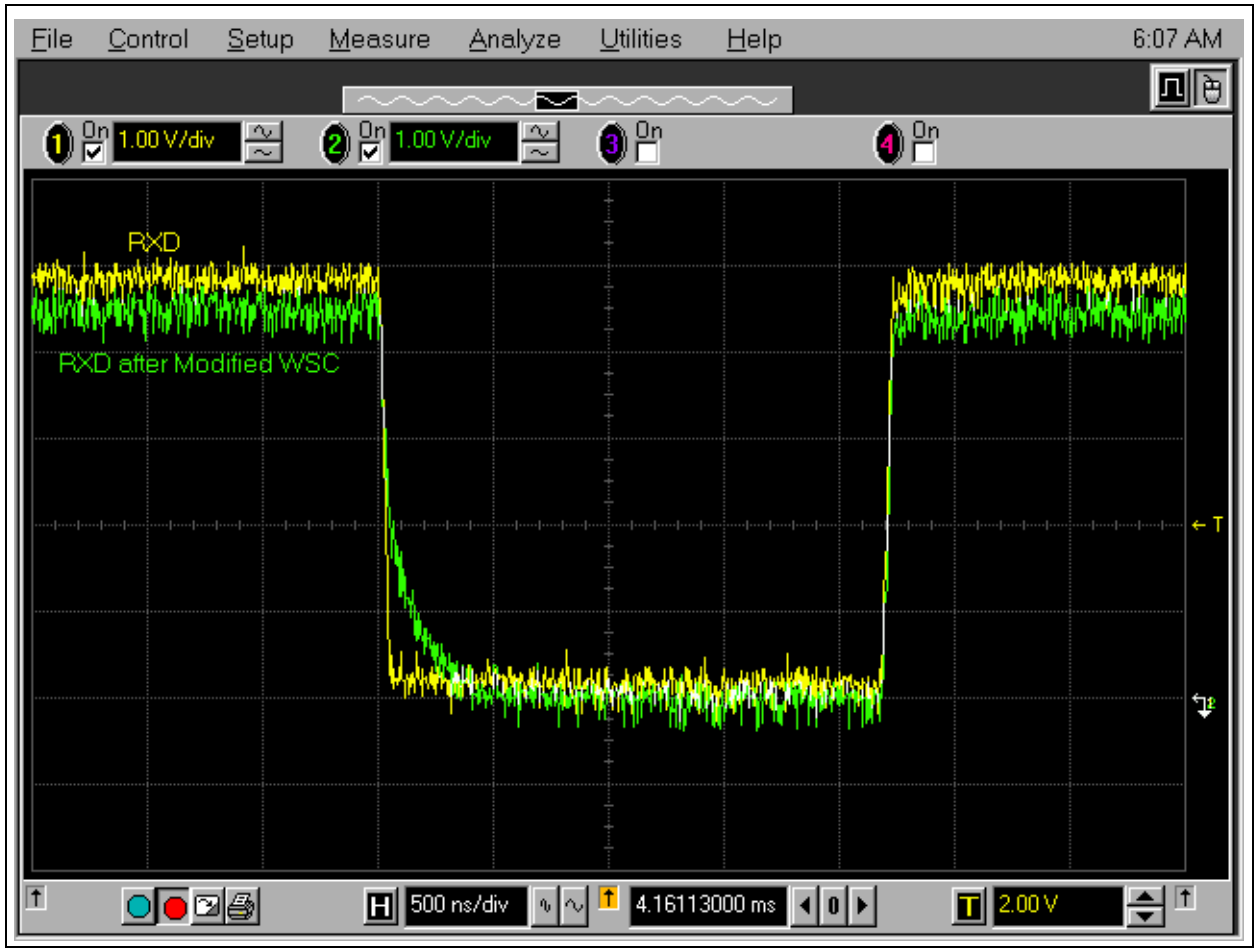


FIGURE 2-19: MCP2140A MODIFICATIONS OF MCP2140 WAVE SHAPING CIRCUIT



2.14 Migrating from the MCP2140 to the MCP2140A

This section shows you in the major differences between the MCP2140 and the MCP2140A. Your application may have other sensitivities and a complete system validation should be done.

Table 2-3 shows the differences and enhancements of the MCP2140A in comparison to the MCP2140.

TABLE 2-3: DIFFERENCE BETWEEN MCP2140 AND MCP2140A

Feature		MCP2140	MCP2140A
Voltage Range		3.0V - 5.5V	2.0V - 5.5V
Frequency of Operation (MHz)		7.3728	3.6864
UART operation		Half Duplex	Full Duplex
UART Receiver buffer Size (bytes) (max.)		29	60 (2)
UART Transmit buffer Size (bytes) (max.)		29	60
IR Receiver Frame Payload Size (bytes) (max.)		64 (3)	64 (3)
IR Transmit Frame Payload Size (bytes) (max.)		64 (3)	64 (3)
Max I_{DD} (uA) at min. V_{DD}.	PHACT = H	2200	407
	PHACT = L	60	23
Integrated Optical Transceivers RXD wave shaping circuit		Required	Not Required (1)
Optical Transceiver RXPD bit signal polarity		High to Low or Low to High	High to Low only

Note 1: The External Wave Shaping Circuit is not required. For applications replacing the MCP2140, components of the circuit can be replaced to effectively remove the waveshaping circuit. See **Section 2.13 "Optical Interface"**.

2: The MCP2140A will drive the CTS signal active after the UART Receive Buffer has 59 bytes. The Receive buffer supports the reception of a 60th byte for systems that have 0 delay between UART data bytes.

3: Includes 4 bytes overhead for 9-wire "cooked" protocol. This means that there are a maximum of 60 data bytes per frame.

2.15 The PIC IrDA Standard Stack Library and the MCP2140A

The MCP2140A is compatible with the PIC IrDA Standard Stack Library routines for 16-bit PIC microcontrollers. The application must use the Client Library routines for the IrCOMM 9-wire Cooked protocol (for Primary Device operation).

2.16 References

The IrDA Standards organization information can be found at:

http://www.irda.org

Some common manufacturers of optical transceivers are shown in Table 2-4.

TABLE 2-4: COMMON OPTICAL TRANSCEIVER MANUFACTURERS

Company	Company Web Site Address
Sharp®	www.sharpsma.com
Infineon®	www.infineon.com
Agilent®	www.agilent.com
Vishay®/Temic	www.vishay.com
Rohm	www.rohm.com

3.0 DEVELOPMENT TOOLS

The MCP2140A currently has three Demo/Development boards that can be used to demonstrate or evaluate the MCP2140A. These boards are:

- MCP215x/40 Data Logger Demo Board
- MCP215x/40 Developers Daughter Board
- MCP2140 Wireless Temperature Sensor Demo Board

These boards have not been tested with the MCP2140A, but the supplied device can easily be replaced with the MCP2140A. The waveshaping circuit of the MCP2140 will need to be modified. See **Section 2.13 "Optical Interface"** for additional information on modifing the MCP2140 wave shaping circuit.

Please check with the Microchip Technology Inc. web site (www.microchip.com) for additional boards and technical information.

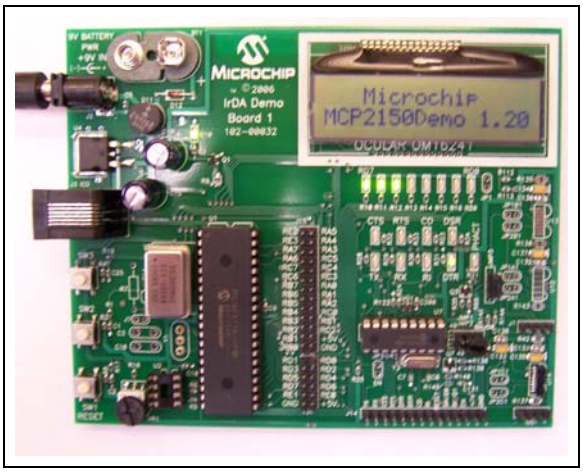
3.1 MCP215X/40 Data Logger Demo Board

Part Number: MCP215XDM

Devices Supported: MCP2150, MCP2155, MCP2140, and MCP2140A

The MCP215X IrDA Data Logger Demo Board demonstrates the MCP2150 (or MCP2155) IrDA Standard Protocol Stack Controller device in a real world application. The system designer can use this design as an example of how to integrate an IrDA standard port in their embedded system.

FIGURE 3-1: MCP215X/40 DATA LOGGER DEMO BOARD



Features:

- Demonstrates the MCP2150 IrDA Protocol Controller in a data logging application
- Communicates directly to a Laptop computer, Palm or Pocket PC PDA
- Primary Device application programs are provided to demonstrate operation (for PC, Palm OS, Pocket PC)
- F/W routines transmit data to a Primary Device (i.e., Laptop, PDA)
- LCD display indicates system state
- Reprogrammable PIC16F877 with ICSP™ (In-Circuit Serial Programming™) interface and ICD header
- Interface Header allows board to be interfaced to a prototype system application
- Header allows other Optical Transceiver circuits to be interfaced to the MCP215X device
- Operates on 9V DC input or a 9V battery

3.2 MCP215X/40 Developer's Daughter Board

Part Number: MCP215X/40EV-DB

Devices Supported: MCP2150, MCP2155, MCP2140, and MCP2140A

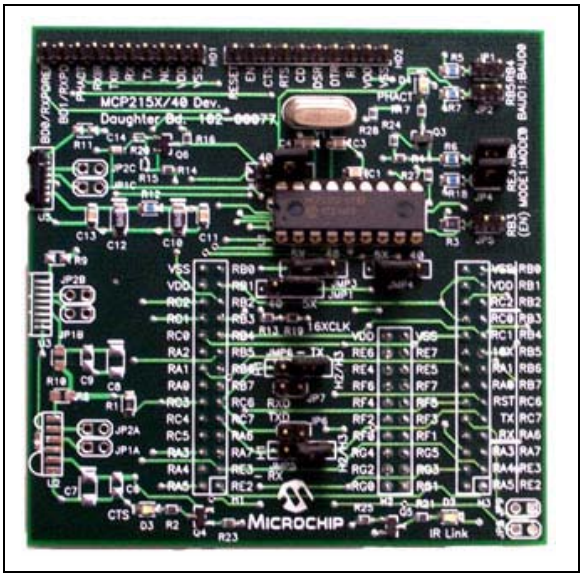
The MCP215X/40 Developer's Daughter Board is used to evaluate and demonstrate the MCP2150, MCP2155 or the MCP2140 IrDA® Standard Protocol Handler with Encoder/Decoder devices.

Headers allow the MCP215X/40 Developer's Daughter Board to be easily jumpered into systems for development purposes.

The MCP215X/40 Developer's Daughter Board is designed to interface to several of the "new" low-cost PICmicro® Demo Boards. These include the PICDEM™ HPC Explorer Demo board, the PICDEM™ FS USB Demo board, and the PICDEM™ LCD Demo board.

When the MCP215X/40 Developer's Daughter Board is used in conjunction with the PICDEM™ HPC Explorer Demo board, the MCP215X or MCP2140 can be connected to either of the PIC18F8772's two UARTs or the RX and TX signals can be "crossed" so the MCP215X or MCP2140 device can communicate directly out the PICDEM™ HPC Explorer Demo Board's UART (DB-9).

FIGURE 3-2: MCP215X/40 DEVELOPERS DAUGHTER BOARD



Features:

- 18-pin socket for installation of MCP2150, MCP2155, or MCP2140
- Three Optical Transceiver circuits (1 installed)
- MCP2140 Optical Transceiver waveshaping circuit
- Headers to interface to low cost PICDEM Demo Boards, including:
  - PICDEM™ HPC Explorer Demo Board
  - PICDEM™ LCD Demo Board
  - PICDEM™ FS USB Demo Board
  - PICDEM™ 2 Plus Demo Board
- Headers to easily connect to the user's embedded system
- Jumpers to select circuit connections between MCP2150, MCP2155, and MCP2140
- Jumpers to select routing of MCP215X/40 signals to the PICDEM™ Demo Board Headers
- Jumpers to configure the operating mode of the board

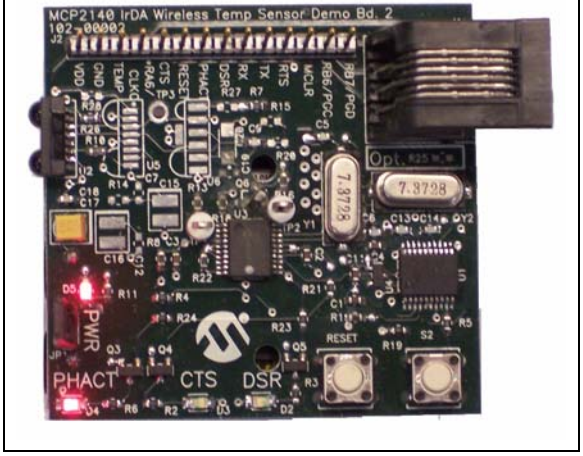
3.3 MCP2140 IrDA Wireless Temperature Sensor Demo Board

Part Number: MCP2140DM-TMPSNS

Devices Supported: MCP2140 and MCP2140A

The MCP2140 IrDA Standards Wireless Temp Sensor Demo Board demonstrates the MCP2140 device in a real world application. The system designer can use this design as an example of how to integrate an IrDA standard port in their system.

FIGURE 3-3: MCP2140 IRDA WIRELESS TEMPERATURE SENSOR DEMO BOARD



Features:

- Demonstrates the MCP2140 IrDA Protocol Controller in a data logging application
- Communicates directly to a laptop computer, Palm or Pocket PC PDA
- Primary device application programs are provided to demonstrate operation (for PC, Palm OS, Pocket PC)
- Demonstrates the MCP2140 IrDA Protocol Controller in a data logging application
- F/W routines transmit TC1047A temperature and other data to a primary device (i.e., Laptop, PDA)
- Reprogrammable PIC18F1320 with ICSP™ (In-Circuit Serial Programming™) interface and ICD header
- Operates on 3 AAA alkaline batteries

NOTES:

4.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

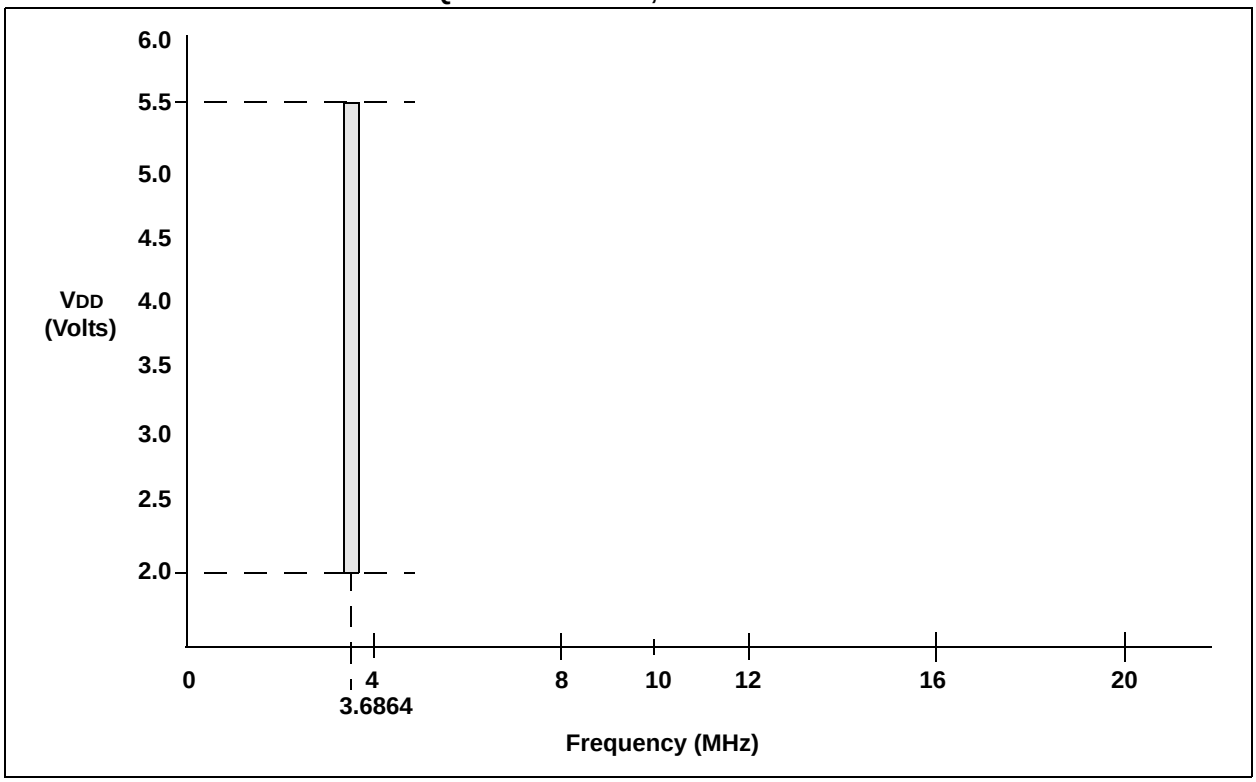
Ambient Temperature under bias ..... –40°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on $\overline{RESET}$ with respect to V_{SS} ..... -0.3V to +14V
Voltage on all other pins with respect to V_{SS} ..... –0.3V to (V_{DD} + 0.3V)
Total Power Dissipation **(1)** ..... 800 mW
Max. Current out of V_{SS} pin ..... 300 mA
Max. Current into V_{DD} pin ..... 250 mA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_0 < 0 or V_0 > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any Output pin ..... 25 mA
Max. Output Current sourced by any Output pin ..... 25 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

†**NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below V_{SS} at the RESET pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 - 100Ω should be used when applying a “low” level to the RESET pin rather than pulling this pin directly to V_{SS}. .

FIGURE 4-1: VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



4.1 DC Characteristics

DC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified) Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial)				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.0	—	5.5	V	See **Figure 4-1**
D002	VDR	RAM Data Retention Voltage (2)	2.0	—	—	V	Device Oscillator/Clock stopped
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05	—	—	V/ms	
D010A	IDD	Supply Current (3, 4)	—	—	23	µA	VDD = 2.0V, PHACT = H
D010B			—	—	38	µA	VDD = 3.0V, PHACT = H
D010C			—	—	71	µA	VDD = 5.0V, PHACT = H
D010D			—	—	350	µA	VDD = 2.0V, PHACT = L
D010E			—	—	600	µA	VDD = 3.0V, PHACT = L
D010F			—	—	995	µA	VDD = 5.0V, PHACT = L

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.

3: When the device is in IR communication (PHACT pin is high), supply current is mainly a function of the operating voltage and frequency. Pin loading, pin rate and temperature have an impact on the current consumption.The test conditions for all IDD measurements are made when device is:
OSC1 = external square wave, from rail-to-rail; all input pins pulled to VSS, RXIR = VDD, $\overline{\text{RESET}}$ = VDD;

4: When the device is in low power mode (PHACT pin is low), current is measured with all input pins tied to VDD or VSS and the output pins driving a high or low level into infinite impedance.

4.1 DC Characteristics (Continued)

DC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified) Operating temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 4.1 "DC Characteristics".				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	Input pins					
D030		TX, RI, DTR, RTS, and CD	VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D030A			VSS	—	0.15 VDD	V	otherwise
D032		$\overline{\text{RESET}}$	VSS	—	0.2 VDD	V	
D033		OSC1	VSS	—	0.6	V	
		Input High Voltage					
	VIH	Input pins		—			
D040		TX, RI, DTR, RTS, and CD	0.8 VDD	—	VDD	V	
D042		$\overline{\text{RESET}}$	0.8 VDD	—	VDD	V	
D043		OSC1	1.3	—	VDD	V	
		Input Leakage Current (Notes 1, 2)					
D060	IIL	TX, RI, DTR, RTS, and CD	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance.
D061		$\overline{\text{RESET}}$	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
		Output Low Voltage					
D080	VOL	TXIR, RX, DSR, and CTS pins	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage (Note 2)					
D090	VOH	TXIR, RX, DSR, and CTS pins	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	When external clock is used to drive OSC1.
D101	CIO	All Input or Output pins	—	—	50	pF	

Note 1: The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as coming out of the pin.

4.2 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

4.2.1 TIMING CONDITIONS

The temperature and voltages specified in Table 4-2 apply to all timing specifications, unless otherwise noted. Figure 4-2 specifies the load conditions for the timing specifications.

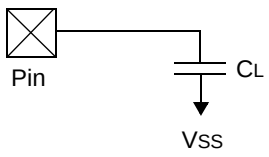
TABLE 4-1: SYMBOLOGY

1. TppS2ppS		2. TppS	
T			
F	Frequency	T	Time
E	Error		
Lowercase letters (pp) and their meanings:			
pp			
io	Input or Output pin	osc	Oscillator
rx	Receive	tx	Transmit
bitclk	RX/TX BITCLK	RST	Reset
drt	Device Reset Timer		
Uppercase letters and their meanings:			
S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (high-impedance)	V	Valid
L	Low	Z	High-impedance

TABLE 4-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS

AC Specifications	**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise stated):** Operating temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec **Section 4.1 "DC Characteristics"**.

FIGURE 4-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



CL = 50 pF for all pins except OSC2
15 pF for OSC2 when external clock is used to drive OSC1

4.3 Timing Diagrams and Specifications

FIGURE 4-3: EXTERNAL CLOCK TIMING

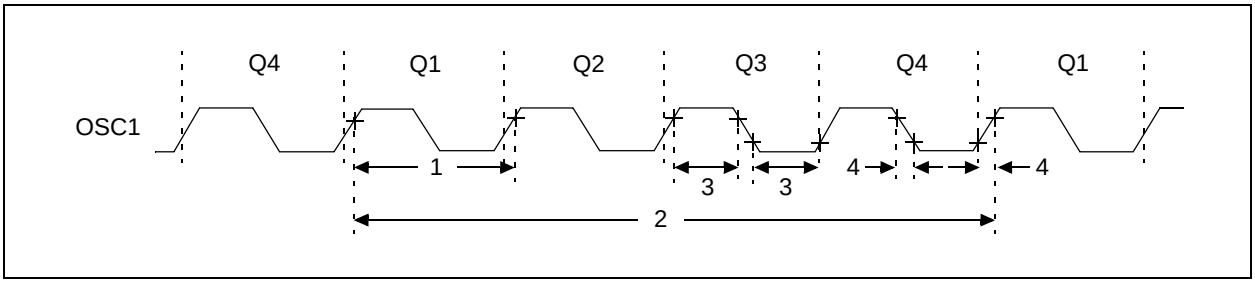


TABLE 4-3: EXTERNAL CLOCK TIMING REQUIREMENTS

AC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1 "DC Characteristics"				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period (3, 4)	271.3 271.3	— —	271.3 —	ns ns	Device Operation Low Power mode (PHACT drives Low)
		Oscillator Period (3)	271.3	—	271.3	ns	
1A	FOSC	External CLKIN Frequency (3, 4)	3.6864	3.6864	3.6864	MHz	
		Oscillator Frequency (3)	3.6864	—	3.6864	MHz	
1B	FERR	Error in Frequency	—	—	± 0.01	%	
1C	ECLK	External Clock Error	—	—	± 0.01	%	
3	TosH, TosL	Clock in (OSC1) High or Low Time	100 (2)	—	—	ns	
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	85 (2)	ns	

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: These parameters are for design guidance only and are not tested.

3: All specified values are based on oscillator characterization data under standard operating conditions. Exceeding these specified limits may result in unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

4: A duty cycle of no more than 60% (High time/Low time or Low time/High time) is recommended for external clock inputs.

FIGURE 4-4: $\overline{\text{RESET}}$ AND DEVICE RESET TIMING

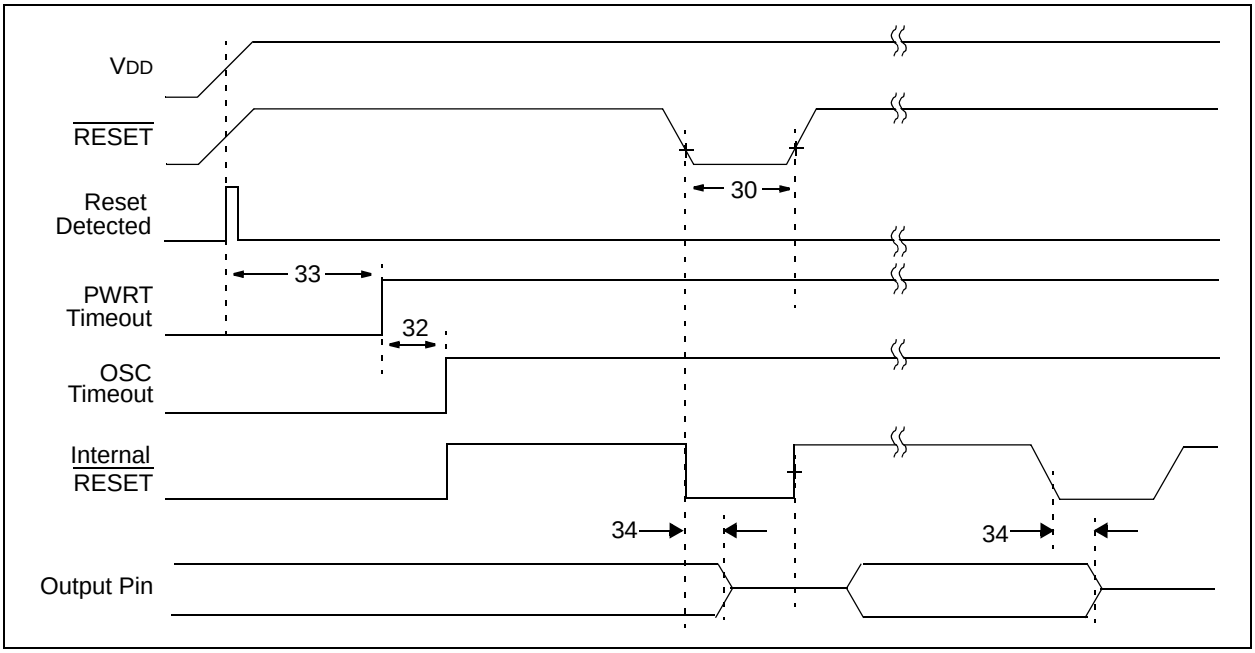


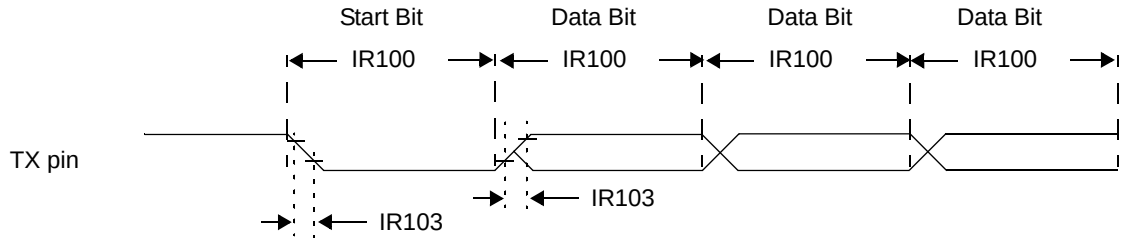
TABLE 4-4: $\overline{\text{RESET}}$ AND DEVICE RESET REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TRSTL	$\overline{\text{RESET}}$ Pulse Width (low)	2000	—	—	ns	VDD = 5.0V
32	TOST	Oscillator Start-up Timer Period	1024	—	1024	TOSC	
33	TPWRT	Power up Timer Period	28 (2)	72	132 (2)	ms	VDD = 5.0V
34	TIOZ	Output High-impedance from $\overline{\text{RESET}}$ Low or device Reset	—	—	2.0 (2)	µs	

Note 1: Data in the Typical ("Typ") column is at 5V, +25°C unless otherwise stated.

2: These parameters are for design guidance only and are not tested.

FIGURE 4-5: UART ASYNCHRONOUS TRANSMISSION WAVEFORM



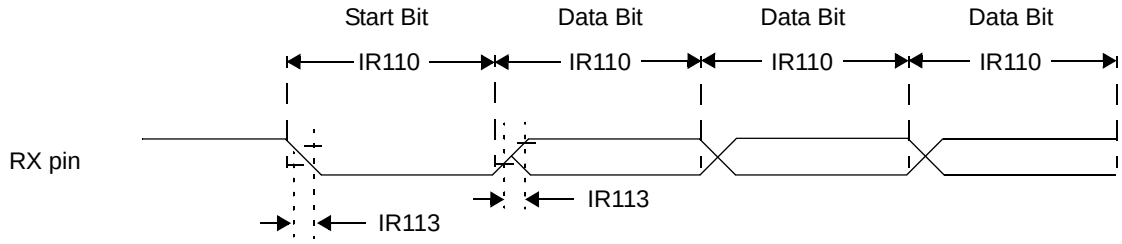
Note: Refer to Figure 4-2 for load conditions.

TABLE 4-5: UART ASYNCHRONOUS TRANSMISSION REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR100	TTXBIT	Transmit Baud rate	384	—	384	TOSC	
IR101	ETXBIT	Transmit (TX pin) Baud rate Error (into MCP2140A)	—	—	±2	%	
IR102	ETXIRBIT	Transmit (TXIR pin) Baud rate Error (out of MCP2140A) (1)	—	—	±1	%	

Note 1: This error is not additive to IR101 parameter.

FIGURE 4-6: UART ASYNCHRONOUS RECEIVE TIMING



Note: Refer to Figure 4-2 for load conditions.

TABLE 4-6: UART ASYNCHRONOUS RECEIVE REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85×C (industrial) Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR110	TRXBIT	Receive Baud Rate	384	—	384	TOSC	
IR111	ERXBIT	Receive (RXPD and RXPDREF pin detection) Baud rate Error (into MCP2140A)	—	—	±1	%	
IR112	ERXBIT	Receive (RX pin) Baud rate Error (out of MCP2140A) (1)	—	—	±1	%	

Note 1: This error is not additive to the IR111 parameter.

FIGURE 4-7: TXIR WAVEFORMS

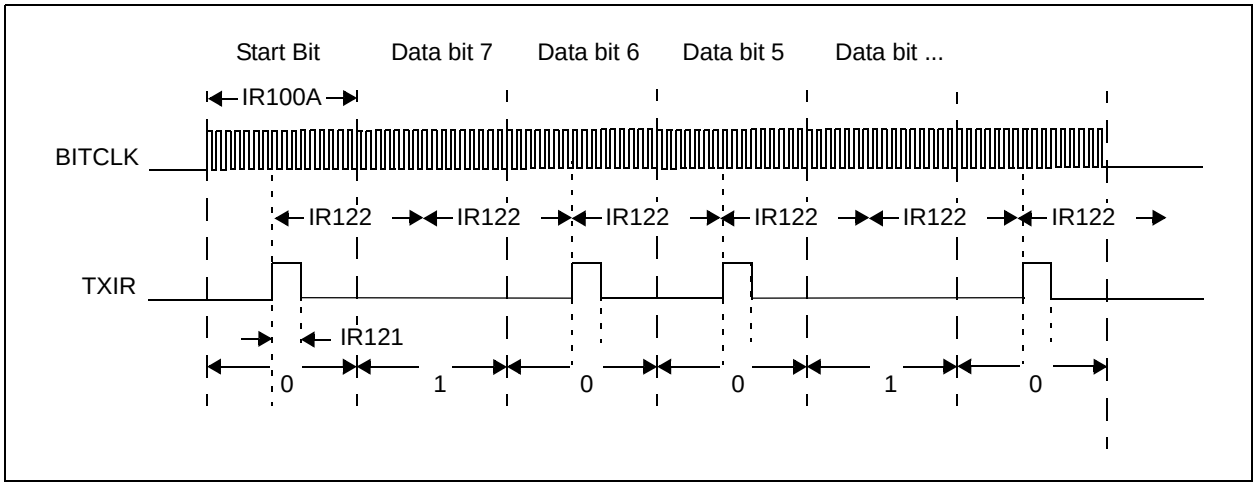


TABLE 4-7: TXIR REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR100A	TTXIRBIT	Transmit Baud Rate	384	—	384	TOSC	BAUD = 9600
IR121	TTXIRPW	TXIR pulse width	12	—	12	TOSC	
IR122	TTXIRP	TXIR bit period (1)	—	16	—	TBITCLK	

Note 1: TBITCLK = TTXBIT/16.

FIGURE 4-8: RXPD/RXPDREF WAVEFORMS

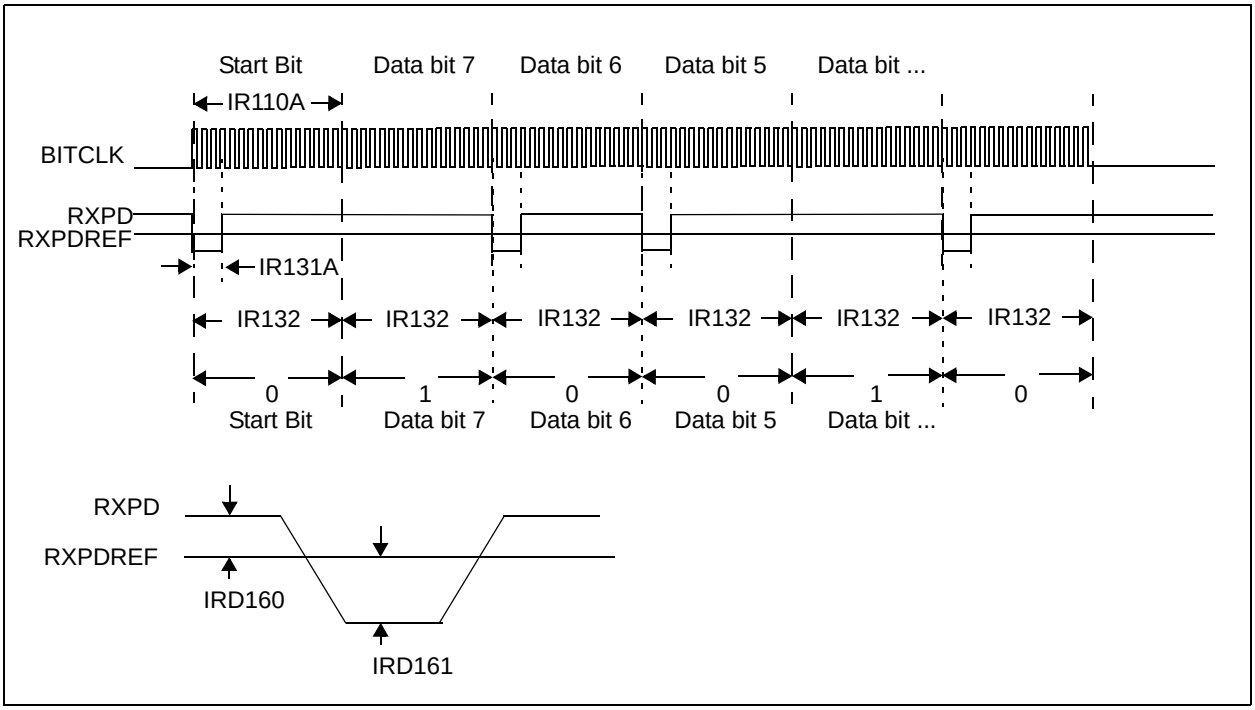


TABLE 4-8: RXPD/RXPDREF REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR110A	TRXPDBIT	Receive Baud Rate	384	—	384	TOSC	BAUD = 9600
IR132	TRXPDP	RXPD/RXPDREF bit period (1)	—	8	—	TBITCLK	
IRD060	VRXPDDΔ	Quiescent Delta Voltage between RXPD and RXPDREF	20	—	—	mV	
IRD061	VRXPDE	IR Pulse Detect Delta Voltage (RXPD to RXPDREF)	30	—	—	mV	RXPD signal must cross RXPDREF signal level
IR133	TRESP	Response Time (2)	—	—	600 *	ns	

* These parameters characterized but not tested.

Note 1: TBITCLK = TRXBIT/16.

2: Response time measured with RXPDREF at (VDD - 1.5V)/2, while RXPD transitions from VSS to VDD.

FIGURE 4-9: LOW POWER WAVEFORM

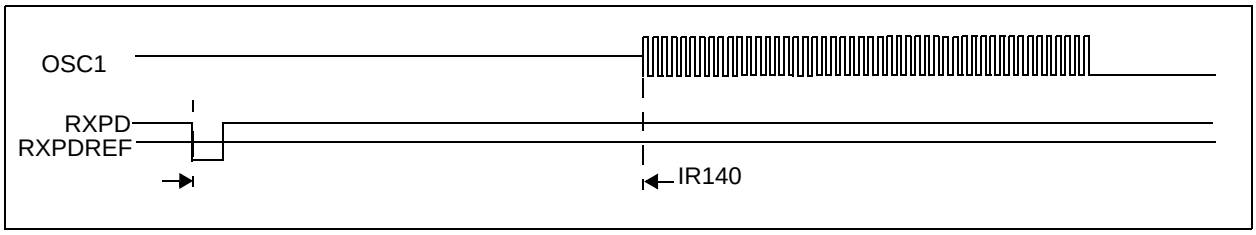


TABLE 4-9: LOW POWER REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in **Section 4.1 "DC Characteristics"**				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR140	TRXPD2OSC	RXPD pulse edge to valid device oscillator (1)	—	—	4	ms	

Note 1: At 9600 Baud, 4 ms is 4 bytes (of the 11 byte repeated SOF character). This allows the MCP2140A to recognize a SOF character and properly receive the IR packet.

5.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, all limits are specified for V_{DD} = 1V to 5.5V, T_A = -40°C to +125°C.

FIGURE 5-1: I_{DD} (PHACT = H) VS. TEMPERATURE

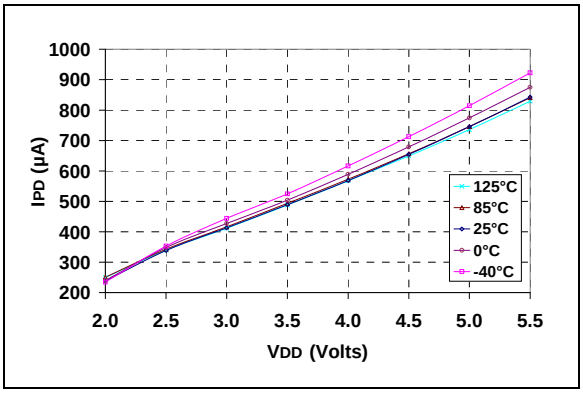
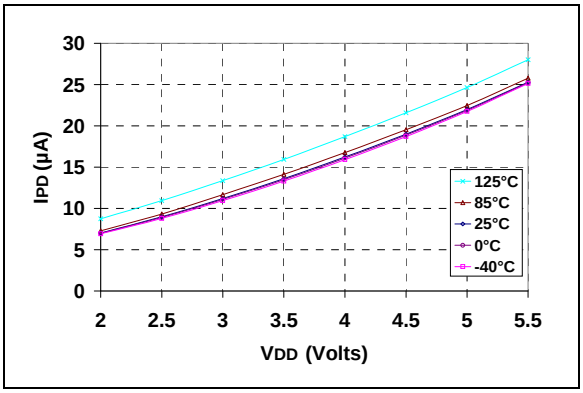


FIGURE 5-2: I_{DD} (PHACT = L) VS. TEMPERATURE

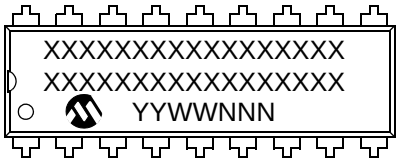


NOTES:

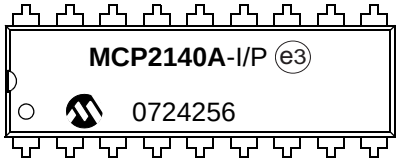
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

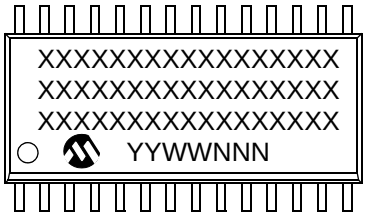
18-Lead PDIP (300 mil)



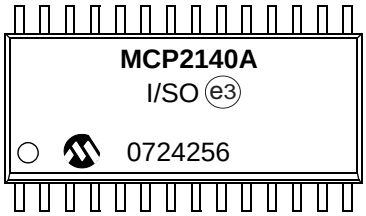
Example:



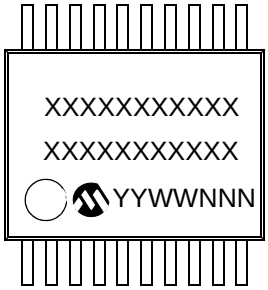
18-Lead SOIC (300 mil)



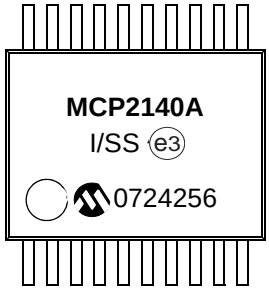
Example:



20-Lead SSOP (209 mil, 5.30 mm)



Example:

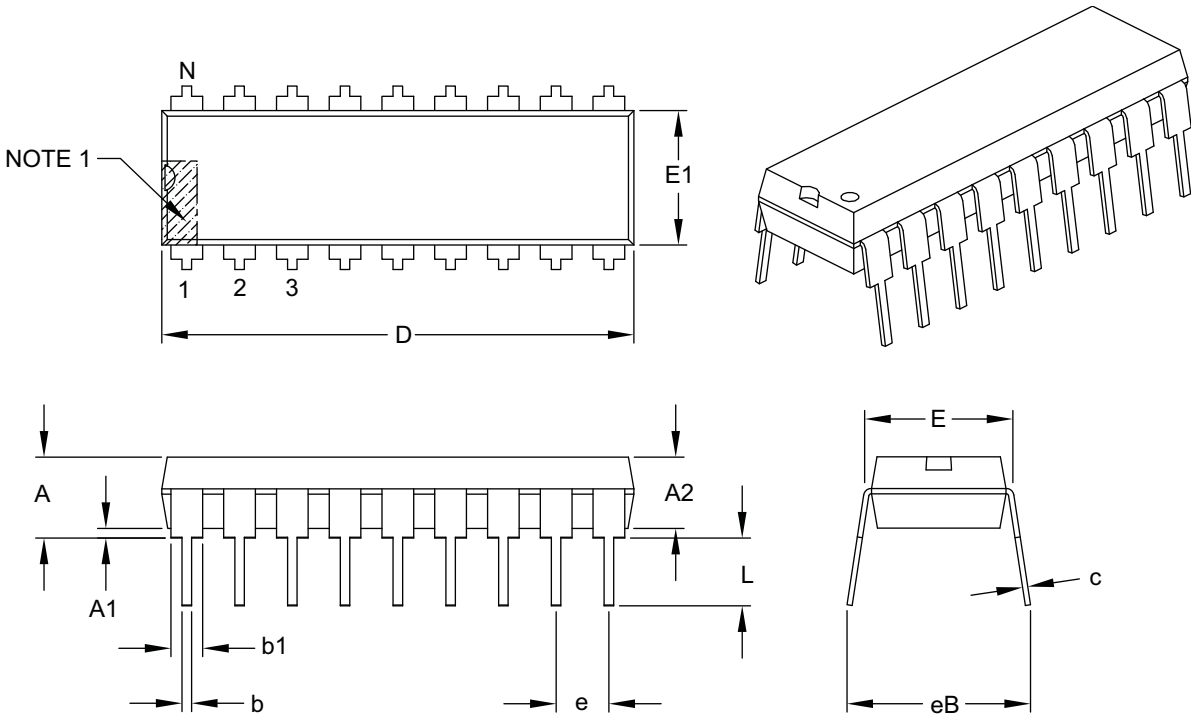


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

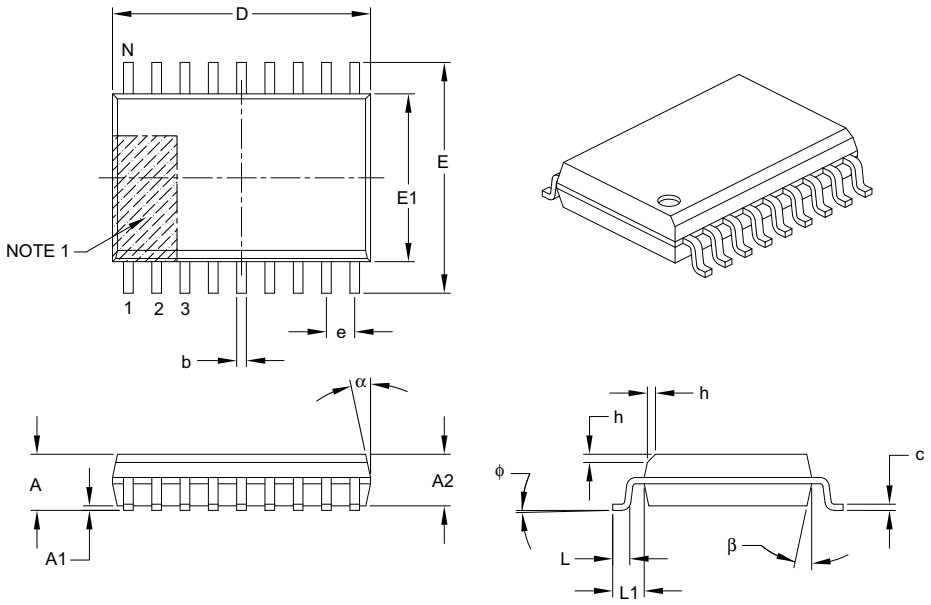
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

18-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		11.55 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

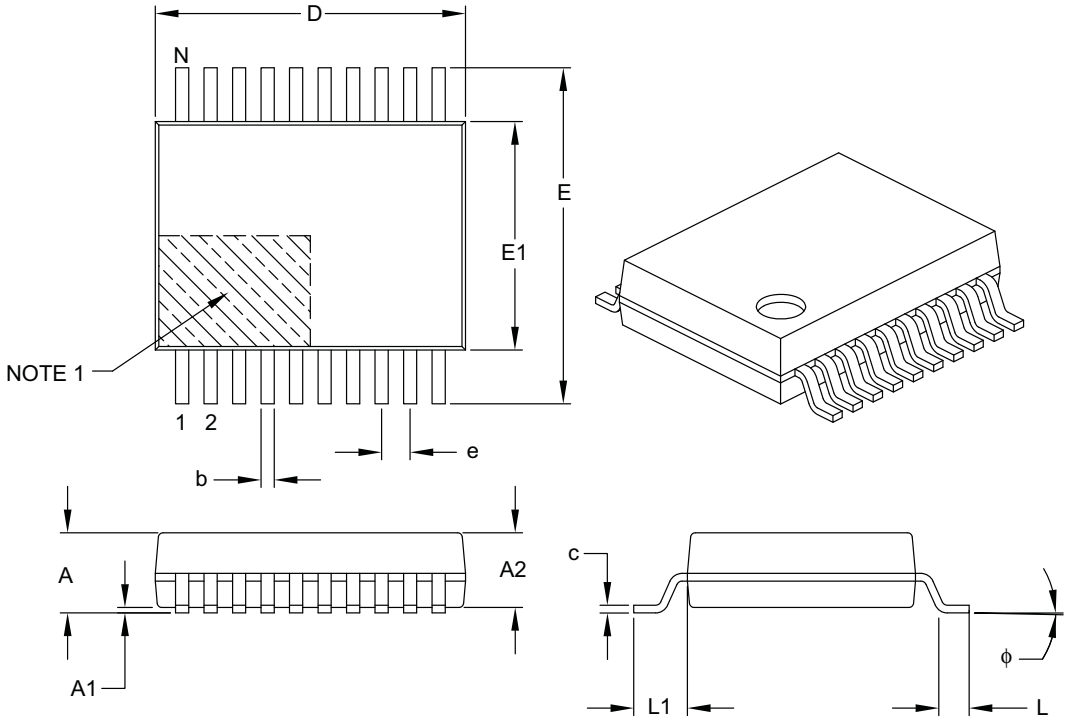
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-051B

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

APPENDIX A: REVISION HISTORY

Revision A (June 2007)

- Original release of this document

APPENDIX B: HOW DEVICES CONNECT

When two devices implementing the IrDA standard feature establish a connection using the IrCOMM protocol, the process is analogous to connecting two devices with serial ports using a cable. This is referred to as a “point-to-point” connection. This connection is limited to half-duplex operation because the IR transceiver cannot transmit and receive at the same time. The purpose of the IrDA protocols is to allow this half-duplex link to emulate, as much as possible, a full-duplex connection. In general, this is done by dividing the data into “packets”, or groups of data. These packets can then be sent back and forth, when needed, without risk of collision. The rules of how and when these packets are sent constitute the IrDA protocol. The MCP2140A supports elements of this IrDA standard protocol to communicate with other IrDA standard compatible devices.

When a wired connection is used, the assumption is made that both sides have the same communications parameters and features. A wired connection has no need to identify the other connector because it is assumed that the connectors are properly connected. In the IrDA standard, a connection process has been defined to identify other IrDA compatible devices and establish a communication link. There are three steps that these two devices go through to make this connection. They are:

- Normal Disconnect Mode (NDM)
- Discovery Mode
- Normal Connect Mode (NCM)

Figure B-1 shows the connection sequence.

B.1 Normal Disconnect Mode (NDM)

When two IrDA standard compatible devices come into range, they must first recognize each other. The basis of this process is that one device has some task to accomplish and the other device has a resource needed to accomplish this task. One device is referred to as a Primary Device and the other is referred to as a Secondary Device. This distinction between Primary Device and Secondary Device is important. It is the responsibility of the Primary Device to provide the mechanism to recognize other devices. So the Primary Device must first poll for nearby IrDA standard compatible devices. During this polling, the default baud rate of 9600 baud is used by both devices.

Note:	In the parlance of software development, the Primary Device is called a Client and the Secondary Device is called a Server.

For example, if you want to print from an IrDA equipped laptop to an IrDA printer, utilizing the IrDA standard feature, you would first bring your laptop in range of the printer. In this case, the laptop is the one that has something to do and the printer has the resource to do it. The laptop is called the Primary Device (Client) and the printer is the Secondary Device (Server). Some data-capable cell phones have IrDA standard infrared ports. If you used such a cell phone with a Personal Digital Assistant (PDA), the PDA that supports the IrDA standard feature would be the Primary Device and the cell phone would be the Secondary Device.

When a Primary Device polls for another device, a nearby Secondary Device may respond. When a Secondary Device responds, the two devices are defined to be in the Normal Disconnect Mode (NDM) state. NDM is established by the Primary Device broadcasting a packet and waiting for a response. These broadcast packets are numbered. Usually 6 or 8 packets are sent. The first packet is number 0, the last packet is usually number 5 or 7. Once all the packets are sent, the Primary Device sends an ID packet, which is not numbered.

The Secondary Device waits for these packets and then responds to one of the packets. The packet responds to determines the “timeslot” to be used by the Secondary Device. For example, if the Secondary Device responds after packet number 2, then the Secondary Device will use timeslot 2. If the Secondary Device responds after packet number 0, then the Secondary Device will use timeslot 0. This mechanism allows the Primary Device to recognize as many nearby devices as there are timeslots. The Primary Device will continue to generate timeslots and the Secondary Device should continue to respond, even if there’s nothing to do.

Note 1:	The MCP2140A can only be used to implement a Secondary Device.
2:	The MCP2140A supports a system with only one Secondary Device having exclusive use of the IrDA standard infrared link (known as “point-to-point” communication).
3:	The MCP2140A always responds to packet number 0. This means that the MCP2140A will always use timeslot 0.
4:	If another Secondary Device is nearby, the Primary Device may fail to recognize the MCP2140A, or the Primary Device may not recognize either of the devices.

During NDM, the MCP2140A handles all responses to the Primary Device (Figure B-1) without any communication with the Host Controller. The Host Controller is inhibited by the CTS signal of the MCP2140A from sending data to the MCP2140A.

B.2 Discovery Mode

Discovery mode allows the Primary Device to determine the capabilities of the MCP2140A (Secondary Device). Discovery mode is entered once the MCP2140A (Secondary Device) has sent an XID response to the Primary Device and the Primary Device has completed sending the XIDs and a Broadcast ID. If this sequence is not completed, a Primary and Secondary Device can stay in NDM indefinitely.

When the Primary Device has something to do, it initiates Discovery. Discovery has two parts. They are:

- Link initialization
- Resource determination

The first step is for the Primary and Secondary Devices to determine, and then adjust to, each other's hardware capabilities. These capabilities are parameters like:

- Data rate
- Turn around time
- Number of packets without a response
- How long to wait before disconnecting

Both the Primary and Secondary Devices begin communications at 9600 baud, which is the default baud rate. The Primary Device sends its parameters and the Secondary Device responds with its parameters. For example, if the Primary Device supports all data rates up to 115.2 kbaud and the Secondary Device only supports 9.6 kbaud, the link will be established at 9.6 kbaud.

Note:	The MCP2140A is limited to a data rate of 9.6 kbaud.

Once the hardware parameters are established, the Primary Device must determine if the Secondary device has the resources it requires. If the Primary Device has a job to print, then it must know if it's talking to a printer, not a modem or other device. This determination is made using the Information Access Service (IAS). The job of the Secondary Device is to respond to IAS queries made by the Primary Device. The Primary Device must ask a series of questions like:

- What is the name of your service?
- What is the address of this service?
- What are the capabilities of this device?

When all the Primary Device's questions are answered, the Primary Device can access the service provided by the Secondary Device.

During Discovery mode, the MCP2140A handles all responses to the Primary Device (see Figure B-1) without any communication with the Host Controller. The Host Controller is inhibited by the CTS signal of the MCP2140A from sending data to the MCP2140A.

B.3 Normal Connect Mode (NCM)

Once discovery has been completed, the Primary Device and Secondary Device can freely exchange data.

The MCP2140A uses a hardware handshake to stop the local serial port from sending data when the MCP2140A Host UART Receiving buffer is full.

Note:	Data loss will result if this hardware handshake is not observed.

Both the Primary Device and the MCP2140A (Secondary Device) check to make sure that data packets are received by the other without errors. Even when data is required to be sent, the Primary and Secondary Devices will still exchange packets to ensure that the connection hasn't, unexpectedly, been dropped. When the Primary Device has finished, it then transmits the close link command to the MCP2140A (Secondary Device). The MCP2140A will confirm the "close link" command and both the Primary Device and the MCP2140A (Secondary Device) will revert to the NDM state.

Note:	If the NCM mode is unexpectedly terminated for any reason (including the Primary Device not issuing a close link command), the MCP2140A will revert to the NDM state after a time delay (after the last frame has been received).

It is the responsibility of the Host Controller program to understand the meaning of the data received and how the program should respond to it. It's just as if the data were being received by the Host Controller from a UART.

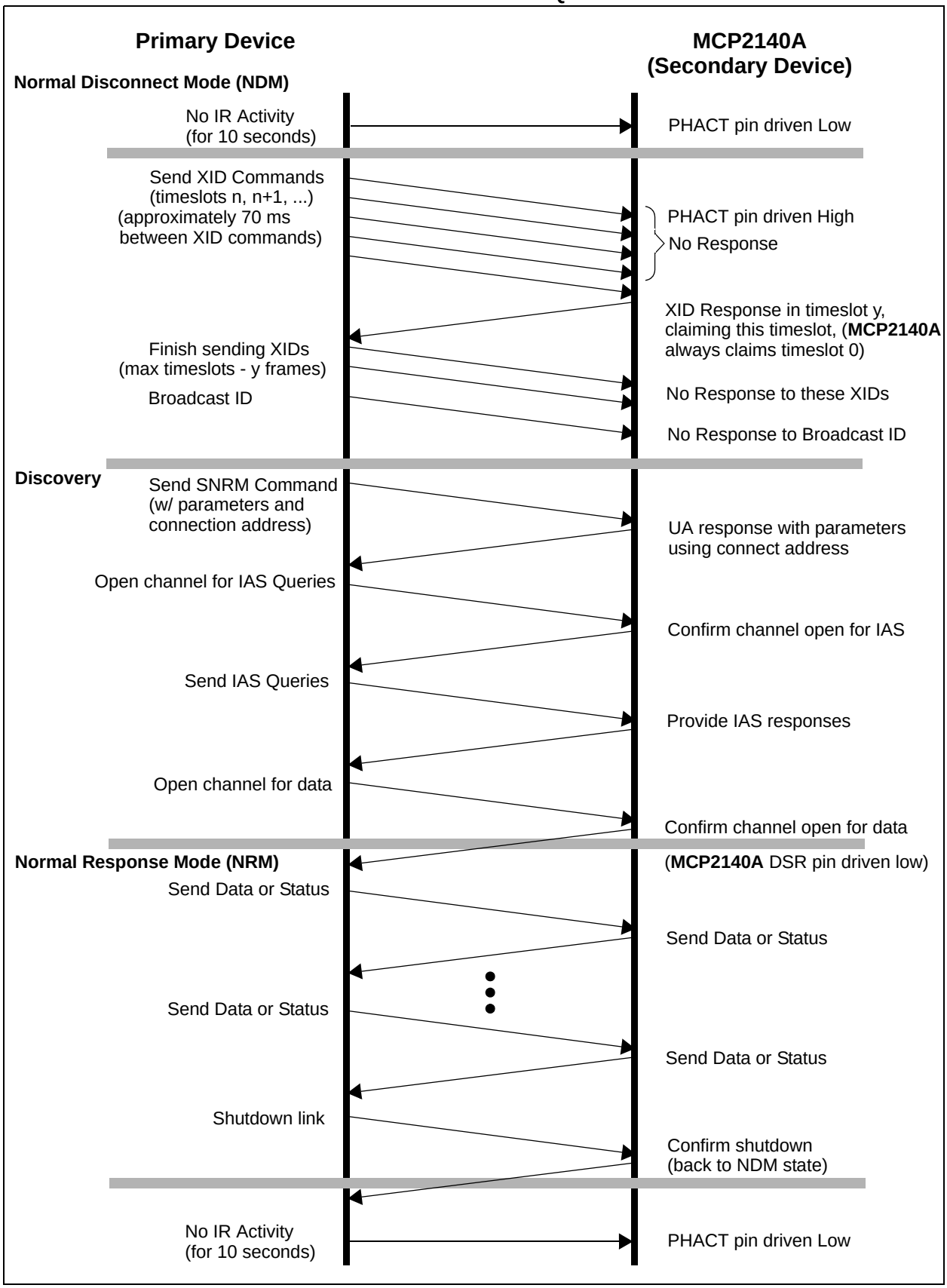
6.1.0.1 Primary Device Notification

The MCP2140A identifies itself to the Primary Device as a modem.

Note:	The MCP2140A identifies itself as a modem to ensure that it is identified as a serial device with a limited amount of memory.

However, the MCP2140A is not a modem, and the non-data circuits are not handled in a modem fashion.

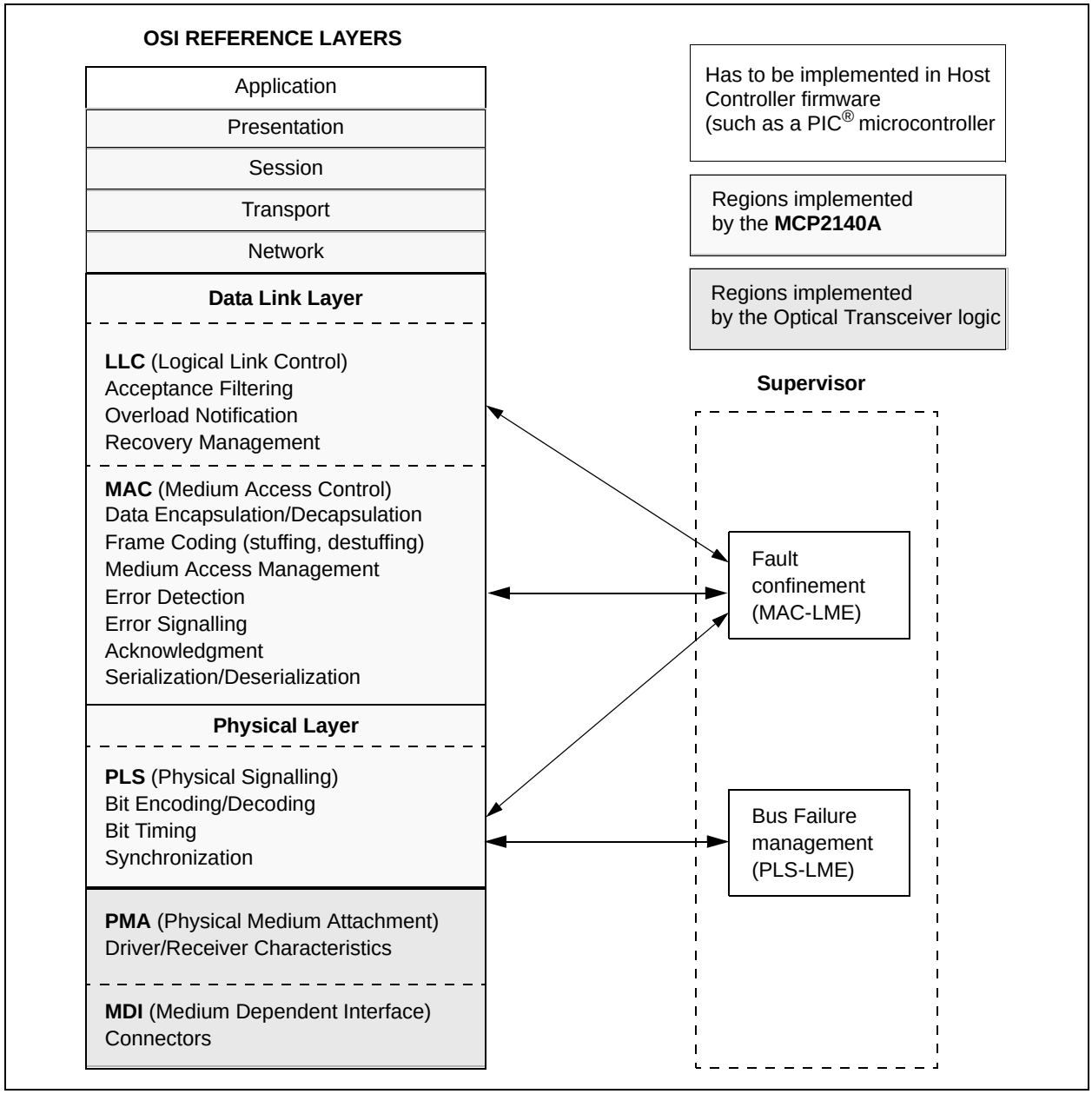
FIGURE B-1: HIGH LEVEL MCP2140A CONNECTION SEQUENCE



APPENDIX C: NETWORK LAYERING REFERENCE MODEL

Figure C-1 shows the ISO Network Layering Reference Model. The shaded areas are implemented by the MCP2140A, while the cross-hatched area is implemented by an infrared transceiver. The unshaded areas should be implemented by the Host Controller.

FIGURE C-1: ISO REFERENCE LAYER MODEL



The IrDA Standard specifies the following protocols:

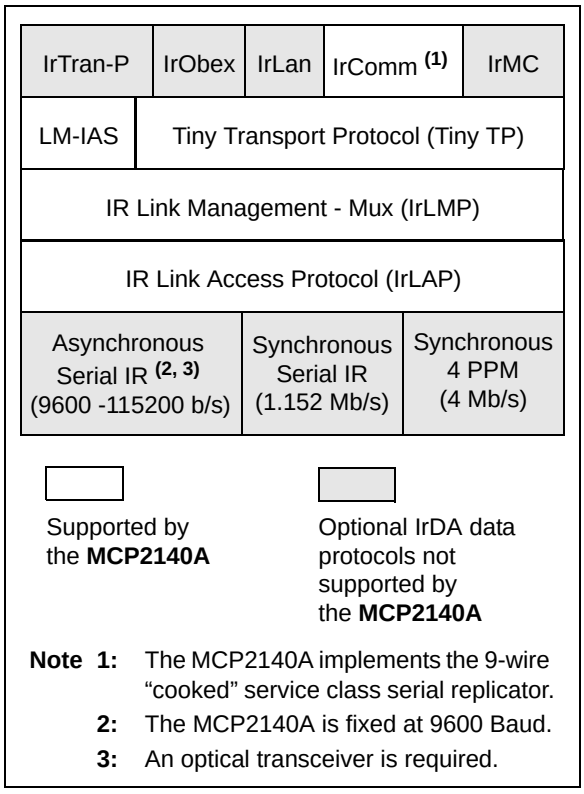
- Physical Signaling Layer (PHY)
- Link Access Protocol (IrLAP)
- Link Management Protocol/Information Access Service (IrLMP/IAS)

The IrDA data lists optional protocols. They are:

- Tiny TP
- IrTran-P
- IrOBEX
- IrLAN
- IrCOMM
- IrMC
- IrDA Lite

Figure C-2 shows the IrDA data protocol stack and which components are implemented by the MCP2140A.

FIGURE C-2: IRDA DATA - PROTOCOL STACKS



Note 1: The MCP2140A implements the 9-wire "cooked" service class serial replicator.
2: The MCP2140A is fixed at 9600 Baud.
3: An optical transceiver is required.

C.1 IrDA STANDARD DATA PROTOCOLS SUPPORTED BY MCP2140A

The MCP2140A supports these required IrDA standard protocols:

- Physical Signaling Layer (PHY)
- Link Access Protocol (IrLAP)
- Link Management Protocol/Information Access Service (IrLMP/IAS)

The MCP2140A also supports some of the optional protocols for IrDA data. The optional protocols that the MCP2140A implements are:

- Tiny TP
- IrCOMM

C.1.1 PHYSICAL SIGNAL LAYER (PHY)

The MCP2140A provides the following Physical Signal Layer specification support:

- Bidirectional communication
- Data Packets are protected by a CRC
  - 16-bit CRC for speeds up to 115.2 kbaud

Note: MCP2140A supports 9600 Baud only.

- Data Communication Rate
  - 9600 baud minimum data rate (with primary speed/cost steps of 115.2 kbaud

Note: MCP2140A supports 9600 Baud only.

The following Physical Layer Specification is dependant on the optical transceiver logic used in the application. The specification states:

- Communication Range, which sets the end user expectation for discovery, recognition and performance
  - Continuous operation from contact to at least 1 meter (typically 2 meters can be reached)
  - A low power specification reduces the objective for operation from contact to at least 20 cm (low power and low power) or 30 cm (low power and standard power)

C.1.2 IrLAP

The IrLAP protocol provides:

- Management of communication processes on the link between devices
- A device-to-device connection for the reliable, ordered transfer of data
- Device discover procedures
- Hidden node handling. 115.2 kbaud

Note:	Not supported by MCP2140A.

Figure C-3 identifies the key parts and hierarchy of the IrDA protocols. The bottom layer is the Physical layer, IrPHY. This is the part that converts the serial data to and from pulses of IR light. IR transceivers can't transmit and receive at the same time. The receiver has to wait for the transmitter to finish sending. This is sometimes referred to as a "Half-Duplex" connection. The IR Link Access Protocol (IrLAP) provides the structure for packets (or "frames") of data to emulate data that would normally be free to stream back and forth.

FIGURE C-3: IrDA STANDARD PROTOCOL LAYERS

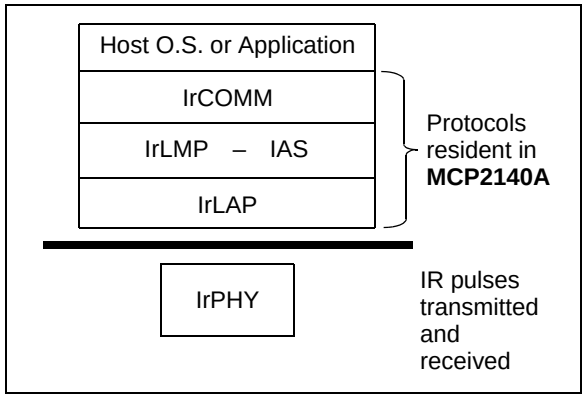
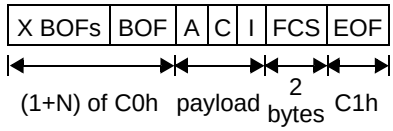


Figure C-4 shows how the IrLAP frame is organized. The frame is preceded by some number of Beginning of Frame characters (BOFs). The value of the BOF is generally 0xC0, but 0xFF may be used if the last BOF character is a 0xC0. The purpose of multiple BOFs is to give the other station some warning that a frame is coming.

The IrLAP frame begins with an address byte ("A" field), then a control byte ("C" field). The control byte is used to differentiate between different types of frames and is also used to count frames. Frames can carry status, data or commands. The IrLAP protocol has a command syntax of it's own. These commands are part of the control byte. Lastly, IrLAP frames carry data. This data is the information (or "I") field. The integrity of the frame is ensured with a 16-bit CRC, referred to as the Frame Check Sequence (FCS). The 16-bit CRC value is transmitted LSB first. The end of the frame is marked with an EOF character, which is always a 0xC1. The frame structure described here is used for all versions of IrDA protocols used for serial wire replacement for speeds up to 115.2 kbaud.

Note 1:	The MCP2140A only supports communication baud rate of 9600 baud.
2:	Another IrDA standard that is entering into general usage is IR Object Exchange (IrOBEX). This standard is not used for serial connection emulation.
3:	IrDA communication standards faster than 115.2 kbaud use a different CRC method and physical layer.

FIGURE C-4: IrLAP FRAME



In addition to defining the frame structure, IrLAP provides the "housekeeping" functions of opening, closing and maintaining connections. The critical parameters that determine the performance of the link are part of this function. These parameters control how many BOFs are used, identify the speed of the link, how fast either party may change from receiving to transmitting, etc. IrLAP has the responsibility of negotiating these parameters to the highest common set so that both sides can communicate as quickly and reliably as possible.

C.1.3 IrLMP

The IrLMP protocol provides:

- Multiplexing of the IrLAP layer. This allows multiple channels above an IrLAP connection
- Protocol and service discovery. This is accomplished via the Information Access Service (IAS)

When two devices that contain the IrDA standard feature are connected, there is generally one device that has something to do and the other device that has the resource to do it. For example, a laptop may have a job to print and an IrDA standard compatible printer has the resources to print it. In IrDA standard terminology, the laptop is a Primary Device and the printer is the Secondary Device. When these two devices connect, the Primary Device must determine the capabilities of the Secondary Device to determine if the Secondary Device is capable of doing the job. This determination is made by the Primary Device asking the Secondary Device a series of questions. Depending on the answers to these questions, the Primary Device may or may not elect to connect to the Secondary Device.

The queries from the Primary Device are carried to the Secondary Device using IrLMP. The responses to these queries can be found in the Information Access Service (IAS) of the Secondary Device. The IAS is a list of the resources of the Secondary Device. The Primary Device compares the IAS responses with its requirements and then makes the decision if a connection should be made.

C.1.4 LINK MANAGEMENT - INFORMATION ACCESS SERVICE (LM-IAS)

Each LM-IAS entity maintains an information database to provide:

- Information on services for other devices that contain the IrDA standard feature (Discovery)
- Information on services for the device itself
- Remote accessing of another device's information base

This is required so that clients on a remote device can find configuration information needed to access a service.

C.1.5 TINY TP

Tiny TP provides the flow control on IrLMP connections. An optional service of Segmentation and Reassembly can be handled.

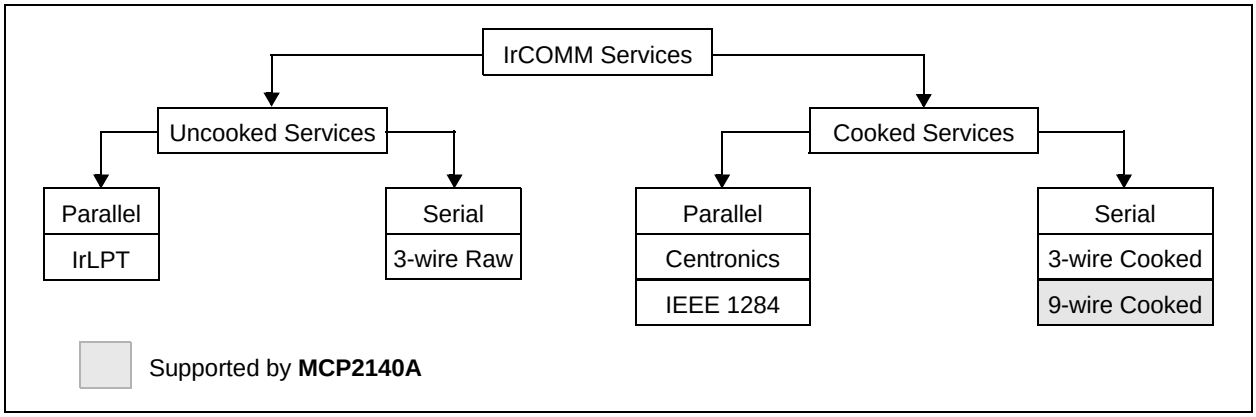
C.1.6 IRCOMM

IrCOMM provides the method to support serial and parallel port emulation. This is useful for legacy COM applications, such as printers and modem devices.

The IrCOMM standard is a syntax that allows the Primary Device to consider the Secondary Device a serial device. IrCOMM allows for emulation of serial or parallel (printer) connections of various capabilities.

Note:	The MCP2140A supports the 9-wire "cooked" service class of IrCOMM. Other service classes supported by IrCOMM are shown in Figure C-5.

FIGURE C-5: IRCOMM SERVICE CLASSES



C.1.7 OTHER OPTIONAL IRDA DATA PROTOCOLS

Other IrDA data protocols have been developed to specific application requirements. These IrDA data protocols are briefly described in the following subsections. For additional information, please refer to the IrDA web site **(www.IrDA.org)**.

C.1.7.1 IrTran-P

IrTran-P provides the protocol to exchange images with digital image capture devices/cameras.

Note:	Not supported by MCP2140A.

C.1.7.2 IrOBEX

IrOBEX provides OBject EXchange services. This is similar to HTTP.

Note:	Not supported by MCP2140A.

C.1.7.3 IrLAN

IrLAN describes a protocol to support IR wireless access to a Local Area Network (LAN).

Note:	Not supported by MCP2140A.

C.1.7.4 IrMC

IrMC describes how mobile telephony and communication devices can exchange information. This information includes phone book, calender and message data.

Also how call control and real-time voice are handled (RTCON).

Note:	Not supported by MCP2140A.

C.1.7.5 IrDA Lite

IrDA Lite describes how to reduce the application code requirements, while maintaining compatibility with the full implementation.

Note:	Not supported by MCP2140A.

APPENDIX D: DB-9 PIN INFORMATION

Table D-1 shows the DB-9 pin information and the direction of the MCP2140A signals. The MCP2140A is designed for use in Data Communications Equipment (DCE) applications.

TABLE D-1: DB-9 SIGNAL INFORMATION

DB-9 Pin No.	Signal	Direction	Comment
1	CD	HC → MCP2140A	Carrier Detect
2	RX	MCP2140A → HC	Received Data
3	TX	HC → MCP2140A	Transmit Data
4	DTR	HC → MCP2140A	Data Terminal Ready
5	GND	—	Ground
6	DSR	MCP2140A → HC	Data Set Ready
7	RTS	HC → MCP2140A	Request to Send
8	CTS	MCP2140A → HC	Clear to Send
9	RI	HC → MCP2140A	Ring Indicator

Legend: HC = Host Controller

APPENDIX E: KNOW PRIMARY DEVICE COMPATIBILITY ISSUES

- None

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	MCP2140A: Infrared Communications Controller MCP2140AT: Infrared Communications Controller (Tape and Reel)
Temperature Range	I = -40°C to +85°C
Package	P = Plastic DIP (300 mil, Body), 18-lead SO = Plastic SOIC (300 mil, Body), 18-lead SS = Plastic SSOP (209 mil, Body), 20-lead

Examples:

a) MCP2140A-I/P: Industrial Temp., PDIP packaging

b) MCP2140A-I/SO: Industrial Temp., SOIC package

c) MCP2140AT-I/SS: Tape and Reel, Industrial Temp., SSOP package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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