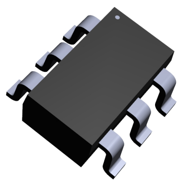
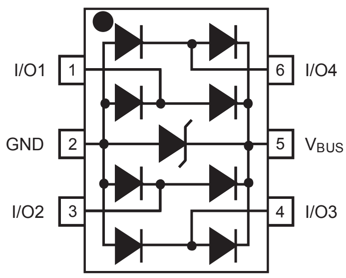
DVIULC6-4SC6Y

Datasheet

Automotive ultralow capacitance ESD protection



SOT23-6L



Product status link
DVIULC6-4SC6Y

Product summary	
Order code	DVIULC6-4SC6Y
Package	SOT23-6L
Packing	Tape and reel

Features

- AEC-Q101 qualified
- 4-line ESD protection (IEC 61000-4-2)
- Protects V_{BUS} when applicable
- Ultralow capacitance: 0.6 pF at F = 825 MHz
- Fast response time compared with varistors
- RoHS compliant
- **Benefits:**
- ESD protection of V_{BUS}
- Optimized rise and fall times for maximum data integrity
- Consistent D+ / D- signal balance:
  - Optimum capacitance matching tolerance for ultralow intra pair skew: I/O to ground = 0.015 pF, I/O to I/O = 0.007 pF
  - Matching high bit rate DVI, HDMI, and IDB 1394 bus requirements
- Low PCB space occupation: 9 mm²
- Higher reliability offered by monolithic integration
- Complies with the standard ISO 10605 (C = 330 pF, R = 330 Ω)
  - ±18 kV (air discharge, contact discharge)
- Complies with the standard ISO 10605 (C = 150 pF, R = 330 Ω)
  - ±18 kV (air discharge, contact discharge)
- MIL STD883G-Method 3015-7
- Complies with the standard ISO 7637-3
  - Pulse 3a: V_S = -150 V
  - Pulse 3b: V_S = +100 V

Application

- DVI ports and HDMI ports up to 1.65 Gb/s
- IDB 1394
- USB 2.0 ports up to 480 Mb/s (high speed), backwards compatible with USB1.1 low and full speed
- Ethernet port: 10/100/1000 Mb/s
- SIM card protection
- Video line protection

Description

The DVIULC6-4SC6Y is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces, such as DVI, HDMI, IDB 1394 bus, USB2.0, Ethernet links and video lines.

Its ultralow line capacitance secures a high level of signal integrity without compromise in protecting sensitive chips against the most stringently characterized ESD strikes.

1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	ISO 10605 / IEC 61000-4-2 (C = 150 pF, R = 330 Ω) Contact discharge Air discharge	 ±18 ±18	kV
		ISO 10605 (C = 330 pF, R = 330 Ω) Contact discharge Air discharge	 ±18 ±18	
		MIL STD883G-Method 3015-7	±25	
T_{stg}	Storage temperature range		-65 to +125	°C
T_j	Operating junction temperature range		-40 to +125	°C
T_L	Maximum temperature for soldering during 10 s		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{RM}	Reverse leakage current	V_{RM} = 5 V			0.5	µA
V_{BR}	Reverse breakdown voltage	I_R = 1 mA	6			V
V_{CL}	ESD clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, t_p = 8/20 µs Any I/O pin to GND			17	V
$C_{I/O-GND}$	Capacitance between I/O and GND	V_R = 0 V, F = 1 MHz		0.85	1	pF
		V_R = 0 V, F = 825 MHz		0.6		
$\Delta C_{I/O-GND}$	Capacitance variation between I/O and GND			0.015		pF
$C_{I/O-I/O}$	Capacitance between I/O	V_R = 0 V, F = 1 MHz		0.42	0.5	pF
		V_R = 0 V, F = 825 MHz		0.3		
$\Delta C_{I/O-I/O}$	Capacitance variation between I/O			0.007		pF

1.1 Characteristics (curves)

Figure 1. Line capacitance versus line voltage (typical values)

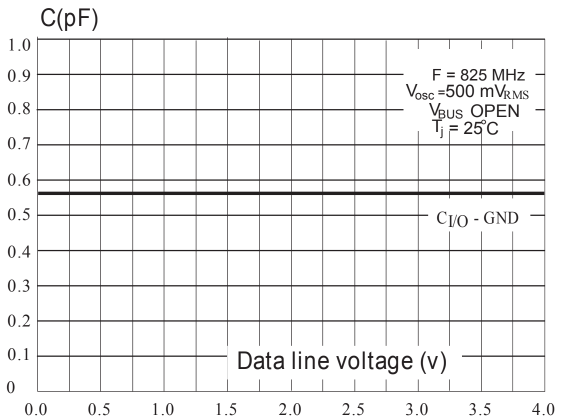


Figure 2. Line capacitance versus frequency (typical values)

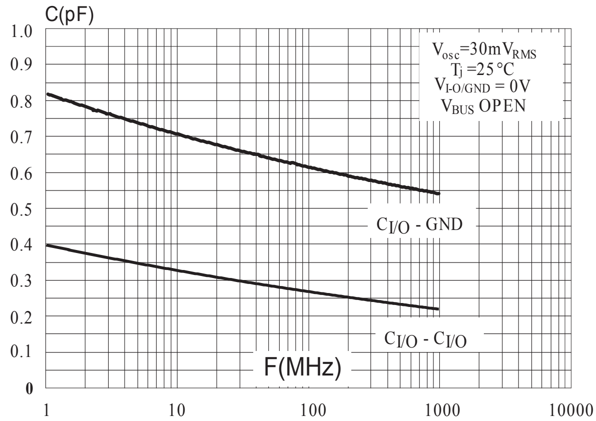


Figure 3. Relative variation of leakage current versus junction temperature (typical values)

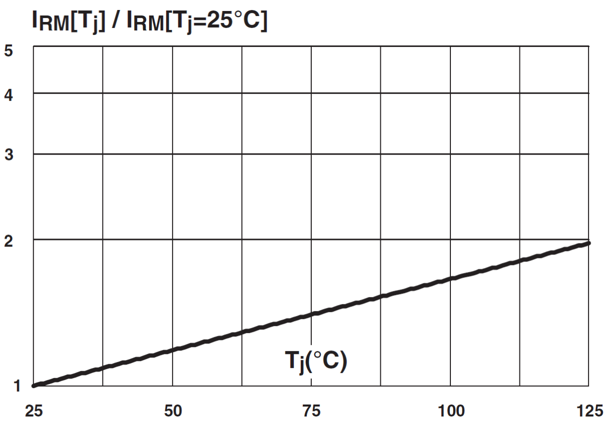


Figure 4. Frequency response

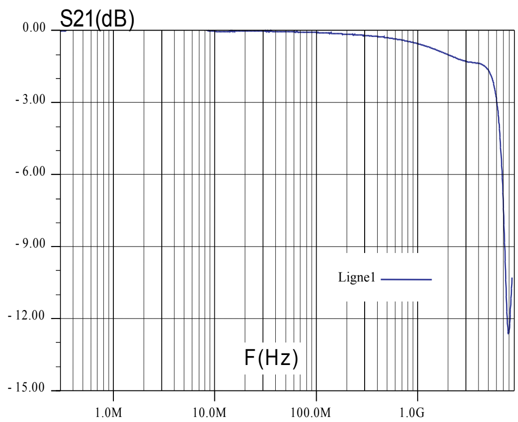


Figure 5. Remaining voltage after the DVIULC6-4SC6Y during positive ESD surge

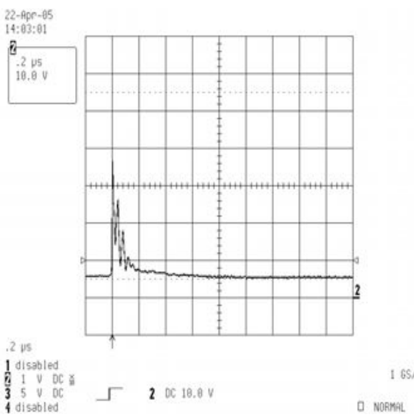
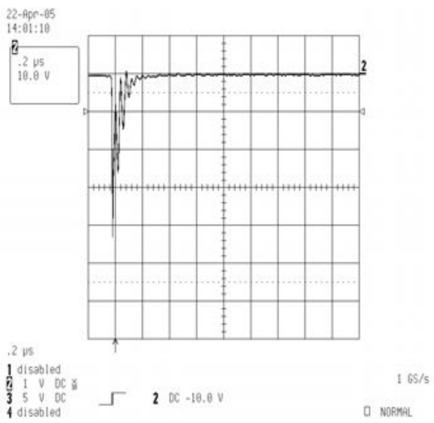


Figure 6. Remaining voltage after the DVIULC6-4SC6Y during positive ESD surge



Note: Measurements were done with DVIULC-4SC6 in open circuit

Figure 7. **Analog crosstalk results**

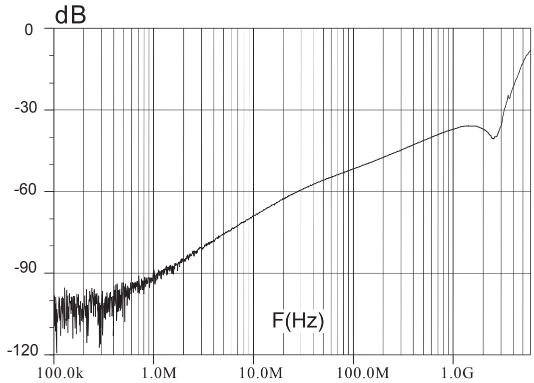


Figure 8. **ISO7637-3 pulse 3a response (V_S = -150 V)**

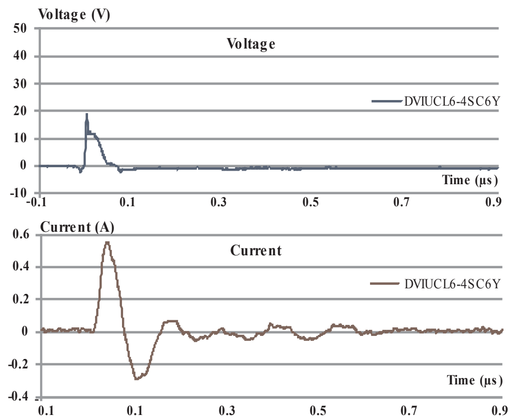
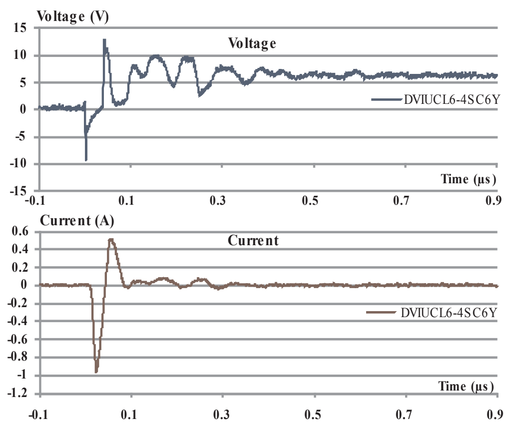


Figure 9. **ISO7637-3 pulse 3b response (V_S = 100 V)**



2 Application examples

More information is available in the STMicroelectronics Application note AN2689 “Protection of automotive electronics from electrical hazards, guidelines for design and component selection”.

Figure 10. **DVI/HDMI digital single link application**

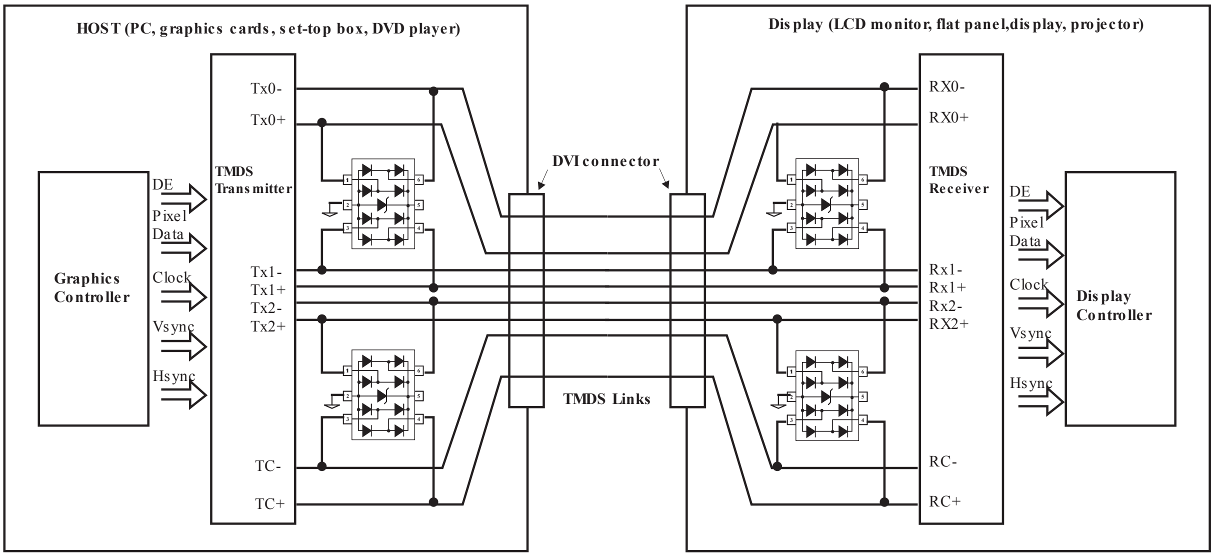
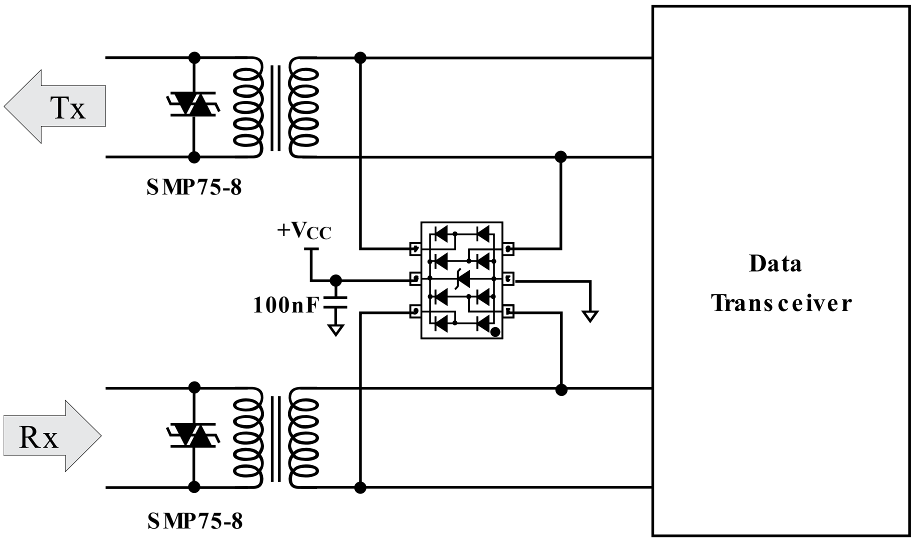


Figure 11. **T1/E1/Ethernet protection**



3 Technical information

3.1 Surge protection

The DVIULC6-4SC6Y is particularly optimized to perform ESD surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follows:

- $V_{CL^+} = V_{BUS} + V_F$, for positive surges
- $V_{CL^-} = - V_F$, for negative surges

with: $V_F = V_T + R_D.I_P$

(V_F = forward drop voltage) / (V_T = forward drop threshold voltage)

Calculation example

We can assume that the value of the dynamic resistance of the clamping diode is typically:

- $R_D = 1.4\ \Omega$ and $V_T = 1.2$ V

For an IEC 61000-4-2 surge level 4 (contact discharge: $V_G = 8$ kV, $R_G = 330\ \Omega$), $V_{BUS} = +5$ V, and, in a first approximation, we assume that:

- $I_P = V_G / R_G = 24$ A

We find:

- $V_{CL^+} = +39$ V
- $V_{CL^-} = -34$ V

Note: The calculations do not take into account phenomena due to parasitic inductances.

3.2 Surge protection application example

If we consider that the connections from the pin V_{BUS} to V_{CC} and from GND to PCB GND plane are two tracks 10 mm long and 0.5 mm wide, we can assume that the parasitic inductances, L_W of these tracks are about 6 nH. So when an IEC 61000-4-2 surge occurs, due to the rise time of this spike (t_r = 1 ns), the voltage V_{CL} has an extra value equal to L_W.dI/dt.

The dI/dt is calculated as:

- $dI/dt = I_P/t_r = 24$ A/ns for an IEC 61000-4-2 surge level 4 (contact discharge $V_G = 8$ kV, $R_G = 330\ \Omega$)

The over voltage due to the parasitic inductances is: LW.dI/dt = 6 x 24 = 144 V.

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

- $V_{CL^+} = +39 + 144 = 183$ V
- $V_{CL^-} = -34 - 144 = -178$ V

We can reduce as much as possible these phenomena with simple layout optimization.

This is the reason why some recommendations have to be followed (see Section 3.3: How to ensure good ESD protection.

3.3 How to ensure good ESD protection

While the DVIULC6-4SC6Y provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from V_{BUS} pin to the power supply $+V_{CC}$, and from V_{BUS} pin to GND pin must be as short as possible to avoid over voltages due to parasitic phenomena (see Figure 12 and Figure 13 for layout considerations).

Figure 12. IESD behavior: parasitic phenomena due to unsuitable layout

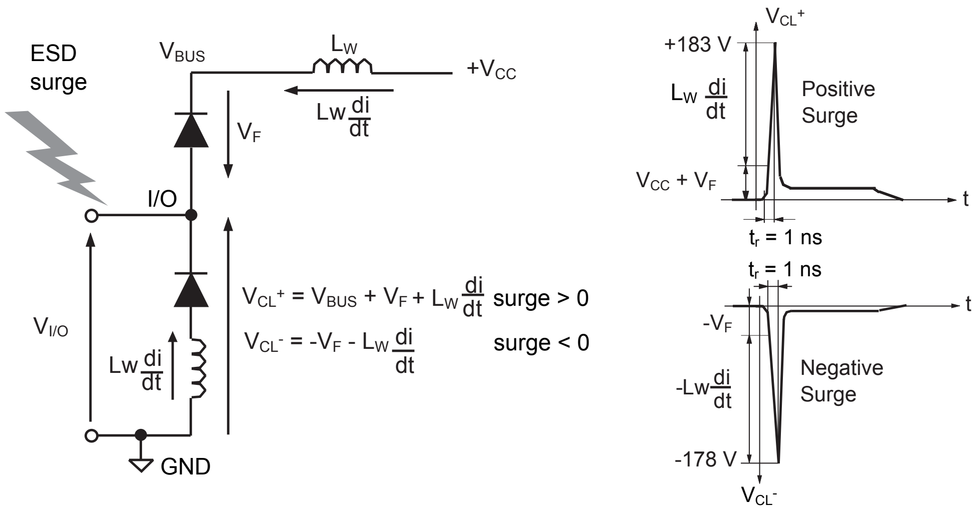


Figure 13. ESD behavior: layout optimization and addition of a 100 nF capacitor

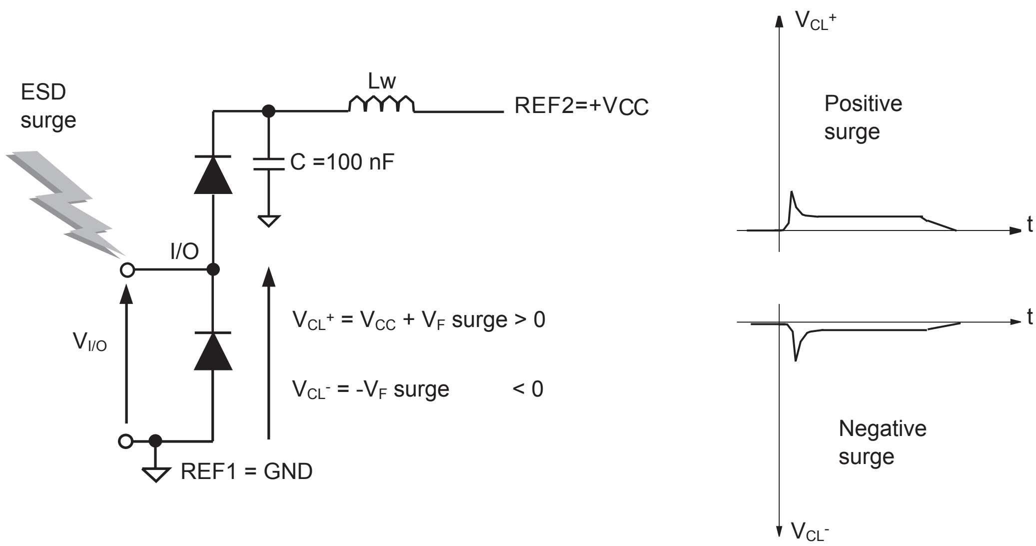
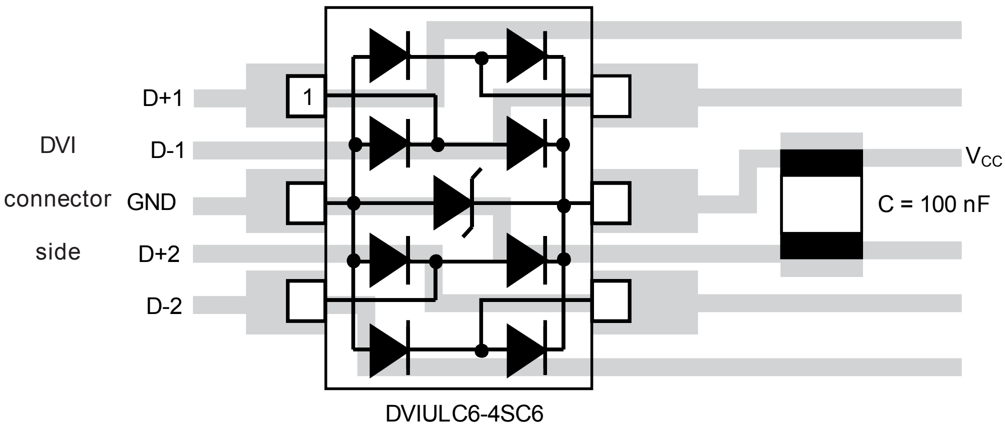
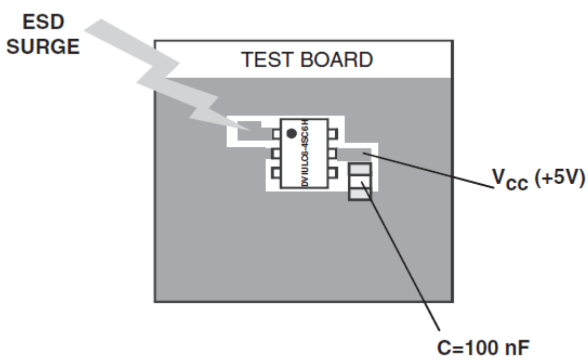


Figure 14. **PCB layout considerations (VCC connection is application dependent)**



It's often harder to connect the power supply near to the DVIULC6-4SC6Y unlike the ground thanks to the ground plane that allows a short connection. To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend to put close to the DVIULC6-4SC6Y, between VBUS and ground, a capacitance of 100 nF to prevent from these kinds of overfatigue disturbances (see Figure 13 and Figure 14). The addition of this capacitance will allow a better protection by providing a constant voltage during a surge.
Figure 15, Figure 5, and Figure 6 show the improvement of the ESD protection according to the recommendations described in Section 3.3: How to ensure good ESD protection.

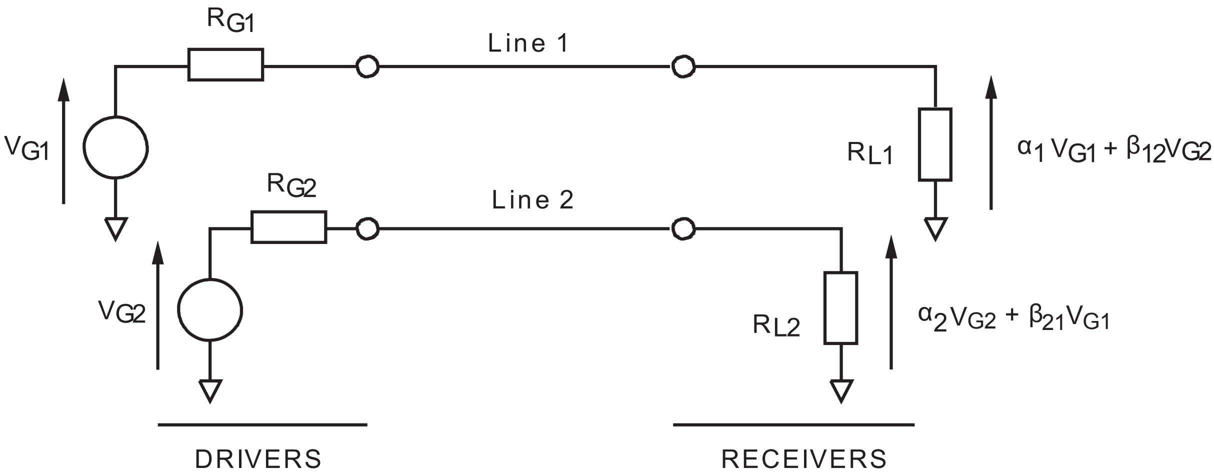
Figure 15. **ESD behavior: measurement conditions (with coupling capacitor)**



Important: *An important precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).*

3.4 Crosstalk behavior

Figure 16. **Crosstalk phenomena**



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor (β12 or β21) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load RL2 is $\alpha 2V_{G2}$, in fact the real voltage at this point has got an extra value $\beta 21V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of line 1 on line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 17. **Analog crosstalk measurements**

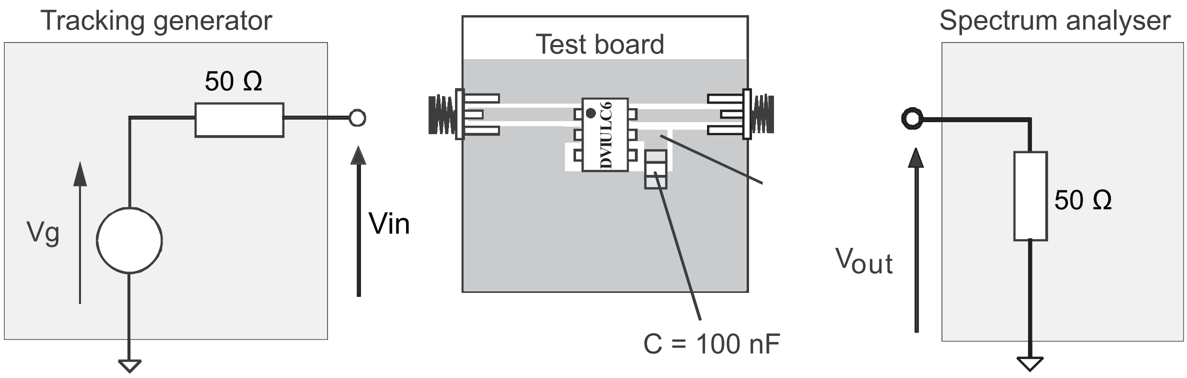


Figure 17 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -45 dB (see Figure 7).

As the DVIULC6-4SC6Y is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (Figure 4) gives attenuation information and shows that the DVIULC6-4SC6Y is well suitable for data line transmission up to 1.65 Gb/s.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT23-6L package information

- Epoxy meets UL 94,V0
- Lead-free package

Figure 18. SOT23-6L package outline

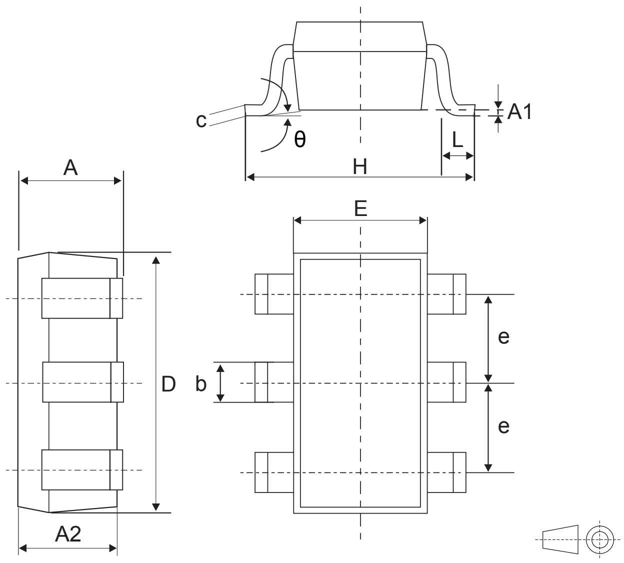
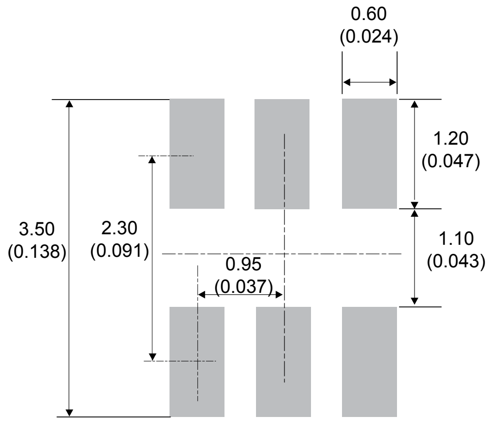


Table 3. SOT23-6L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.15	0		0.006
A2	0.90		1.30	0.035		0.051
b	0.30		0.50	0.012		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.110		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.30		0.60	0.012		0.024
θ	0°		10°	0°		10°

1. *Value in inches are converted from mm and rounded to 4 decimal digits*

Figure 19. Footprint recommendations, dimensions in mm (inches)



5 Ordering information

Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
DVIULC6-4SC6Y	DL4Y	SOT23-6L	16.7 mg	3000	Tape and reel

Revision history

Table 5. **Document revision history**

Date	Version	Changes
24-May-2011	1	First issue.
06-Sep-2012	2	Updated dimension A1 max., b min., and L min. in Table 3.
18-Jul-2024	3	Updated Table 1, and Figure 3.