PT5820 Series

16-A 12-V Input Adjustable Integrated Switching Regulator

EXCALIBUR

SLTS172

(Released 8/23/2002)

Features

- 12V Input
- DSP Compatible
- High Efficiency (90+%)
- Output Margin Control (±5%)
- Adjustable Output Voltage
- On/Off Enable Function
- Over-Current Protection
- Thermal Shutdown
- Low-Profile (8mm)
- Small Footprint (0.736 in², Suffix 'N')
- Solderable Copper Case
- Surface Mount Compatible

Description

The PT5820 Excalibur™ series of integrated switching regulators (ISRs) combines outstanding power density with a comprehensive list of features. They are an ideal choice for applications where board space is a premium and performance cannot be compromised. These modules provide a full 16A of output current, yet are housed in a low-profile, 18-pin, package. The integral copper case construction requires no heatsink, and offers the advantages of solderability and a small footprint (0.736 in² for suffix 'N'). Both through-hole and surface mount pin configurations are available.

The PT5820 series operates from a 12-V input bus and provides a convenient point-of-load power source for the industry's latest high-performance DSPs and microprocessors. The series includes output voltage options as low as 1.0VDC.

Other features include external output voltage adjustment, a ±5% margin control, on/off enable, short circuit protection, and thermal shutdown. A 560-µF input capacitor and 330µF output capacitor are required for proper operation.

Ordering Information

PT5827❒	= 5.0 Volts
PT5821❒	= 3.3 Volts
PT5822❒	= 2.5 Volts
PT5823❒	= 1.8 Volts
PT5824❒	= 1.5 Volts
PT5825❒	= 1.2 Volts
PT5826❒	= 1.0 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(EPP)
Horizontal	**A**	(EPQ)
SMD	**C**	(EPS)

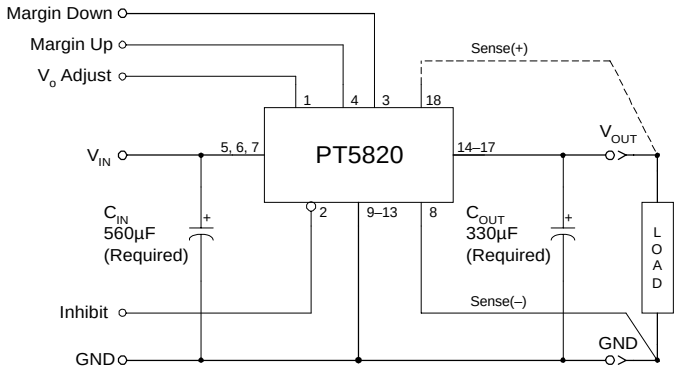
(Reference the applicable package code drawing for the dimensions and PC board layout)

Pin-Out Information

Pin	Function
1	V_o Adjust
2	Inhibit *
3	Margin Down
4	Margin Up
5	V_{in}
6	V_{in}
7	V_{in}
8	Sense(–)
9	GND
10	GND
11	GND
12	GND
13	GND
14	V_{out}
15	V_{out}
16	V_{out}
17	V_{out}
18	Sense(+)

** For Inhibit pin:*
Open = output enabled
Ground = output disabled

Standard Application



C_{in} = Required 560µF
C_{out} = Required 330µF (Note 3)

Performance Specifications (Unless otherwise stated, T_a =25°C, V_{in} =12V, C_{in} =560µF, C_{out} =330µF, and I_o =$I_o$max)

Characteristics	Symbols	Conditions	PT5820 Series Min	Typ	Max	Units
Output Current	I_o		0	—	16	A
Input Voltage Range	V_{in}	Over I_o range	10.8	—	13.2	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2	%V_o
Temperature Variation	ΔReg_{temp}	–40°C <T_a < +85°C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±6	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±12	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40°C ≤ T_a ≤ +85°C	—	—	±3	%V_o
Efficiency	η	PT5827 (5.0V)	—	93	—	%
		PT5821 (3.3V)	—	90	—	
		PT5822 (2.5V)	—	88	—	
		PT5823 (1.8V)	—	84	—	
		PT5824 (1.5V)	—	82	—	
		PT5825 (1.2V)	—	80	—	
		PT5826 (1.0V)	—	77	—	
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	—	20	—	mVpp
Transient Response	t_{tr}	1A/µs load step, 50% to 100% $I_o$max, Recovery Time	—	50	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	70	—	mV
Over-Current Threshold	I_{TRIP}	Reset, followed by auto-recovery	—	22	—	A
Output Voltage Adjust	V_o adj	with V_o Adjust	—	±10	—	%
		with Margin Up/Down	—	±5	—	
Switching Frequency	f_s	Over V_{in} and I_o ranges	300	350	400	kHz
Inhibit Control (pin 2)		Referenced to GND (pins 9–13)				
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (1)	V
Input Low Voltage	V_{IL}		–0.2	—	0.8	
Input Low Current	I_{IL}	Pin 2 to GND	—	–0.5	—	mA
Standby Input Current	I_{in} standby	Pin 2 to GND	—	2	—	mA
External Input Capacitance	C_{in}		560 (2)	—	—	µF
External Output Capacitance	C_{out}		330 (3)	—	TBD	µF
Operating Temperature Range	T_a	Over V_{in} range	–40	—	+85 (4)	°C
Over-Temperature Shutdown	OTP	Center of case, auto-reset V_o≥3.3V	—	TBD	—	°C
		V_o≤2.5V	—	TBD	—	
Storage Temperature	T_s	—	-40	—	+125	°C
Reliability	MTBF	Per Bellcore TR-332 50% stress, T_a =40°C, ground benign	6.3	—	—	10^6 Hrs
Mechanical Shock		Mil-STD-883D, Method 2002.3 Half Sine, mounted to a fixture	—	TBD	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2, 20-2000 Hz, PCB mounted Vertical	—	TBD (5)	—	G's
		Horizontal				
Weight	—	—	—	20	—	grams
Flammability	—	Materials meet UL 94V-0				

Notes: *(1) The Inhibit control (pin 2) has an internal pull-up to 12V (V_{in}), and if left open-circuit the module will operate when input power is applied. A small low-leakage (<100nA) MOSFET is recommended to control this input. See application notes for more information.*

(2) A 560µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimumm of 1.3Arms of ripple current. For further information, consult the related application note on capacitor selection.

(3) An external 330µF output capacitor is required for proper operation. Distributed load capacitance can be included in this value.

(4) See SOA curves or consult factory for the appropriate derating.

(5) The case pins on the through-hole package types (suffixes N & A) must be soldered. For more information see the applicable package outline drawing.

Pin Descriptions

+Vin: The positive supply voltage input for the module with respect to the common GND.

+Vo: This is the regulated output voltage from the module with respect to the common GND.

GND: The common GND node to which the input, output, and external control signals are referenced.

Sense(–): Provides the regulator with the ability to sense the set-point voltage directly across the load. For optimum output voltage accuracy this pin should always be connected to GND, even for applications that demand a relatively light load.

Sense(+): When used with *Sense(–)*, the regulation circuitry will compensate for voltage drop between the converter and the load. The pin may be left open circuit, but connecting it to $+V_o$ will optimize load regulation..

Inhibit: This is an active low input, which is referenced to GND. Driving this pin to GND disables the module's output voltage. If *Inhibit* is left open-circuit, the output will be active whenever a valid input source is applied.

V_o Adjust: This pin is used to trim the output voltage to a value within a range of up to ±10% of the setpoint. The adjustment requires an external resistor. The resistor is connected from *V_o Adjust*, to either the *Sense(–)* or *Sense(+)*, in order to adjust the output voltage either up or down, respectively.

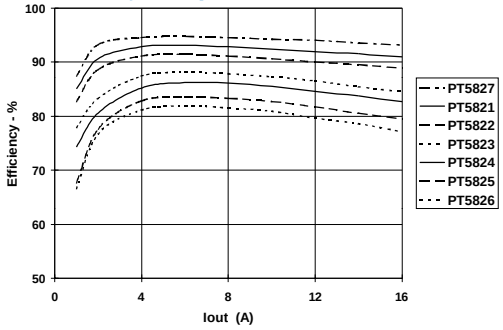
Margin Up: When this pin is connected to *Sense(–)*, the output voltage is increased by 5% of the nominal setpoint. The *Margin Up* and *Margin Down* control inputs provide a convenient method for testing the operation of the load circuit over a ±5% variation in the supply voltage.

Margin Down: When this pin is connected to *Sense(–)*, the output voltage is decreased by approximately 5% from the nominal.

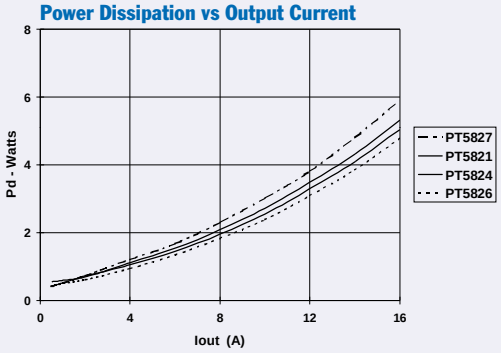
Typical Characteristics

Performance Data; V_{in} =12.0V (See Note A)

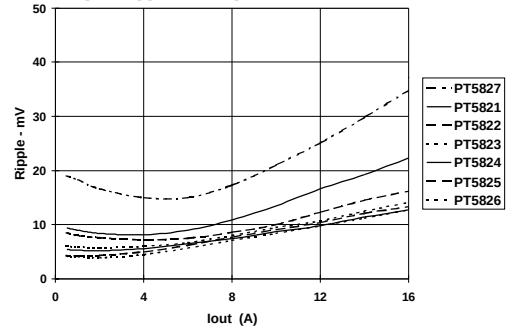
Efficiency vs Output Current



Power Dissipation vs Output Current



Output Ripple vs Output Current

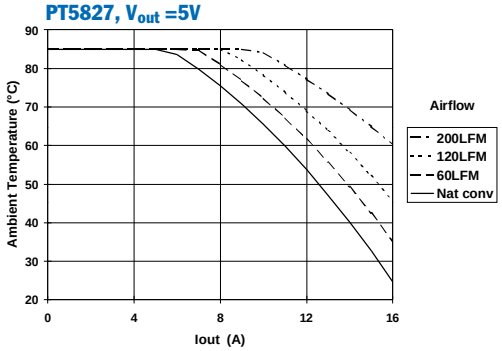


Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

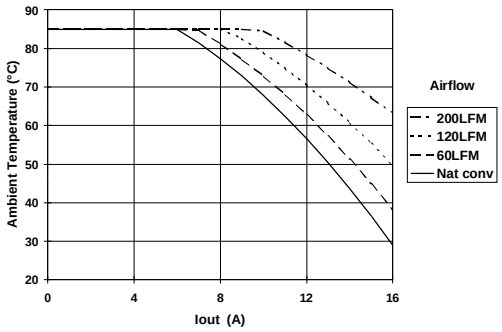
Typical Characteristics

Safe Operating Curves, V_{in} =12V (See Note B)

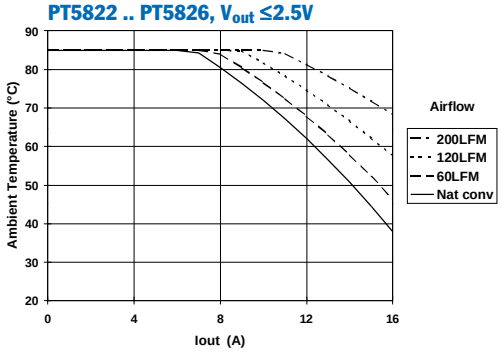
PT5827, V_{out} =5V



PT5821, V_{out} =3.3V



PT5822 .. PT5826, V_{out} ≤2.5V



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Operating Features of the PT5820 Series of Step-Down Integrated Switching Regulators

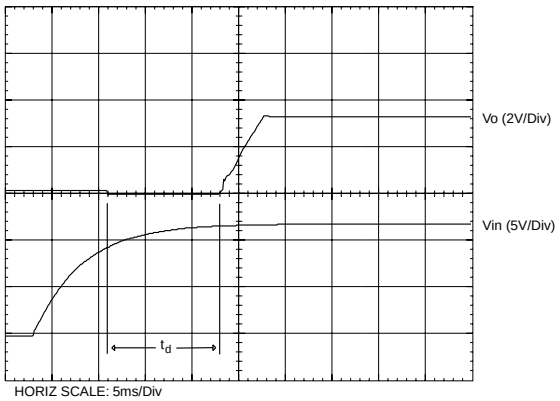
Under-Voltage Lockout (UVLO)

The PT5820 series of non-isolated step-down ISRs incorporate an under-voltage lockout (UVLO) function. The UVLO provides a clean transition during power-up and power-down, allowing the regulator to tolerate a slowly rising input voltage. The UVLO prevents operation of the regulator until the input voltage is at or above above the UVLO threshold. The UVLO threshold is just below the minimum input voltage. Until the input voltage is above this threshold, the status of the *Inhibit* control (pin 2) is overriden, and the module will not produce an output. When the minimum input voltage of 10.8V is applied, the output status is determined by the *Inhibit* control. If the *Inhibit* pin is open-circuit (not grounded), the module will automatically power up. *(Note: Even though the applied input voltage may be above the UVLO threshold, operation to the published specifications requires that the input voltage be at or above the minimum specified. Operation of the module below the minimum input voltage is not recommended).*

Soft-Start Power Up

Following either the application of a valid input source voltage, or the removal of a ground signal to the *Inhibit* control pin (with input power applied), the regulator will initiate a soft-start power up. The soft start slows the rate at which the output voltage rises, and also introduces a short time delay, t_d (approx. 10–15ms). Figure 1-1 shows the power-up characteristic of a PT5821 (3.3V). The delay time, t_d, is measured from the point at which the input voltage rises above the UVLO threshold to when the output voltage starts to rise. During this period the output of the regulator will assert a low impedance to ground. This has the effect of discharging any residual voltage across the output capacitors, and will crowbar any voltage supplied from external sources.

Figure 1-1; Soft-Start Power Up



Over-Current Protection

To protect against load faults, the PT5820 series incorporates output over-current protection. Applying a load that exceeds the regulator's over-current threshold (see data sheet specifications) will cause the regulated output to shut down. Following shutdown the ISR will periodically attempt to recover by initiating a soft-start power-up. This is often described as a "hiccup" mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the converter automatically recovers and returns to normal operation.

Thermal Shutdown

The PT5820 series ISRs incorporate thermal shutdown, which protects the module's internal circuitry against excessively high temperatures. A rise in the temperature of the internal components may be the result of a drop in airflow, or a high ambient temperature. If the module's internal temperature exceeds the shutdown threshold (see data sheet specifications), the regulator output is disabled and the output voltage is reduced to zero. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10°C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Output Voltage Adjustment

The PT5820 series ISRs offer OEMs two alternative methods of output voltage adjustment. The *Margin Up* and *Margin Down* control inputs provide a convenient method of adjusting the output voltage by a nominal ±5% of the factory setpoint voltage. For a more permanent and precise method of adjustment, the V_o *Adjust* control allows the output to be adjusted in any increment by up to ±10%. For more information on this subject, consult the related application note on output voltage adjustment.

Using the Inhibit Control of the PT5820 Series of Step-Down Regulators

For applications requiring output voltage On/Off control, the PT5820 series of ISRs incorporate an inhibit function. This function can be used wherever there is a requirement for the output voltage from the ISR to be turned off. The On/Off function is provided by the *Inhibit* control (pin 2).

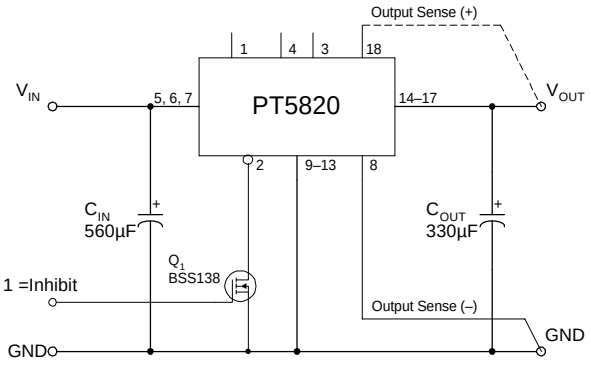
The ISR functions normally with pin 2 open-circuit, providing a regulated output whenever a valid source voltage is applied between V_{in} (pins 5–7) and *GND* (pins 11–13). When a low-level ground signal is applied to pin 2, the regulator output is turned off.

Figure 2-1 shows the typical application of the *Inhibit* function. Note the discrete transistor (Q_1). The *Inhibit* control has its own internal pull-up to $+V_{in}$ potential. An open-collector or open-drain device is required to control this input [1]. The voltage thresholds are given in Table 2-1.

Table 2-1; Inhibit Control Requirements

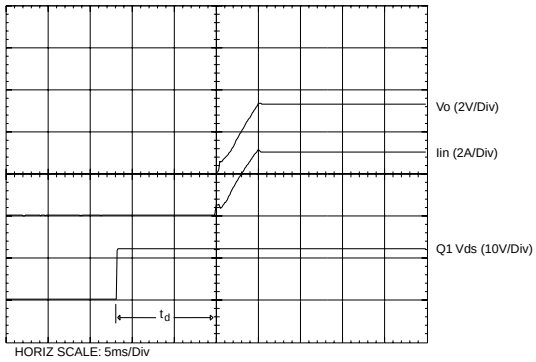
Parameter	Min	Typ	Max
Enable (V_{IH})	V_{in} – 0.5V	—	Open
Disable (V_{IL})	–0.2V	—	+0.8V
I_{IL}	—	–0.5 mA	—

Figure 2-1



Turn-On Time: In the circuit of Figure 2-1, turning Q_1 on applies a low-voltage to the *Inhibit* control (pin 2) and disables the output of the regulator [2]. If Q_1 is then turned off, the ISR executes a soft-start power up. Power up consists of a short delay period, t_d (approx. 10-15msec) [3], followed by a period in which the output voltage rises to its full regulation voltage. The module produces a regulated output voltage within 20msec. Figure 2-2 shows the typical rise in both the output voltage and input current for a PT5821 (3.3V), following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 12VDC input voltage, and 10-A load.

Figure 2-2



Notes:

1. Use an open-collector device with a breakdown voltage of at least 15V (preferably a discrete transistor) for the *Inhibit* input. A pull-up resistor is not necessary. To disable the output voltage the control pin should be pulled low to less than +0.8VDC.
2. When a ground signal is applied to the *Inhibit* control (pin 2) the module output is turned off. The output voltage decays to zero as the load impedance discharges the output capacitors.
3. During the period 't_d' in Figure 2-2 the module will assert a low impedance to ground. This will discharge any residual voltage across the output capacitors, and will crowbar any voltage supplied from external sources.

Adjusting the Output Voltage of the PT5820 Series of Step-Down ISRs

Using Margin Up/ Margin Down

The *Margin Up* (pin 4) and *Margin Down* (pin 3) control inputs allow the output voltage to be easily adjusted by approximately ±5% of the the set-point voltage. These control inputs provide a convenient method for applying a momentary adjustment to test a load circuit's supply voltage margins. To activate, simply connect the appropriate control input to the *Sense(–)* (pin 8), or the local starpoint ground. Either a logic level MOSFET or a p-channel JFET is recommended for this application.

Using the 'V_o Adjust' Control

For a more permanent and precise adjustment, use the *Vo Adjust* control (pin 1). The *V_o Adjust* control allows adjustment in any increment by up to ±10% of the set-point. The adjustment method requires the addition of a single external resistor. Table 3-1 gives the allowable adjustment range for each model of the series as V_a (min) and V_a (max). The value of the external resistor can either be calculated using the formulas given below, or simply selected from the range of values provided in Table 3-2. Refer to Figure 3-1 for the placement of the required resistor. Use the resistor R_1 to adjust up, and the resistor (R_2) to down.

Adjust Up: An increase in the output voltage is obtained by adding a resistor R_1, between *V_o Adjust* (pin 1) and *Sense(–)* (pin 8). See Figure 3-1.

Adjust Down: Add a resistor (R_2), between *V_o Adjust* (pin 1) and *Sense(+)* (pin 18). See Figure 3-1.

Notes:

1. Use a 1% (or better) tolerance resistor in either the R_1 or (R_2) location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from *V_o Adjust* to either *GND* or *V_{out}*. Any capacitance added to the *V_o Adjust* pin will affect the stability of the ISR.
3. If the remote sense feature is not being used, the adjust resistor (R_2) can be connected to *V_{out}*, (pins 14-17) instead of *Sense (+)*.

V_o Adjust Resistor Calculations

The values of R_1 [adjust up] and (R_2) [adjust down] can also be calculated using the following formulas. Again, use Figure 3-1for the placement of the required resistor; either R_1 or (R_2) as appropriate.

$$R_1 = \frac{V_r \cdot R_o}{V_a - V_o} - 24.9 \quad k\Omega$$

$$(R_2) = \frac{R_o (V_a - V_r)}{V_o - V_a} - 24.9 \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
V_r = The reference voltage in Table 3-1
R_o = The resistance constant in Table 3-1

Figure 3-1; V_o Adjust Resistor Placement

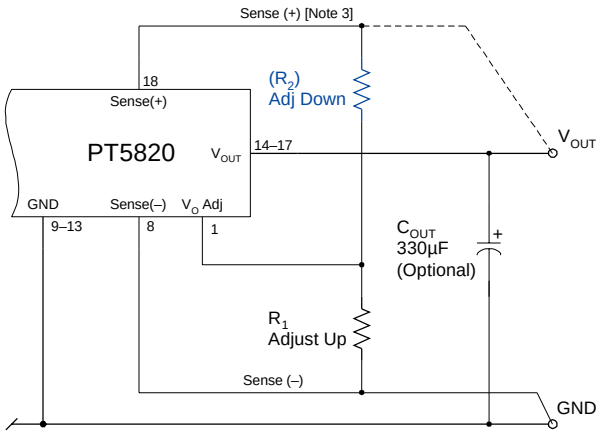


Table 3-1

ISR OUTPUT VOLTAGE ADJUSTMENT RANGE AND FORMULA PARAMETERS

Series Pt. No.	PT5827	PT5821	PT5822	PT5823	PT5824	PT5825	PT5826
V_o (nom)	5.0V	3.3V	2.5V	1.8V	1.5V	1.2V	1.0V
V_a (min)	4.0V	2.6V	2.0V	1.52V	1.31V	1.1V	0.94V
V_a (max)	5.5V	3.63V	2.8V	2.1V	1.82V	1.52V	1.32V
V_r	1.27V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
R_o (kΩ)	10.0	10.2	10.7	10.2	9.76	10.0	10.2

Table 3-2

ISR ADJUSTMENT RESISTOR VALUES

Series Pt. No.	PT5827	PT5821
V_o (nom)	5.0V	3.3V
V_a (req.d)		
5.50	0.5kΩ	
5.40	6.9kΩ	
5.30	17.4kΩ	
5.20	38.6kΩ	
5.10	102.0kΩ	
5.00		
4.90	(338.0)kΩ	
4.80	(152.0)kΩ	
4.70	(89.4)kΩ	
4.60	(58.3)kΩ	
4.50	(39.7)kΩ	
4.40	(27.3)kΩ	
4.30	(18.4)kΩ	
4.20	(11.7)kΩ	
4.10	(6.5)kΩ	
4.00	(2.4)kΩ	
•		
3.60		2.3kΩ
3.55		7.7kΩ
3.50		15.9kΩ
3.45		29.5kΩ
3.40		56.7kΩ
3.35		138.0kΩ
3.30		
3.25		(475.0)kΩ
3.20		(220.0)kΩ
3.15		(135.0)kΩ
3.10		(92.4)kΩ
3.05		(66.9)kΩ
3.00		(49.9)kΩ
2.95		(37.5)kΩ
2.90		(28.6)kΩ
2.85		(21.6)kΩ
2.80		(15.9)kΩ
2.75		(11.3)kΩ
2.70		(7.4)kΩ
2.65		(4.1)kΩ
2.60		(1.3)kΩ

	PT5822	PT5823	PT5824	PT5825	PT5826
	2.5V	1.8V	1.5V	1.2V	1.0V
V_a (req.d)					
2.800	3.6KΩ				
2.750	9.3KΩ				
2.700	17.9KΩ				
2.650	32.2KΩ				
2.600	60.7KΩ				
2.550	146.0KΩ				
2.500					
2.450	(321.0)kΩ				
2.400	(146.0)kΩ				
2.350	(85.7)kΩ				
2.300	(55.3)kΩ				
2.250	(37.2)kΩ				
2.200	(25.0)kΩ				
2.150	(16.4)kΩ				
2.100	(9.9)kΩ	2.3kΩ			
2.050	(4.8)kΩ	7.7kΩ			
2.000	(0.8)kΩ	15.9kΩ			
1.950		29.5kΩ			
1.900		56.7kΩ			
1.850		138.0kΩ			
1.800			1.1kΩ		
1.750		(169.0)kΩ	6.3kΩ		
1.700		(66.9)kΩ	14.1kΩ		
1.650		(32.9)kΩ	27.2kΩ		
1.600		(15.9)kΩ	53.2kΩ		
1.550		(5.7)kΩ	131.0kΩ		
1.500				1.8kΩ	
1.475			(239.0)kΩ	4.2kΩ	
1.450			(102.0)kΩ	7.1kΩ	
1.425			(56.4)kΩ	10.7kΩ	
1.400			(33.7)kΩ	15.1kΩ	
1.375			(20.0)kΩ	20.8kΩ	
1.350			(10.9)kΩ	28.4kΩ	
1.325			(4.4)kΩ	39.1kΩ	
1.300				55.1kΩ	2.3kΩ
1.275				81.8kΩ	4.8kΩ
1.250				135.0kΩ	7.7kΩ
1.225				295.0kΩ	11.4kΩ
1.200					15.9kΩ
1.175				(125.0)kΩ	21.7kΩ
1.150				(45.1)kΩ	29.5kΩ
1.125				(18.4)kΩ	40.4kΩ
1.100				(5.1)kΩ	56.7kΩ
1.075					83.9kΩ
1.050					138.0kΩ
1.025					302.0KΩ
1.000					
0.975					(46.5)kΩ
0.950					(5.7)kΩ

R_1 = Black R_2 = (Blue)

Capacitor Recommendations for the PT5820 Regulator Series

Input Capacitor:

The recommended input capacitance is determined by 1.3 ampere minimum ripple current rating and 560µF minimum capacitance.

Ripple current and <100mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of twice the maximum DC voltage + AC ripple. This is necessary to insure reliability for input voltage bus applications.

Output Capacitors:

The maximum allowable ESR of the output capacitor is 150mΩ. Electrolytic capacitors have marginal ripple performance at frequencies greater than 400kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions. Preferred low ESR type capacitor part numbers are identified in Table 4-1.

Tantalum Capacitors

Tantalum type capacitors can be used for the output but only the AVX TPS, Sprague 593D/594/595 or Kemet T495/T510 series. These capacitors are recommended over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation, and lower ripple current capability. The TAJ series is less reliable than the AVX TPS series when determining power dissipation capability. Tantalum or Oscon® types are recommended for applications where ambient temperatures fall below 0°C.

Capacitor Table

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (Equivalent Series Resistance at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 4-1: Input/Output Capacitors

Capacitor Vendor/ Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value(µF)	(ESR) Equivalent Series Resistance	105°C Maximum Ripple Current(Irms)	Physical Size(mm)	Input Bus	Output Bus	Vendor Part Number
Panasonic FC (Radial)	35V 25V 25V	680 330 1000	0.043Ω 0.090Ω 0.038Ω	1655mA 755mA 1690mA	12.5×20 10×12.5 16×15	1 N/R (1) 1	1 1 1	EEUFC1V681 EEUFC1E331 EEUFC1E102S
FC/FK (Surface Mtg)	50V 35V 50V	1000 680 1000	0073Ω 0.060Ω 0.073Ω	1610mA 1100mA 1610mA	16×16.5 12.5×13.5 16×16.5	1 1 (2) 1	1 1 1	EEVFK1H102M EEVFK1V681Q **(Vo<2.6V)** EEVFK1H102M
United Chemi-con LXZ/LXV Series MVY (Surface Mtg)	35V 35V 25V	680 680 330	0.037Ω 0.068Ω 0.15Ω	1660mA 1050mA 670mA	12.5×20 10×16 10×10.3	1 1 (2) N/R (1)	1 1 1	LXZ35VB681M12X20LL LXV35VB102M16X20LL**(Vo<2.6V)** MVY25VC331M10X10TP
Nichicon PL Series PM Series	35V 25V 25V	680 1270 820	0.042Ω 0.055Ω 0.049Ω	1540mA 1270mA 1340mA	18×15 16×15 16×15	1 1 (2) 1	1 1 1	UPL1V681MHH6 UPL1E122MHH6 **(Vo<2.6V)** UPM1E821MHH6
Os-con: SS SVP (surface Mount) Old SV Series	 10V 16V	 330 330	 0.025Ω 0.016Ω	 3500mA 4700mA	 10×10.5 11×12	 N/R (1) 2	 1 1	 10SS330M **(V_o<5.1V)** 16SVP330M
AVX Tantalum TPS (Surface Mtgt)	10V 10V	330 330	0.1Ω 0.06Ω	>2500mA >3000mA	7.3L ×5.7W ×4.1H	N/R (1) N/R (1)	1 1	TPSE337M010R0100 **(V_o<5.1V)** TPSV337M010R0060 **(V_o<5.1V)**
Kemet Tantalum T520/T495 Series (Surface Mount)	10V 6.3V	330 220	0.040Ω 0.07Ω	1600mA >2000mA	4.3W ×7.3L ×4.0H	N/R (1) N/R (1)	1 1	520X337M010AS T495X227M0100AS
Sprague Tantalum 594D Series (Surface Mount)	10V	330	0.045Ω	2360mA	7.2L ×6W ×4.1H	N/R (1)	1	594D337X0010R2T

(1) N/R –Not recommended. The voltage rating does not meet the minimum operating limits.
(2) Recommended Input capacitor when V_o<2.6V; lower RMS mA required .

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