LP2952/LP2952A/LP2953/LP2953A Adjustable Micropower Low-Dropout Voltage Regulators

Check for Samples: LP2952-N, LP2952A, LP2953, LP2953A

FEATURES

- **Output voltage adjusts from 1.23V to 29V**
- **Guaranteed 250 mA output current**
- **Extremely low quiescent current**
- **Low dropout voltage**
- **Extremely tight line and load regulation**
- **Very low temperature coefficient**
- **Current and thermal limiting**
- **Reverse battery protection**
- **50 mA (typical) output pulldown crowbar**
- **5V and 3.3V versions available**

APPLICATIONS

- **High-efficiency linear regulator**
- **Regulator with under-voltage shutdown**
- **Low dropout battery-powered regulator**
- **Snap-ON/Snap-OFF regulator**

LP2953 VERSIONS ONLY

- **Auxiliary comparator included with CMOS/TTL-compatible output levels. Can be used for fault detection, low input line detection, etc.**

DESCRIPTION

The LP2952 and LP2953 are micropower voltage regulators with very low quiescent current (130 µA typical at 1 mA load) and very low dropout voltage (typ. 60 mV at light load and 470 mV at 250 mA load current). They are ideally suited for battery-powered systems. Furthermore, the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2952 and LP2953 retain all the desirable characteristics of the LP2951, but offer increased output current, additional features, and an improved shutdown function.

The internal crowbar pulls the output down quickly when the shutdown is activated.

The error flag goes low if the output voltage drops out of regulation.

Reverse battery protection is provided.

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good line and load regulation.

The parts are available in PDIP, CDIP and surface mount packages.

Block Diagrams

LP2952

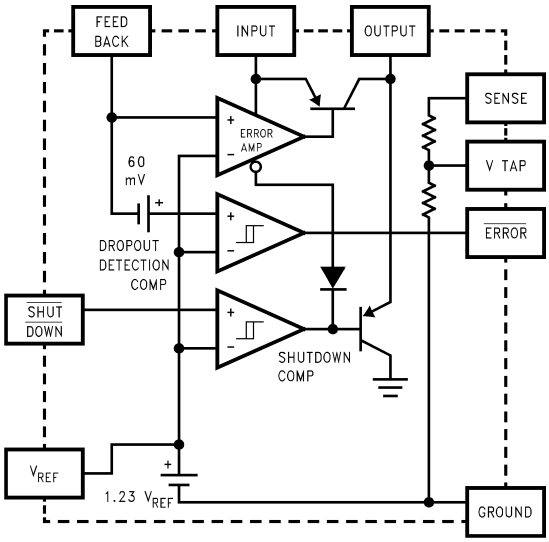


Figure 1.

LP2953

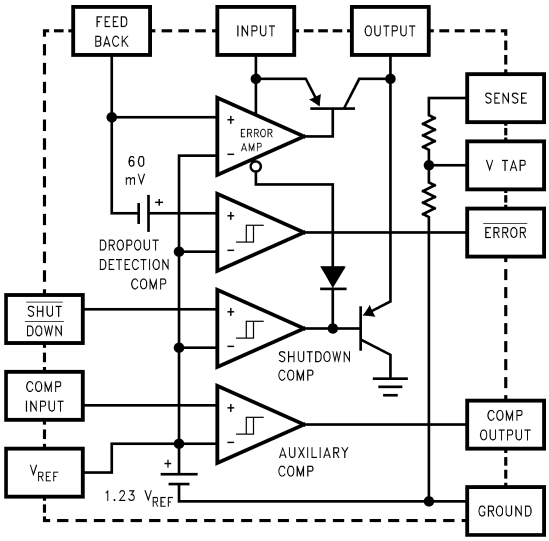


Figure 2.

Pinout Drawings

LP2952
14-Pin PDIP/NFF

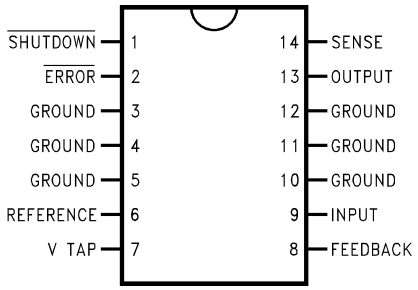


Figure 3.

LP2953
16-Pin PDIP/NBG

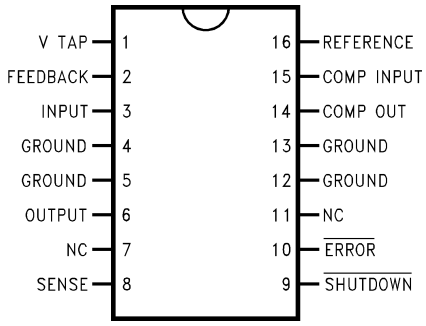


Figure 4.

LP2952
16-Pin SOIC/D

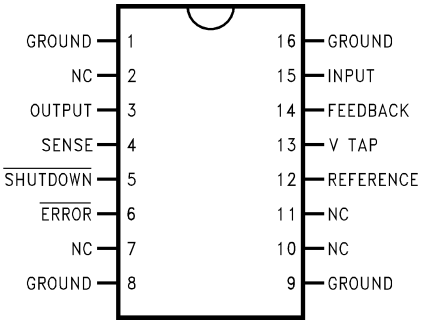


Figure 5.

LP2953
16-Pin SOIC/D

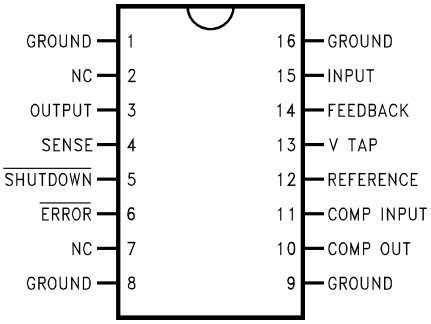


Figure 6.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Operating Temperature Range LP2952I, LP2953I, LP2952AI, LP2953AI, LP2952I-3.3, LP2953I-3.3, LP2952AI-3.3, LP2953AI-3.3	−40°C ≤ T_J ≤ +125°C
LP2953AM	−55°C ≤ T_A ≤ +125°C
Lead Temp. (Soldering, 5 seconds)	260°C
Power Dissipation (2)	Internally Limited
Maximum Junction Temperature LP2952I, LP2953I, LP2952AI, LP2953AI, LP2952I-3.3, LP2953I-3.3, LP2952AI-3.3, LP2953AI-3.3	+125°C
LP2953AM	+150°C
Input Supply Voltage	−20V to +30V
Feedback Input Voltage (3)	−0.3V to +5V
Comparator Input Voltage (4)	−0.3V to +30V
Shutdown Input Voltage (4)	−0.3V to +30V
Comparator Output Voltage (4)	−0.3V to +30V
ESD Rating (5)	2 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using the equation for P(MAX), $P_{(MAX)} = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$. .Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See Application Hints for additional information on heatsinking and thermal resistance.

(3) When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.

(4) May exceed the input supply voltage.

(5) Human body model, 200 pF discharged through 1.5 kΩ.

ELECTRICAL CHARACTERISTICS: 3.3V VERSIONS

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7 µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin.

Symbol	Parameter	Conditions	Typical	LP2952AI-3.3, LP2953AI-3.3		LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
V_O	Output Voltage		3.3	3.284	3.317	3.267	3.333	V
				3.260	**3.340**	**3.234**	**3.366**	
		1 mA ≤ I_L ≤ 250 mA	3.3	**3.254**	**3.346**	**3.221**	**3.379**	

ELECTRICAL CHARACTERISTICS: 5V VERSIONS

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin.

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2953AM		LP2952I, LP2953I		Units
				Min	Max	Min	Max	
V_O	Output Voltage		5.0	4.975	5.025	4.950	5.050	V
				4.940	**5.060**	**4.900**	**5.100**	
		1 mA ≤ I_L ≤ 250 mA	5.0	**4.930**	**5.070**	**4.880**	**5.120**	

ALL VOLTAGE OPTIONS ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7 µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin.

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3, LP2953AM (1)		LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
REGULATOR								
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temp. Coefficient	(2)	**20**		**100**		**150**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Output Voltage Line Regulation	$V_{IN} = V_O(NOM) + 1V$ to 30V	0.03		0.1		0.2	%
					0.2		**0.4**	
$\frac{\Delta V_O}{V_O}$	Output Voltage Load Regulation (3)	I_L = 1 mA to 250 mA	0.04		0.16		0.20	%
		I_L = 0.1 mA to 1 mA			**0.20**		**0.30**	
$V_{IN}–V_O$	Dropout Voltage (4)	I_L = 1 mA	60		100		100	mV
					150		**150**	
		I_L = 50 mA	240		300		300	
					420		**420**	
		I_L = 100 mA	310		400		400	
					520		**520**	
		I_L = 250 mA	470		600		600	
					800		**800**	
I_{GND}	Ground Pin Current (5)	I_L = 1 mA	130		170		170	µA
					200		**200**	
		I_L = 50 mA	1.1		2		2	mA
					2.5		**2.5**	
		I_L = 100 mA	4.5		6		6	
					8		**8**	
		I_L = 250 mA	21		28		28	
					33		**33**	
I_{GND}	Ground Pin Current at Dropout	$V_{IN} = V_O(NOM) - 0.5V$	165		210		210	µA
		I_L = 100 µA			**240**		**240**	
I_{GND}	Ground Pin Current at Shutdown (5)	$V_{SHUTDOWN} \leq 1.1V$	105		140		140	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0	380		500		500	mA
					530		**530**	
$\frac{\Delta V_O}{\Delta Pd}$	Thermal Regulation	(6)	0.05		0.2		0.2	%/W

(1) Drive $\overline{\text{Shutdown}}$ pin with TTL or CMOS-low level to shut regulator OFF, high level to turn regulator ON.
(2) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(3) Load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the range of 100 µA to 1 mA and one for the 1 mA to 250 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
(4) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential. At very low values of programmed output voltage, the input voltage minimum of 2V (2.3V over temperature) must be observed.
(5) Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).
(6) Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at $V_{IN} = V_O(NOM)+15V$ (3W pulse) for T = 10 ms.

ALL VOLTAGE OPTIONS ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7 µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin.

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3, LP2953AM (1)		LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
e_n	Output Noise Voltage (10 Hz to 100 kHz) I_L = 100 mA	C_L = 4.7 µF	400					µV RMS
		C_L = 33 µF	260					
		C_L = 33 µF (7)	80					
V_{REF}	Reference Voltage	(8)	1.230	1.215	1.245	1.205	1.255	V
				1.205	**1.255**	**1.190**	**1.270**	
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to $V_O(NOM)$ + 1V	0.03		0.1		0.2	%
		$V_{IN} = V_O(NOM) + 1V$ to 30V (9)			**0.2**		**0.4**	
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Load Regulation	I_{REF} = 0 to 200 µA	0.25		0.4		0.8	%
					0.6		**1.0**	
$\frac{\Delta V_{REF}}{\Delta T}$	Reference Voltage Temp. Coefficient	(2)	**20**					ppm/°C
I_B(FB)	Feedback Pin Bias Current		20		40		40	nA
					60		**60**	
I_O(SINK)	Output "OFF" Pulldown Current	(10)		30		30		mA
				20		**20**		
DROPOUT DETECTION COMPARATOR								
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V	0.01		1		1	µA
					2		**2**	
V_{OL}	Output "LOW" Voltage	$V_{IN} = V_O(NOM) - 0.5V$, I_O(COMP) = 400 µA	150		250		250	mV
					400		**400**	
V_{THR} (MAX)	Upper Threshold Voltage	(11)	−60	−80	−35	−80	−35	mV
				−95	**−25**	**−95**	**−25**	
V_{THR} (MIN)	Lower Threshold Voltage	(12)	−85	−110	−55	−110	−55	mV
				−160	**−40**	**−160**	**−40**	
HYST	Hysteresis	(12)	15					mV
$\overline{\text{SHUTDOWN}}$ INPUT (13)								
V_{OS}	Input Offset	(Referred to V_{REF})	±3	−7.5	7.5	−7.5	7.5	mV
	Voltage			**−10**	**10**	**−10**	**10**	
HYST	Hysteresis		6					mV

(7) Connect a 0.1 µF capacitor from the output to the feedback pin.
(8) $V_{REF} \le V_{OUT} \le (V_{IN} - 1V)$, $2.3V \le V_{IN} \le 30V$, 100 µA ≤ I_L ≤ 250 mA.
(9) Two separate tests are performed, one covering $2.5V \le V_{IN} \le V_O(NOM)+1V$ and the other test for $V_O(NOM)+1V \le V_{IN} \le 30V$.
(10) $V_{SHUTDOWN} \le 1.1V$, $V_{OUT} = V_O(NOM)$.
(11) Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at$V_{IN} = V_O(NOM) + 1V$. To express these thresholds in terms of output voltage change, multiply by the Error amplifier gain, which is V_{OUT}/V_{REF} = (R1 + R2)/R2(refer to Figure 37).
(12) Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at$V_{IN} = V_O(NOM) + 1V$. To express these thresholds in terms of output voltage change, multiply by the Error amplifier gain, which is V_{OUT}/V_{REF} = (R1 + R2)/R2(refer to Figure 37).
(13) Human body model, 200 pF discharged through 1.5 kΩ.

ALL VOLTAGE OPTIONS ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7 µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin.

Symbol	Parameter	Conditions		Typical	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3, LP2953AM (1)		LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3		Units
					Min	Max	Min	Max	
I_B	Input Bias	V_{IN}(S/D) = 0V to 5V		10	−30	30	−30 **−50**	−30 **50**	nA
	Current				**−50**	**50**			
			LP2953AM	10	−30	30			
					−75	**75**			
AUXILIARY COMPARATOR (LP2953 Only)									
V_{OS}	Input Offset Voltage	(Referred to V_{REF})		±3	−7.5	7.5	−7.5 **−10**	7.5 **10**	mV
					−10	**10**			
			LP2953AM	±3	−7.5	7.5			
					−12	**12**			
HYST	Hysteresis			6					mV
I_B	Input Bias Current	V_{IN}(COMP) = 0V to 5V		10	−30	30	−30 **−50**	30 **50**	nA
					−50	**50**			
			LP2953AM	10	−30	30			
					−75	**75**			
I_{OH}	Output “HIGH” Leakage	V_{OH} = 30V		0.01		1		1 **2**	µA
		V_{IN}(COMP) = 1.3V				**2**			
			LP2953AM	0.01		1			
						2.2			
V_{OL}	Output “LOW” Voltage	V_{IN}(COMP) = 1.1V		150		250		250 **400**	mV
		I_O(COMP) = 400 µA				**400**			
			LP2953AM	150		250			
						420			

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V.

Quiescent Current

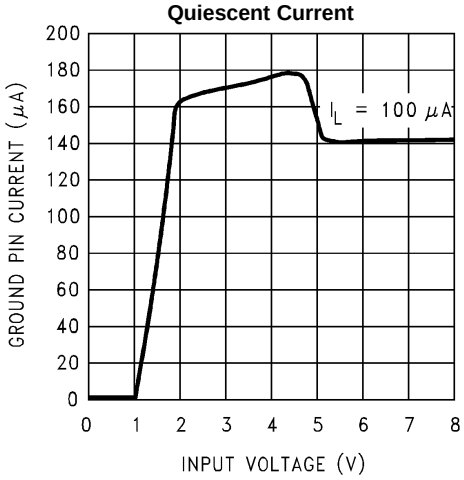


Figure 7.

Quiescent Current

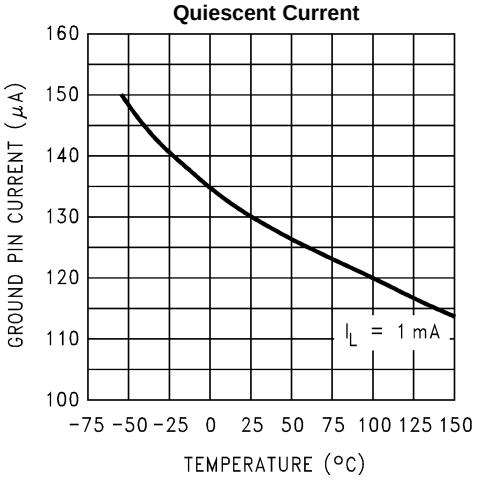


Figure 8.

Ground Pin Current vs Load

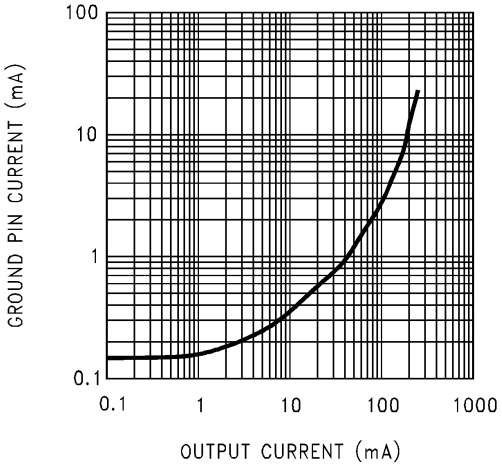


Figure 9.

Ground Pin Current

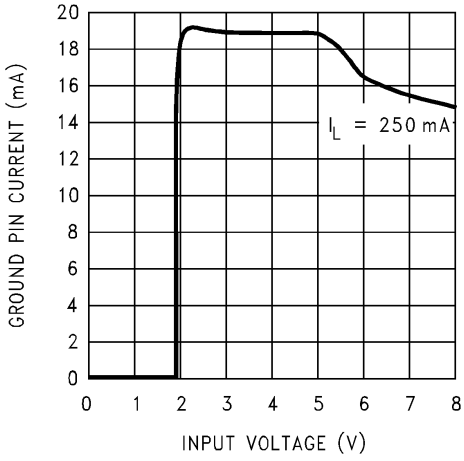


Figure 10.

Ground Pin Current

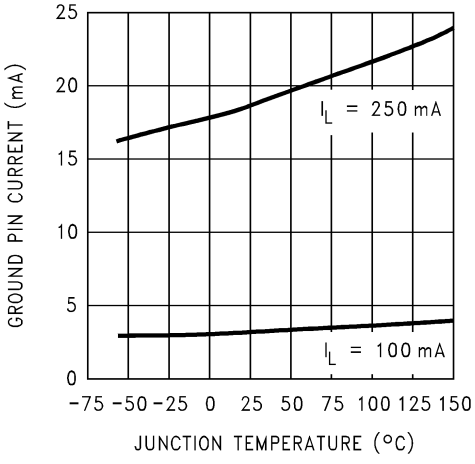


Figure 11.

Output Noise Voltage

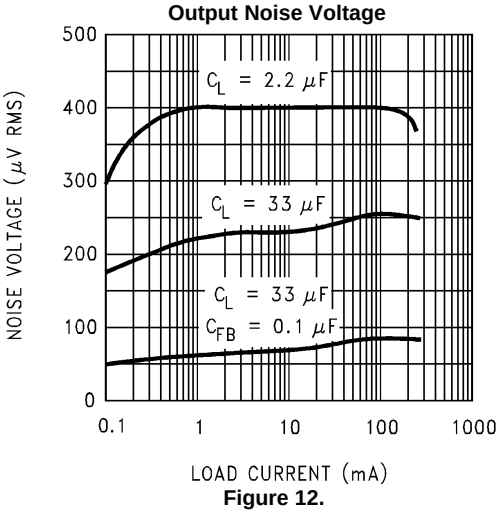


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V.

Ripple Rejection

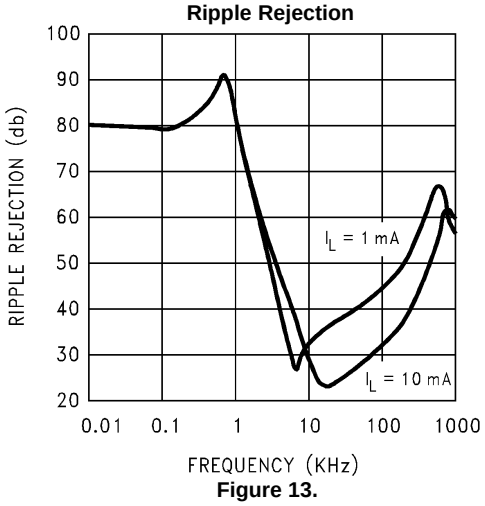


Figure 13.

Ripple Rejection

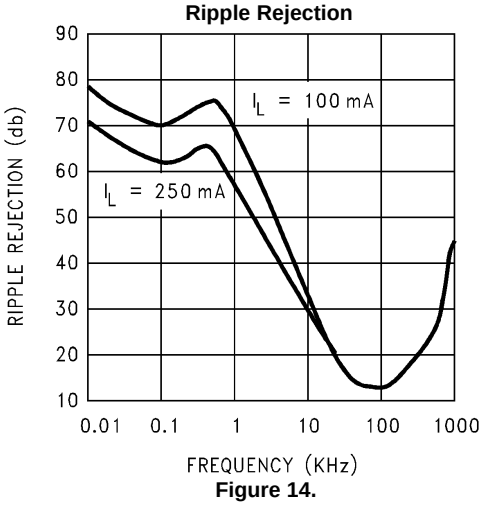


Figure 14.

Ripple Rejection

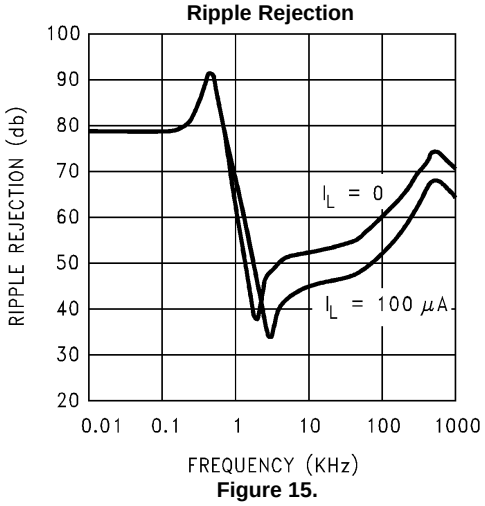


Figure 15.

Line Transient Response

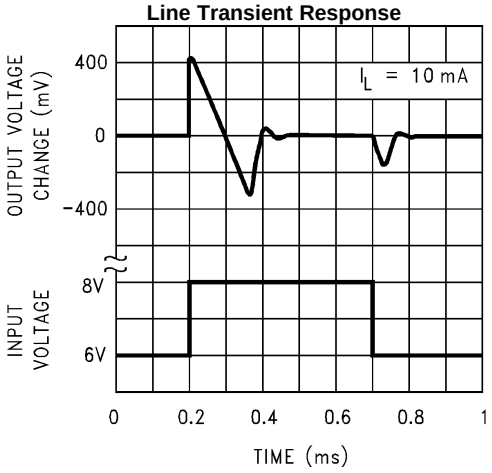


Figure 16.

Line Transient Response

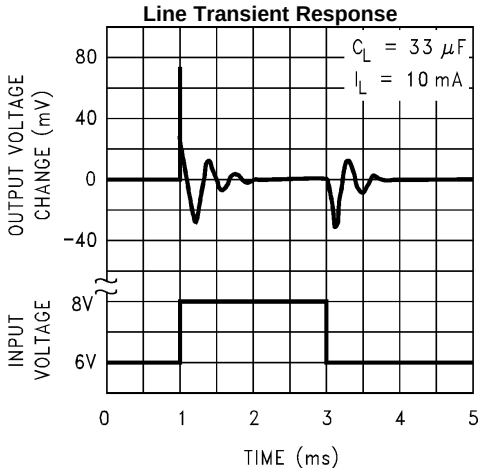


Figure 17.

Output Impedance

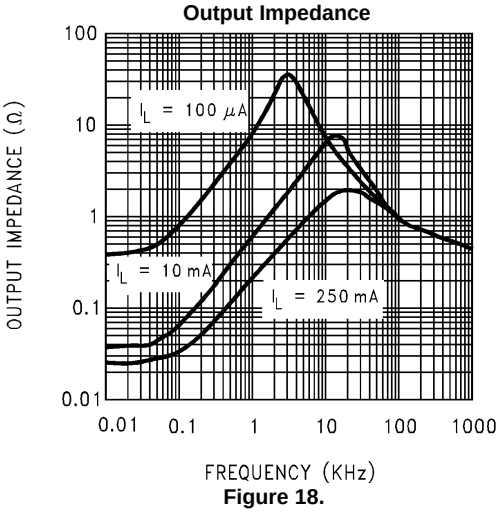


Figure 18.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V.

Load Transient Response

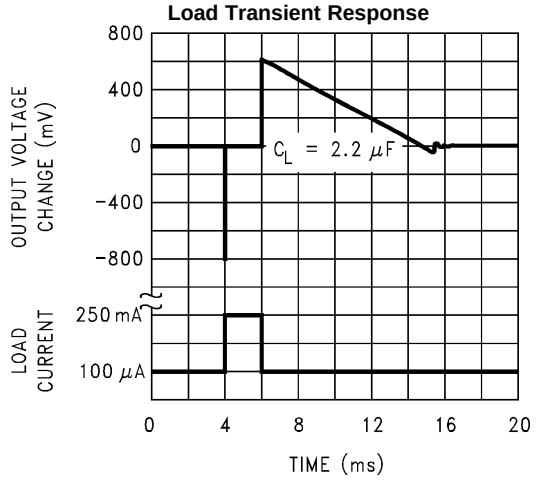


Figure 19.

Load Transient Response

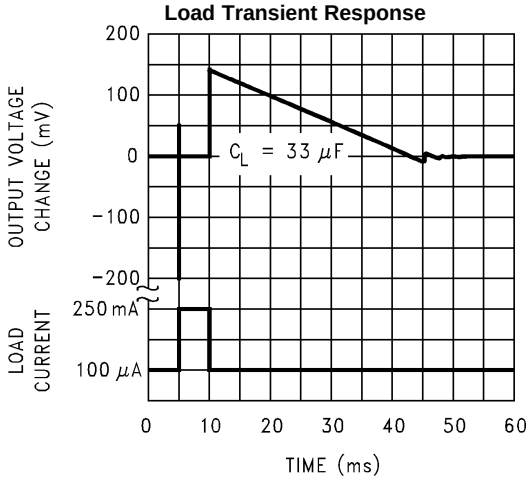


Figure 20.

Dropout Characteristics

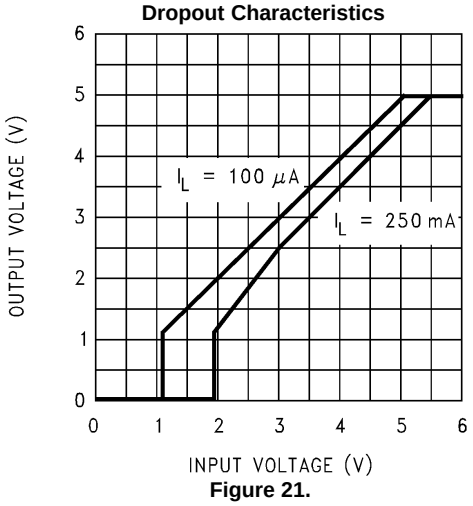


Figure 21.

Enable Transient

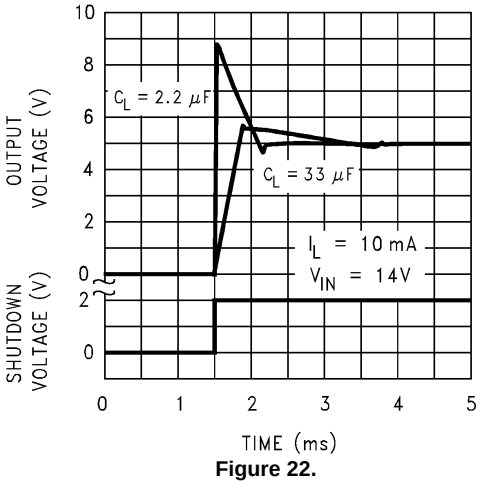


Figure 22.

Enable Transient

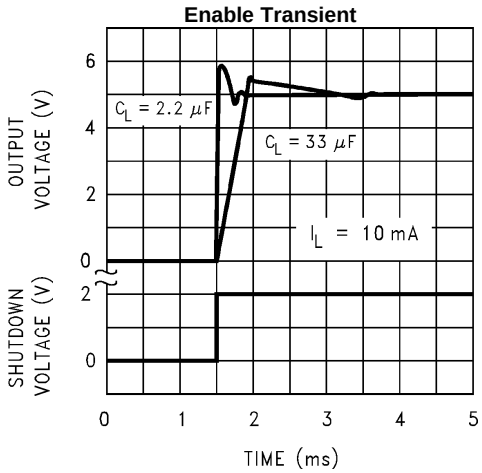


Figure 23.

Short-Circuit Output Current and Maximum Output Current

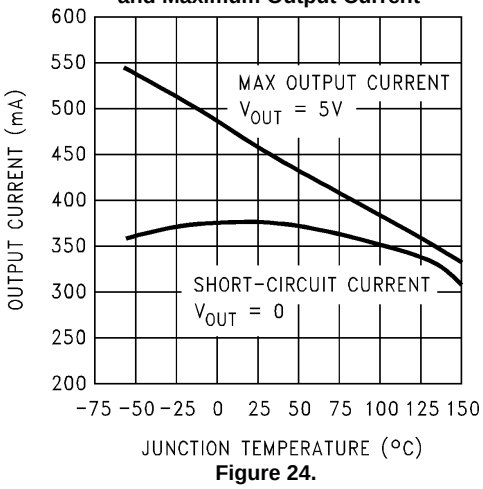


Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V.

Feedback Bias Current

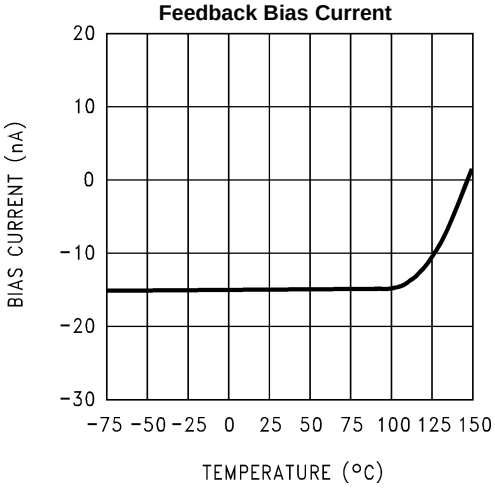


Figure 25.

Feedback Pin Current

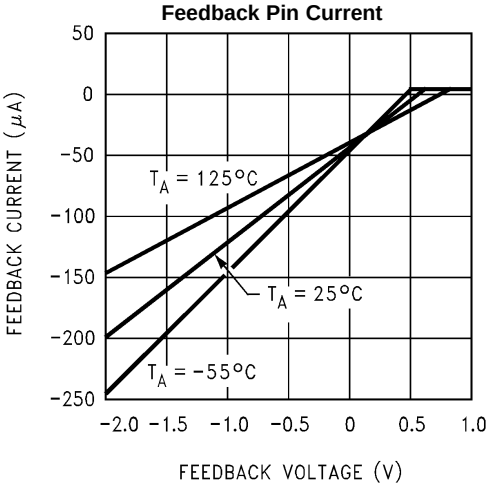


Figure 26.

Error Output

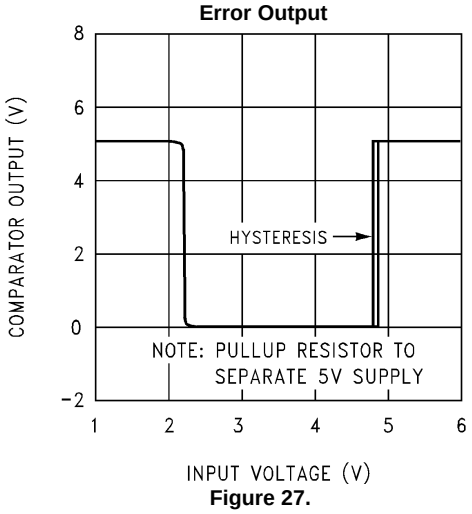


Figure 27.

Comparator Sink Current

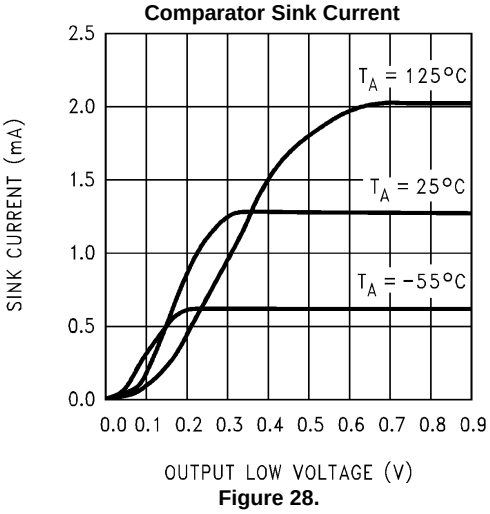


Figure 28.

Divider Resistance

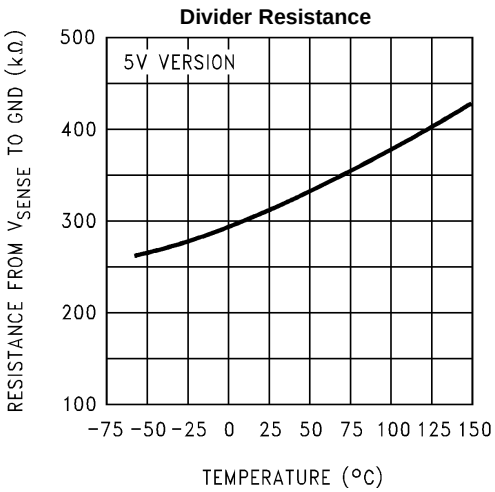


Figure 29.

Dropout Detection Comparator Threshold Voltages

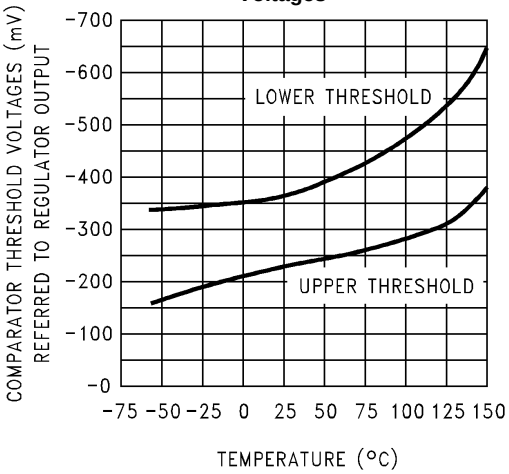


Figure 30.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V.

Thermal Regulation

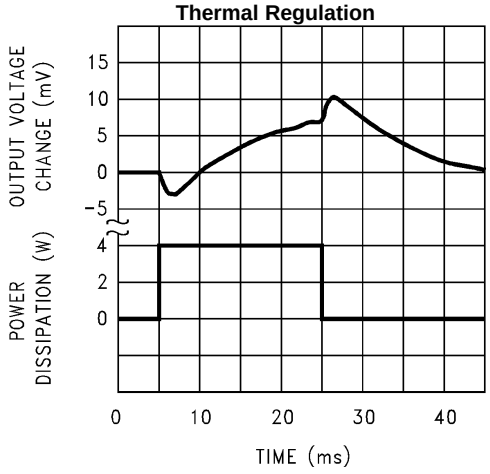


Figure 31.

Minimum Operating Voltage

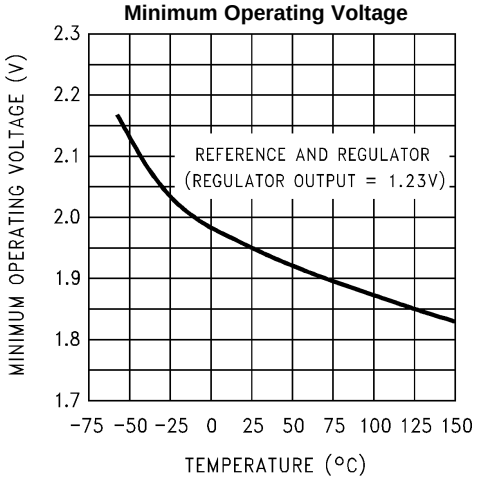


Figure 32.

Dropout Voltage

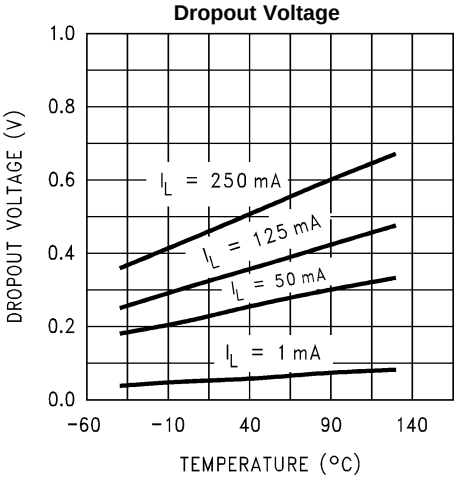
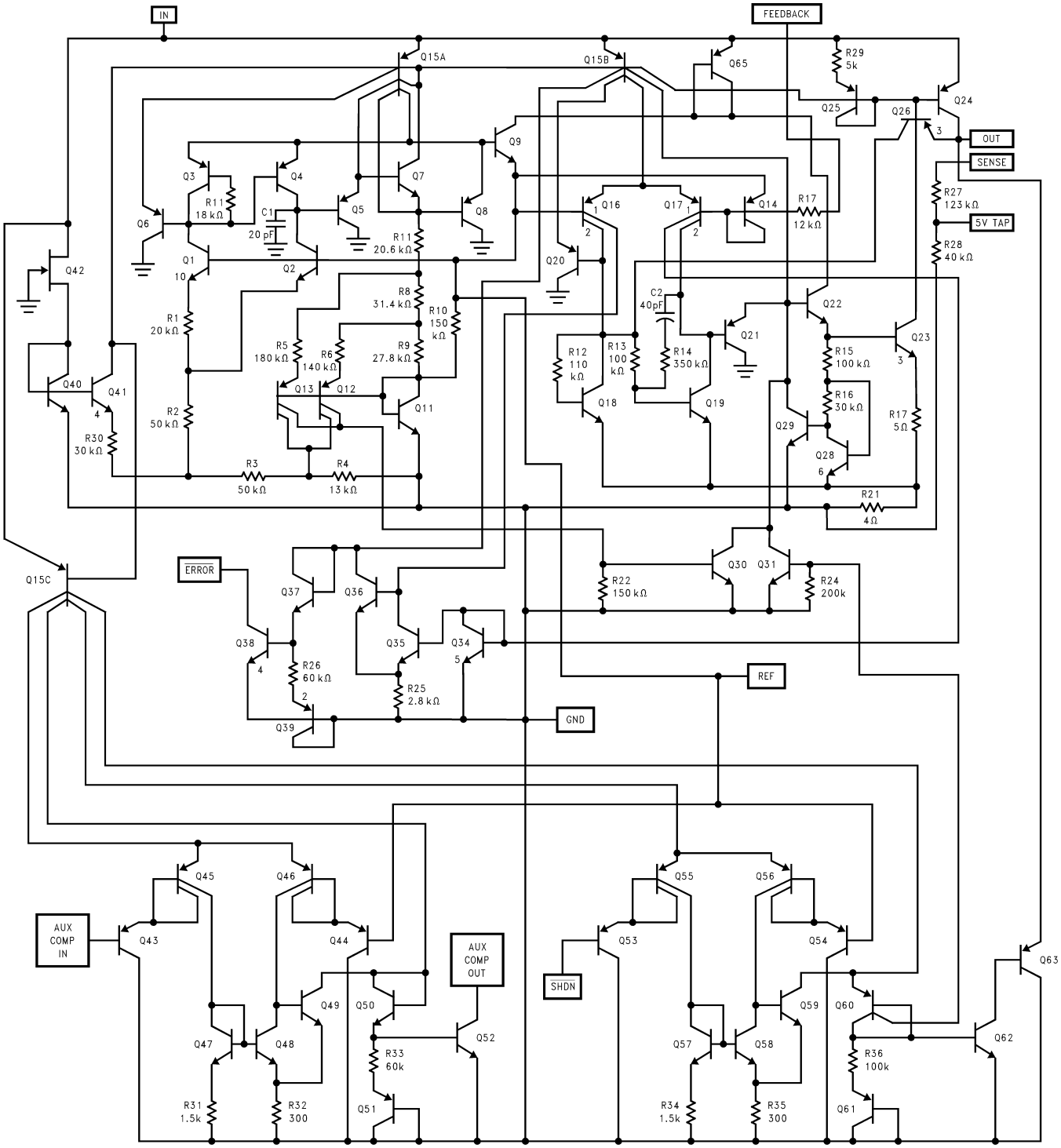


Figure 33.

SCHEMATIC DIAGRAM



APPLICATION HINTS

Heatsink Requirements (Industrial Temperature Range Devices)

The maximum allowable power dissipation for the LP2952/LP2953 is limited by the maximum junction temperature (+125°C) and the external factors that determine how quickly heat flows away from the part: the *ambient temperature* and the *junction-to-ambient thermal resistance* for the specific application.

The industrial temperature range (−40°C ≤ T_J ≤ +125°C) parts are manufactured in PDIP and surface mount packages which contain a copper lead frame that allows heat to be effectively conducted away from the die, through the ground pins of the IC, and into the copper of the PC board. Details on heatsinking using PC board copper are covered later.

To determine if a heatsink is required, the maximum power dissipated by the regulator, P(max), must be calculated. It is important to remember that if the regulator is powered from a transformer connected to the AC line, the **maximum specified AC input voltage** must be used (since this produces the maximum DC input voltage to the regulator). Figure 34 shows the voltages and currents which are present in the circuit. The formula for calculating the power dissipated in the regulator is also shown in Figure 34:

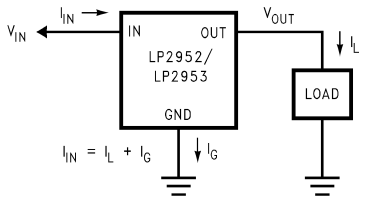


Figure 34. $P_{TOTAL} = (V_{IN} - V_{OUT})\ I_L + (V_{IN})\ I_G$ Current/Voltage Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R(max). This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max)\theta_{(J-A)} = T_R(max)/P(max) \quad (1)$$

where

- T_J(max) is the maximum allowable junction temperature
- T_A(max) is the maximum ambient temperature

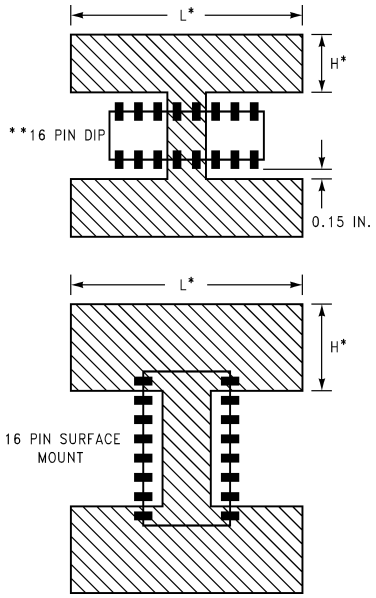
Using the calculated values for T_R(max) and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

The heatsink is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are given in Table 1.

Table 1. Heat Conducting Pins

Part	Package	Pins
LP2952IN, LP2952AIN,	14-Pin PDIP	3, 4, 5,
LP2952IN-3.3, LP2952AIN-3.3		10, 11, 12
LP2953IN, LP2953AIN,	16-Pin PDIP	4, 5, 12, 13
LP2953IN-3.3, LP2953AIN-3.3		
LP2952IM, LP2952AIM,	16-Pin Surface Mount	1, 8, 9, 16
LP2952IM-3.3, LP2952AIM-3.3,		
LP2953IM, LP2953AIM,		
LP2953IM-3.3, LP2953AIM-3.3		

Figure 35 shows copper patterns which may be used to dissipate heat from the LP2952 and LP2953. Table 2 shows some values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W for 1 oz. copper.



* For best results, use L = 2H

** 14-Pin PDIP is similar, refer to Table 1 for pins designated for heatsinking.

Figure 35. Copper Heatsink Patterns

Table 2. Thermal Resistance for Various Copper Heatsink Patterns

Package	L (in.)	H (in.)	θ_{J-A} (°C/W)
16-Pin PDIP	1	0.5	70
	2	1	60
	3	1.5	58
	4	0.19	66
	6	0.19	66
14-Pin PDIP	1	0.5	65
	2	1	51
	3	1.5	49
Surface Mount	1	0.5	83
	2	1	70
	3	1.5	67
	6	0.19	69
	4	0.19	71
	2	0.19	73

Heatsink Requirements (Military Temperature Range Devices)

The maximum allowable power dissipation for the LP2953AMJ is limited by the maximum junction temperature (+150°C) and the two parameters that determine how quickly heat flows away from the die: *the ambient temperature and the junction-to-ambient thermal resistance of the part*.

The military temperature range (−55°C ≤ T_J ≤ +150°C) parts are manufactured in CDIP packages which contain a KOVAR lead frame (unlike the industrial parts, which have a copper lead frame). The KOVAR material is necessary to attain the hermetic seal required in military applications.

The KOVAR lead frame does not conduct heat as well as copper, which means that the PC board copper can not be used to significantly reduce the overall junction-to-ambient thermal resistance in applications using the LP2953AMJ part.

The power dissipation calculations for military applications are done exactly the same as was detailed in the previous section, with one important exception: the value for $\theta_{(J-A)}$, the junction-to-ambient thermal resistance, is fixed at 95°C/W and can not be changed by adding copper foil patterns to the PC board. This leads to an important fact: The *maximum allowable power dissipation in any application using the LP2953AMJ is dependent only on the ambient temperature:*

$$P(max) = T_{R(max)} / \theta_{(J-A)}$$

$$P(max) = \frac{T_{J(max)} - T_{A(max)}}{\theta_{(J-A)}}$$

$$P(max) = \frac{150 - T_{A(max)}}{95} \quad (2)$$

Figure 36 shows a graph of maximum allowable power dissipation vs. ambient temperature for the LP2953AMJ, made using the 95°C/W value for $\theta_{(J-A)}$ and assuming a maximum junction temperature of 150°C (caution: the *maximum* ambient temperature which will be reached in a given application must always be used to calculate maximum allowable power dissipation).

External Capacitors

A 2.2 µF (or greater) capacitor is required between the output pin and ground to assure stability when the output is set to 5V. Without this capacitor, the part will oscillate. Most type of tantalum or aluminum electrolytics will work here. Film types will work, but are more expensive. Many aluminum electrolytics contain electrolytes which freeze at −30°C, which requires the use of solid tantalums below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500 kHz (the ESR may increase by a factor of **20** or **30** as the temperature is reduced from 25°C to −30°C). The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.68 µF for currents below 10 mA or 0.22 µF for currents below 1 mA.

Programming the output for voltages below 5V runs the error amplifier at lower gains requiring *more* output capacitance for stability. At 3.3V output, a minimum of 4.7 µF is required. For the worst-case condition of 1.23V output and 250 mA of load current, a 6.8 µF (or larger) capacitor should be used.

A 1 µF capacitor should be placed from the input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery input is used.

Stray capacitance to the Feedback terminal can cause instability. This problem is most likely to appear when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitance to 6.8 µF (or greater) will cure the problem.

Minimum Load

When setting the output voltage using an external resistive divider, a minimum current of 1 µA is recommended through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the electrical characteristic test conditions, so this value must be used to obtain correlation on these tested limits.

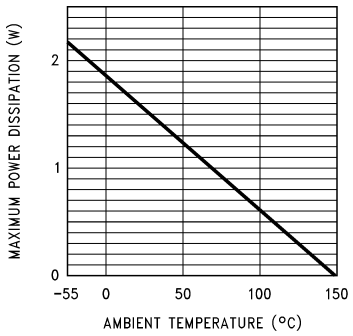


Figure 36. Power Derating Curve for LP2953AMJ

Programming the Output Voltage

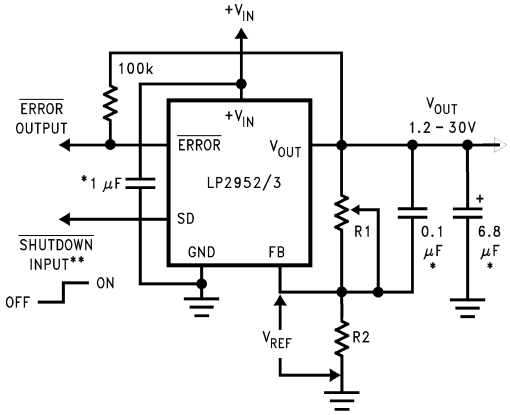
The regulator may be pin-strapped for 5V operation using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and 5V Tap pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 30V maximum rating using an external pair of resistors (see Figure 37). The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1) \quad (3)$$

where

- V_{REF} is the 1.23V reference and I_{FB} is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 1 µA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see **MINIMUM LOAD**). I_{FB} will produce a typical 2% error in V_{OUT} which can be eliminated at room temperature by trimming R1. For better accuracy, choosing R2 = 100 kΩ will reduce this error to 0.17% while increasing the resistor program current to 12 µA. Since the typical quiescent current is 120 µA, this added current is negligible.



* SeeApplication Hints

** Drive with TTL-low to shut down

Figure 37. Adjustable Regulator

Dropout Voltage

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

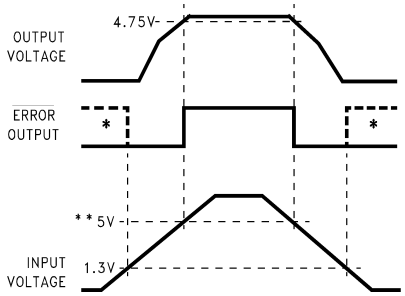
Dropout Detection Comparator

This comparator produces a logic “LOW” whenever the output falls out of regulation by more than about 5%. This figure results from the comparator's built-in offset of 60 mV divided by the 1.23V reference (refer to Block Diagrams). The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 38 gives a timing diagram showing the relationship between the output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5V output. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3V input. It goes high at about 5V input, where the output equals 4.75V. Since the dropout voltage is load dependent, the **input** voltage trip points will vary with load current. The **output** voltage trip point does not vary.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the regulator output or some other supply voltage. Using the regulator output prevents an invalid “HIGH” on the comparator output which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3V. In selecting a value for the pull-up resistor, note that while the output can sink 400 µA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. This resistor is not required if the output is unused.

When $V_{IN} \leq 1.3V$, the error flag pin becomes a high impedance, allowing the error flag voltage to rise to its pull-up voltage. Using V_{OUT} as the pull-up voltage (rather than an external 5V source) will keep the error flag voltage below 1.2V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.



* In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.
** Exact value depends on dropout voltage. (See Application Hints)

Figure 38. $\overline{\text{ERROR}}$ Output Timing

Output Isolation

The regulator output can be left connected to an active voltage source (such as a battery) with the regulator input power shut off, **as long as the regulator ground pin is connected to ground.** If the ground pin is left floating, **damage to the regulator can occur** if the output is pulled up by an external voltage source.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to Figure 37). The formula for selecting the capacitor to be used is:

$$C_B = \frac{1}{2\pi\ R1 \times 20\ Hz} \quad (4)$$

This gives a value of about 0.1 µF. When this is used, the output capacitor must be 6.8 µF (or greater) to maintain stability. The 0.1 µF capacitor reduces the high frequency gain of the circuit to unity, lowering the output noise from 260 µV to 80 µV using a 10 Hz to 100 kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at high output voltages.

Auxiliary Comparator

(LP2953 only)

The LP2953 contains an auxiliary comparator whose inverting input is connected to the 1.23V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The non-inverting input and output are brought out for external connections.

Shutdown Input

A logic-level signal will shut off the regulator output when a “LOW” (<1.2V) is applied to the $\overline{\text{Shutdown}}$ input.

To prevent possible mis-operation, the $\overline{\text{Shutdown}}$ input must be actively terminated. If the input is driven from open-collector logic, a pull-up resistor (20 kΩ to 100 kΩ recommended) should be connected from the $\overline{\text{Shutdown}}$ input to the regulator input.

If the $\overline{\text{Shutdown}}$ input is driven from a source that actively pulls high and low (like an op-amp), the pull-up resistor is not required, but may be used.

If the shutdown function is not to be used, the cost of the pull-up resistor can be saved by simply tying the $\overline{\text{Shutdown}}$ input directly to the regulator input.

IMPORTANT: Since the Absolute Maximum Ratings state that the $\overline{\text{Shutdown}}$ input can not go more than 0.3V below ground, the reverse-battery protection feature which protects the regulator input is sacrificed if the $\overline{\text{Shutdown}}$ input is tied directly to the regulator input.

If reverse-battery protection is required in an application, *the pull-up resistor between the $\overline{\text{Shutdown}}$ input and the regulator input must be used.*

Typical Applications

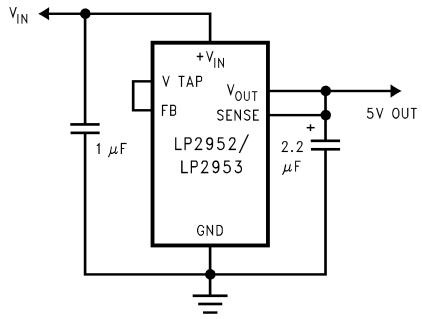
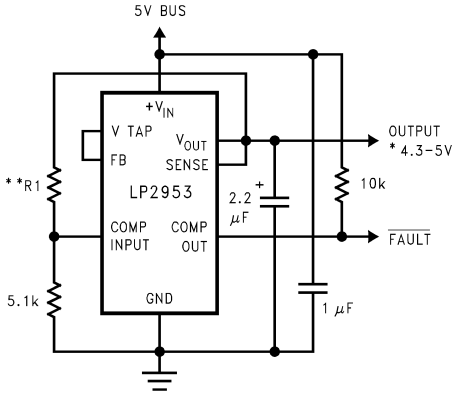


Figure 39. Basic 5V Regulator



* Output voltage equals $+V_{IN}$ minum dropout voltage, which varies with output current. Current limits at a maximum of 380 mA (typical).
** Select R1 so that the comparator input voltage is 1.23V at the output voltage which corresponds to the desired fault current value.

Figure 40. 5V Current Limiter with Load Fault Indicator

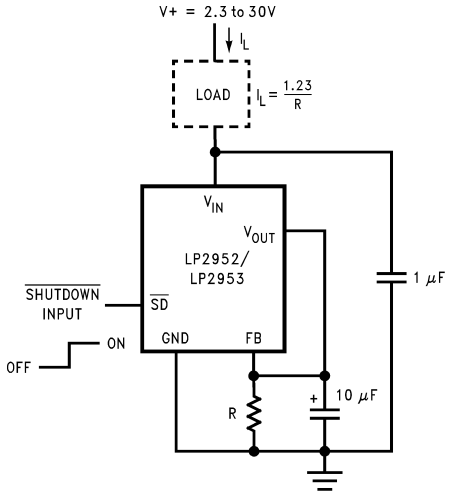
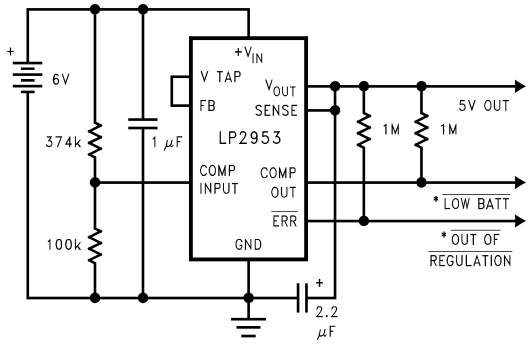


Figure 41. Low T.C. Current Sink

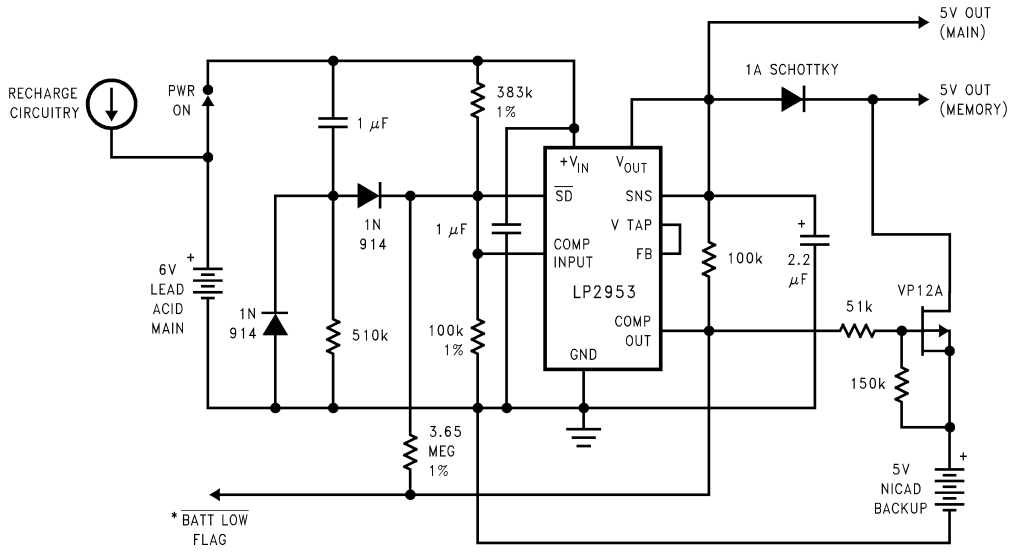


* Connect to Logic or µP control inputs.

LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or power down some hardware with high power requirements. The output is still in regulation at this time.

OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

Figure 42. 5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION



The circuit switches to the NI-CAD backup battery when the main battery voltage drops below about 5.6V, and returns to the main battery when its voltage is recharged to about 6V.

The 5V MAIN output powers circuitry which requires no backup, and the 5V MEMORY output powers critical circuitry which can not be allowed to lose power.

* The $\overline{\text{BATTERY LOW}}$ flag goes low whenever the circuit switches to the NI-CAD backup battery.

Figure 43. 5V Battery Powered Supply with Backup and Low Battery Flag

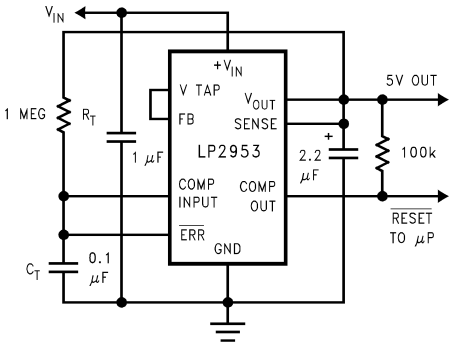
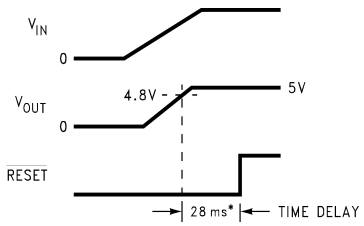
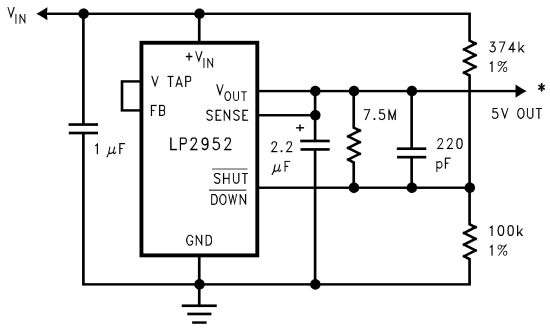


Figure 44. 5V Regulator with Timed Power-On Reset



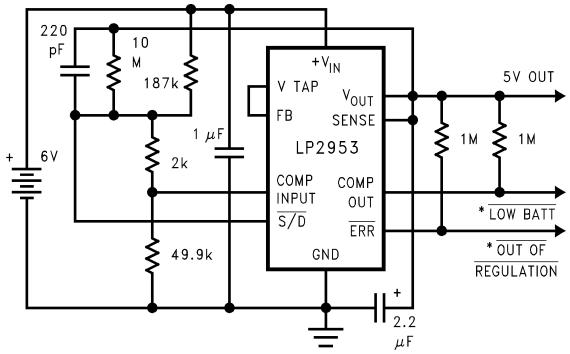
* R_T = 1 MEG, C_T = 0.1 µF

Figure 45. Timing Diagram for Timed Power-On Reset



* Turns ON at V_{IN} = 5.87V
Turns OFF at V_{IN} = 5.64V
(for component values shown)

Figure 46. 5V Regulator with Snap-On/Snap-Off Feature and Hysteresis



* Connect to Logic or µP control inputs.
OUTPUT has SNAP-ON/SNAP-OFF feature.
LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or shut down hardware with high power requirements. The output is still in regulation at this time.
OUT OF REGULATION flag goes low if the output goes below about 4.7V, which could occur from a load fault.
OUTPUT has SNAP-ON/SNAP-OFF feature. Regulator snaps ON at about 5.7V input, and OFF at about 5.6V.

Figure 47. 5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION with SNAP-ON/SNAP-OFF Output

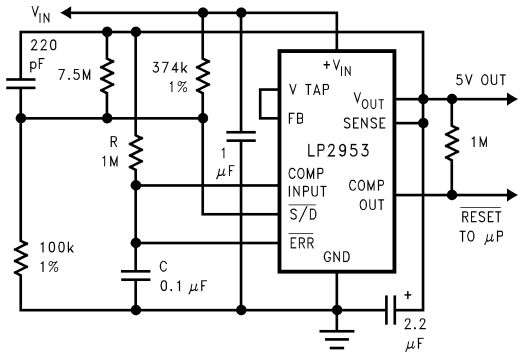
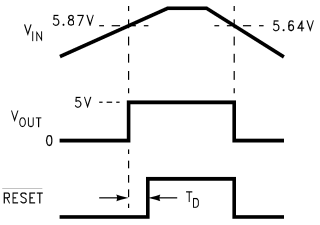


Figure 48. 5V Regulator with Timed Power-On Reset, Snap-On/Snap-Off Feature and Hysteresis



Td = (0.28) RC = 28 ms for components shown.

Figure 49. Timing Diagram

REVISION HISTORY

Changes from Revision C (March 2005) to Revision D	Page
• layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2952AIM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	LP2952AIM	
LP2952AIM-3.3/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952AIM -3.3	Samples
LP2952AIM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952AIM	Samples
LP2952AIMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125	LP2952AIM	
LP2952AIMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952AIM	Samples
LP2952IM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	LP2952IM	
LP2952IM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952IM	Samples
LP2952IMX-3.3/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952IM -3.3	Samples
LP2952IMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2952IM	Samples
LP2953AIM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953AIM	Samples
LP2953AIMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953AIM	Samples
LP2953IM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 125	LP2953IM	
LP2953IM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953IM	Samples
LP2953IMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LP2953IM	Samples
LP2953IN/NOPB	ACTIVE	PDIP	NBG	16	20	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP2953IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

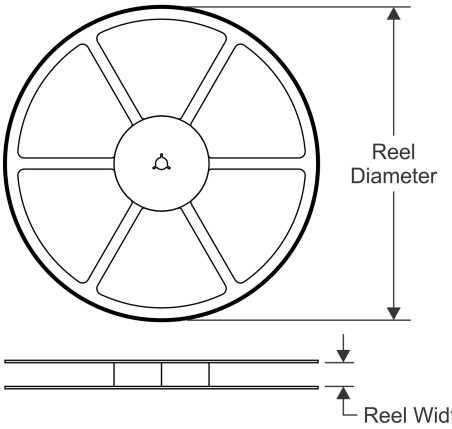
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

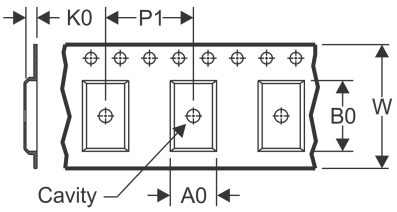
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

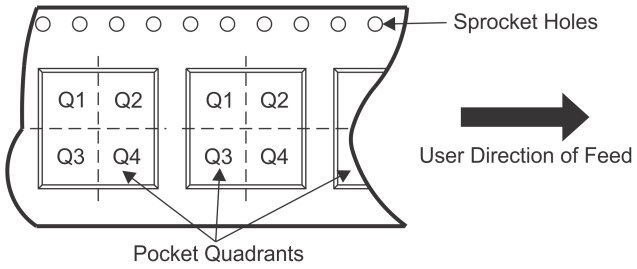


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

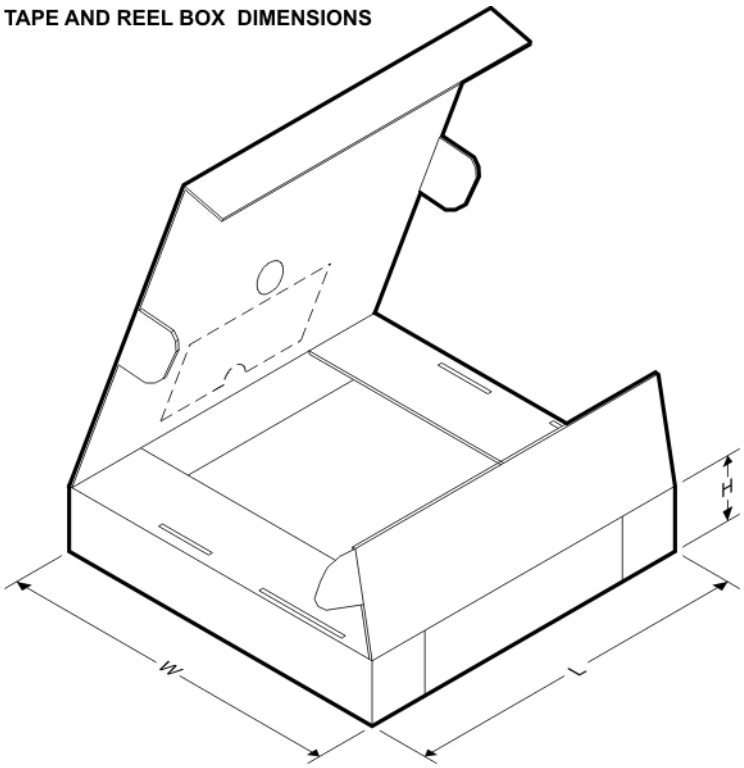
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2952AIMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2952AIMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2952IMX-3.3/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2952IMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2953AIMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2953IMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

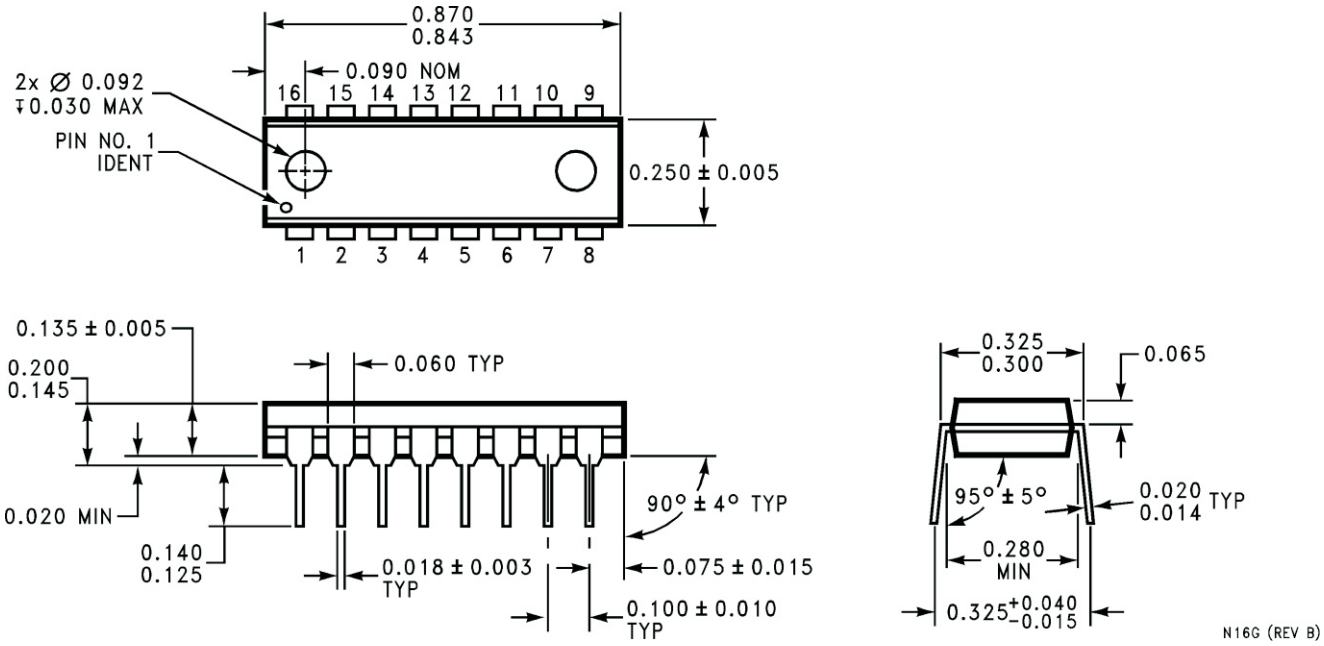
TAPE AND REEL BOX DIMENSIONS



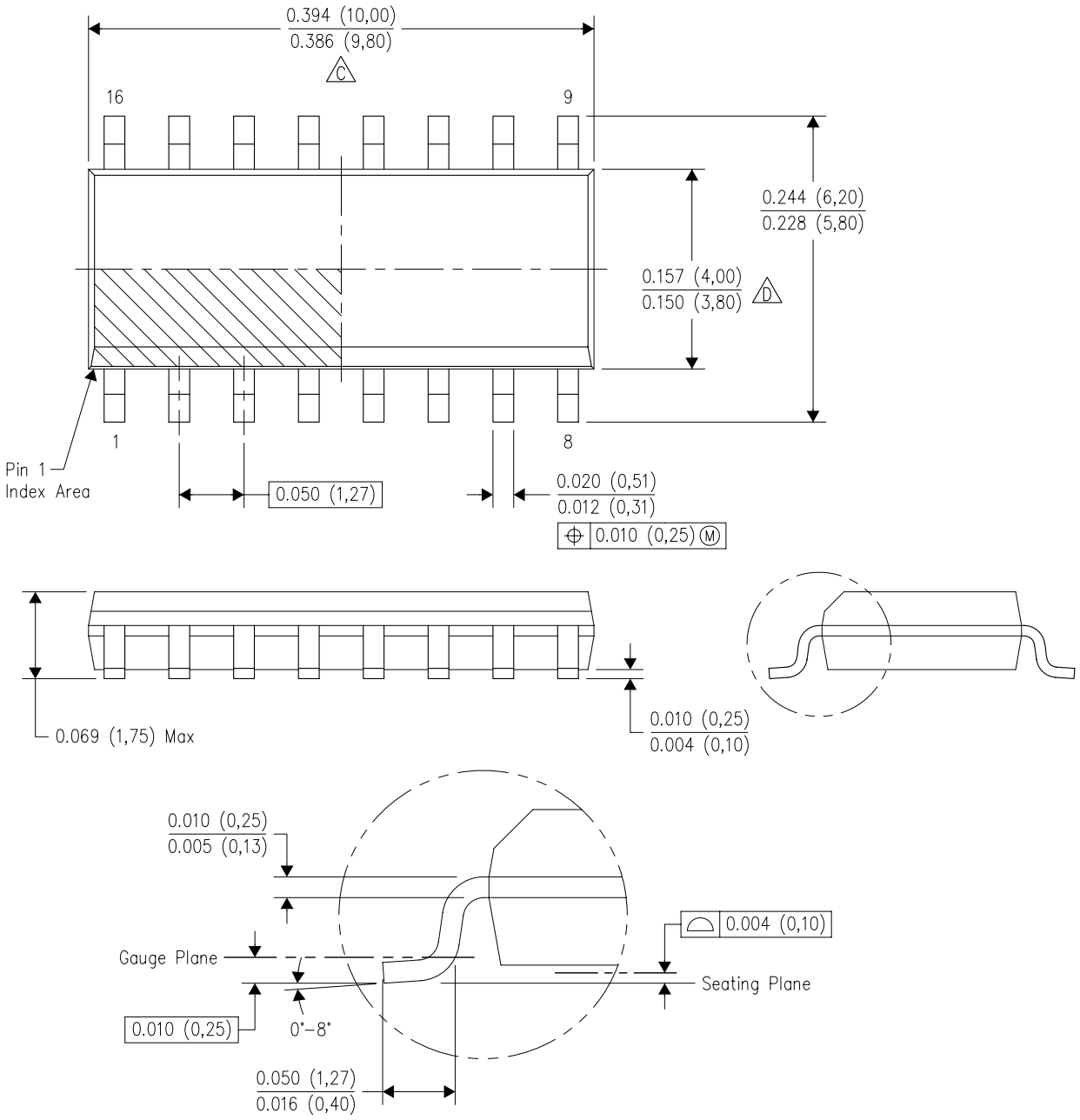
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2952AIMX	SOIC	D	16	2500	367.0	367.0	35.0
LP2952AIMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2952IMX-3.3/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2952IMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2953AIMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
LP2953IMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

NBG0016G


0.870
0.843
0.090 NOM
16 15 14 13 12 11 10 9
2x Ø 0.092
±0.030 MAX
PIN NO. 1
IDENT
0.250 ± 0.005
1 2 3 4 5 6 7 8
0.135 ± 0.005
0.200
0.145
0.060 TYP
0.020 MIN
0.140
0.125
90° ± 4° TYP
0.018 ± 0.003
TYP
0.075 ± 0.015
0.100 ± 0.010
TYP
0.325
0.300
0.065
95° ± 5°
0.020 TYP
0.014
0.280
MIN
0.325 +0.040 −0.015
N16G (REV B)

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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