



BUK7607-30B

N-channel TrenchMOS standard level FET

Rev. 02 — 21 February 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

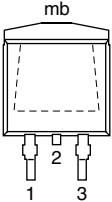
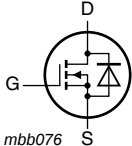
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 3	[1]	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	157	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11 ; see Figure 12	-	5.9	7	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	329	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 24\text{ V}$; $T_j = 25\text{ °C}$; see Figure 13	-	12	-	nC

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT404 (D2PAK)	
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7607-30B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V	
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	30	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 10 V; see Figure 1 [1]	-	75	A	
		T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 3 [2]	-	108	A	
		[1]	-	75	A	
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 3	-	435	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	157	W	
T _{stg}	storage temperature		-55	175	°C	
T _j	junction temperature		-55	175	°C	
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	75	A
			[2]	-	108	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	435	A	
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 75 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	-	329	mJ	

[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.

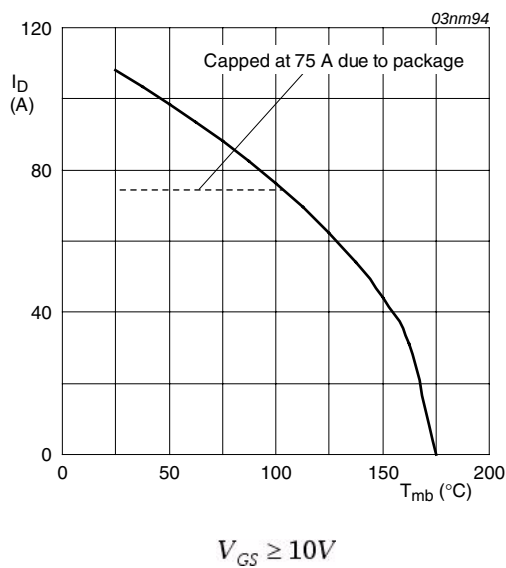


Fig 1. Normalized continuous drain current as a function of mounting base temperature

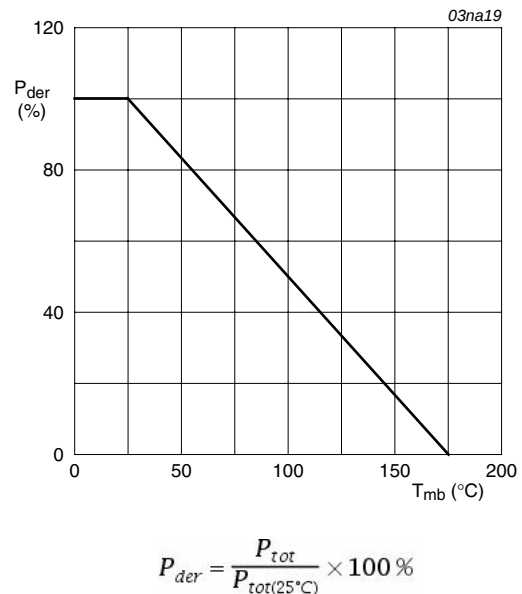


Fig 2. Normalized total power dissipation as a function of mounting base temperature

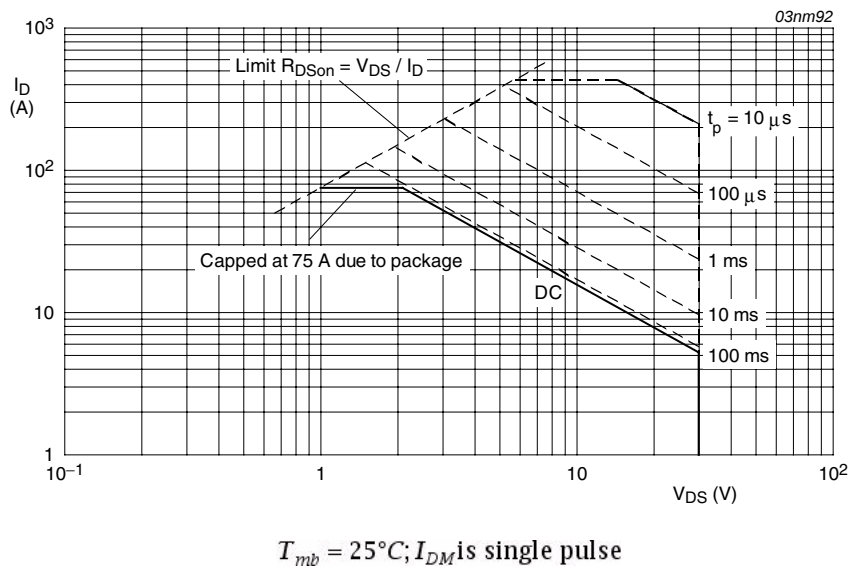


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	-	50	K/W

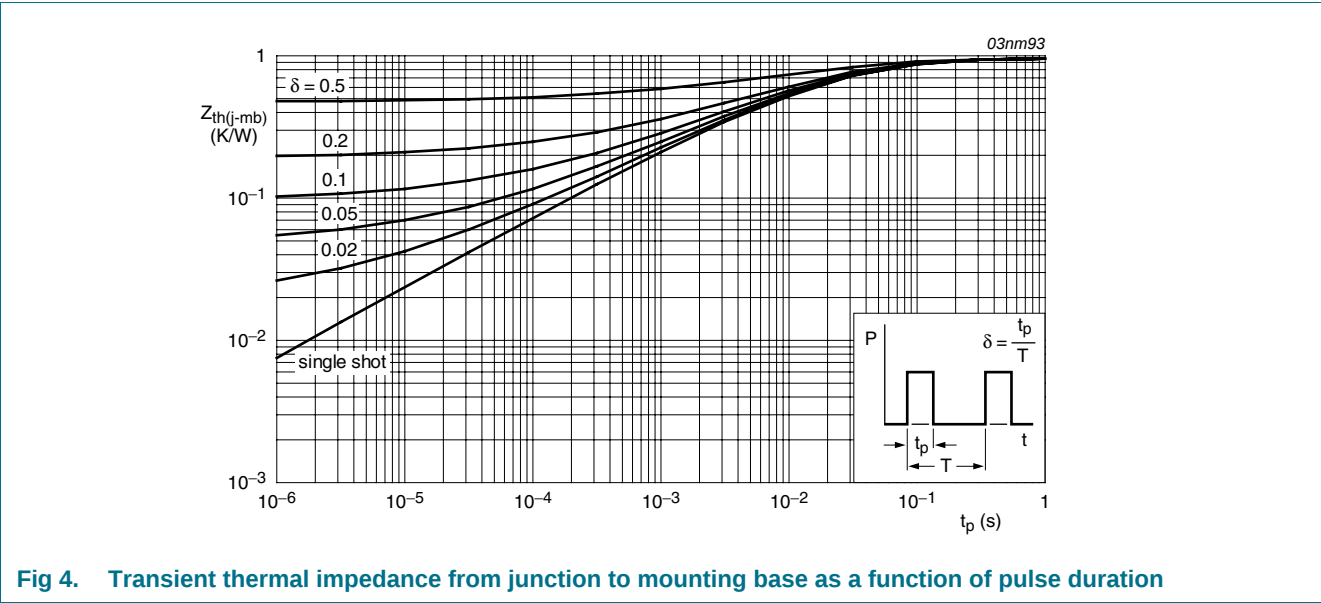
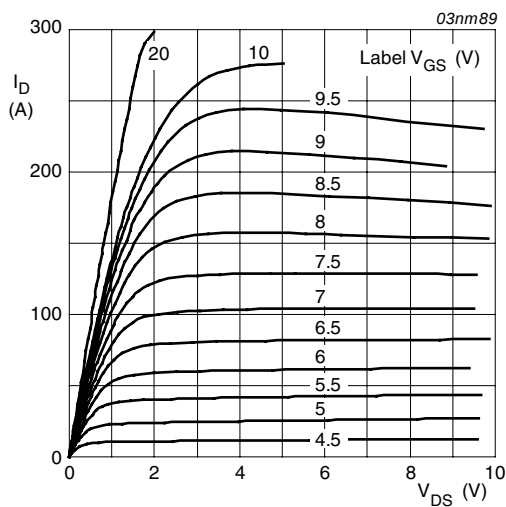


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

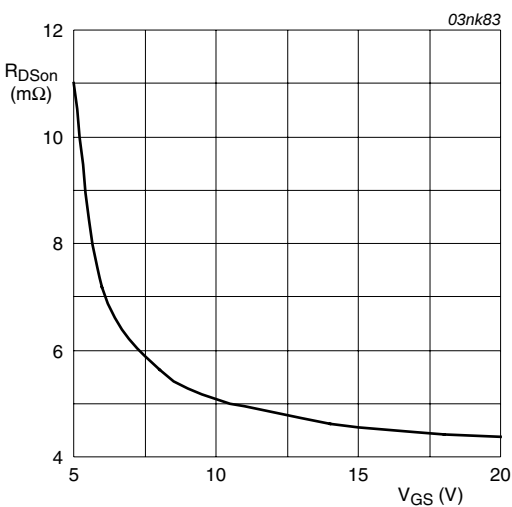
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	4.4	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 11 ; see Figure 12	-	-	13.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	5.9	7	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 24 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 13	-	36	-	nC
Q _{GS}	gate-source charge		-	9	-	nC
Q _{GD}	gate-drain charge		-	12	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 14	-	1820	2427	pF
C _{oss}	output capacitance		-	632	758	pF
C _{rss}	reverse transfer capacitance		-	256	351	pF
t _{d(on)}	turn-on delay time	V _{DS} = 25 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	20	-	ns
t _r	rise time		-	51	-	ns
t _{d(off)}	turn-off delay time		-	51	-	ns
t _f	fall time		-	44	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die ; T _j = 25 °C	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die ; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	from source lead 6 mm from package to source bond pad ; T _j = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = -10 V; V _{DS} = 20 V; T _j = 25 °C	-	46	-	ns
Q _r	recovered charge		-	28	-	nC



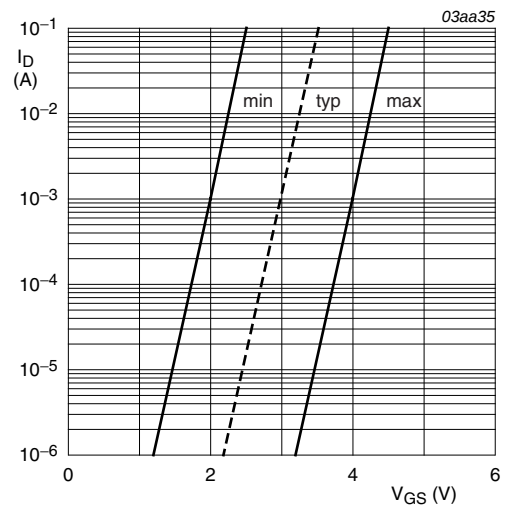
$T_j = 25^{\circ}\text{C}; t_p = 300\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



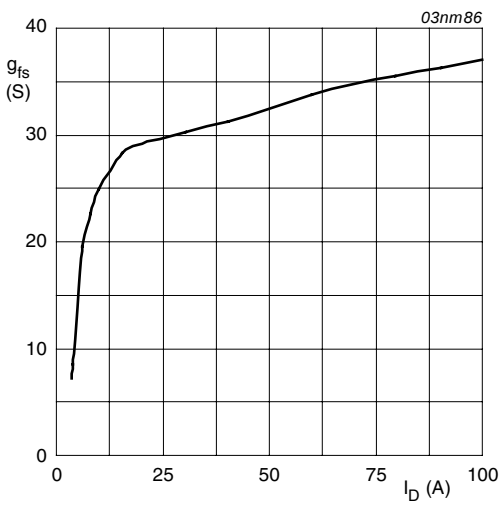
$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^{\circ}\text{C}; V_{DS} = 25\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values

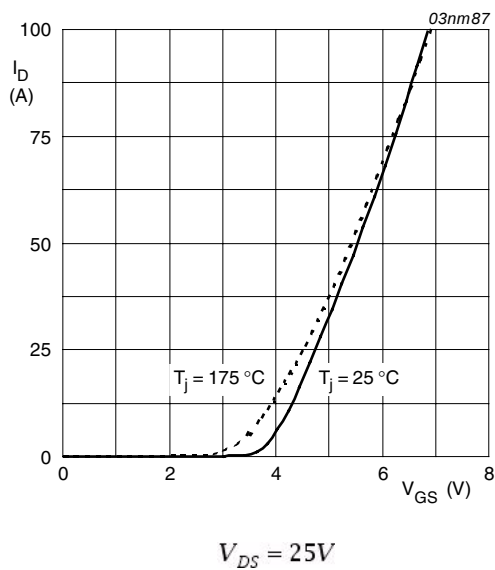


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

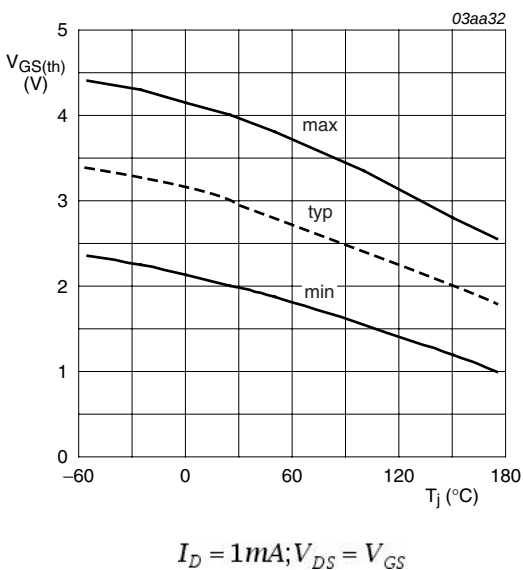


Fig 10. Gate-source threshold voltage as a function of junction temperature

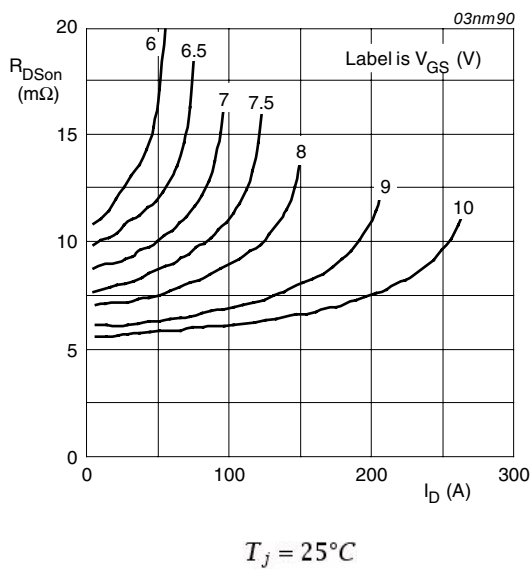


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

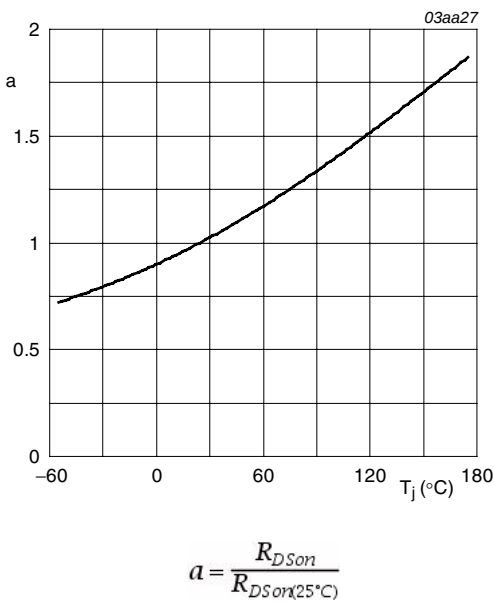
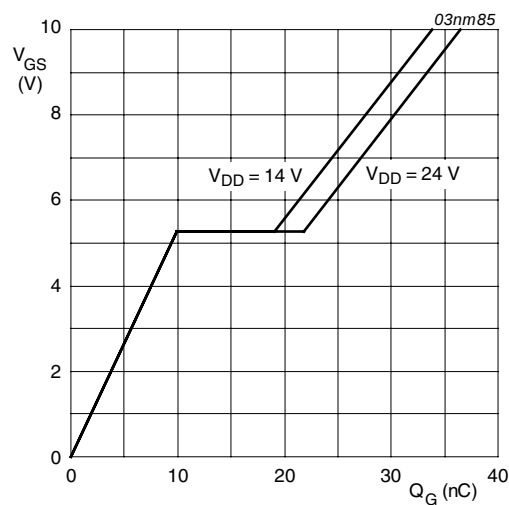
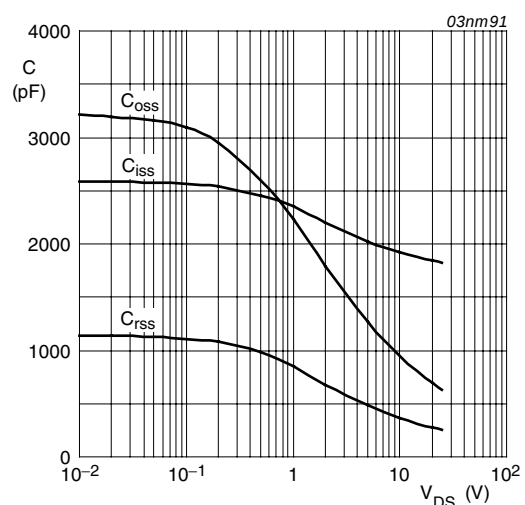


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



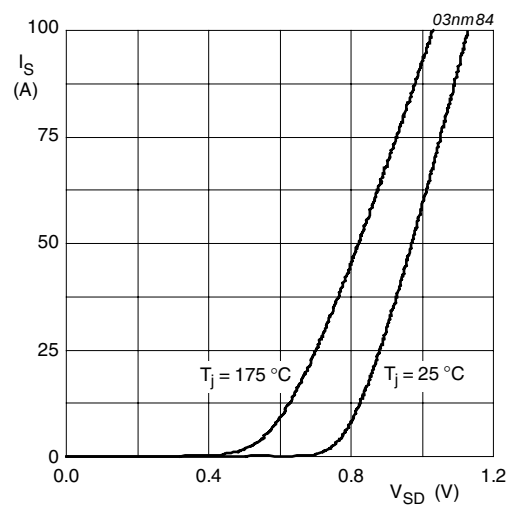
$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

Fig 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



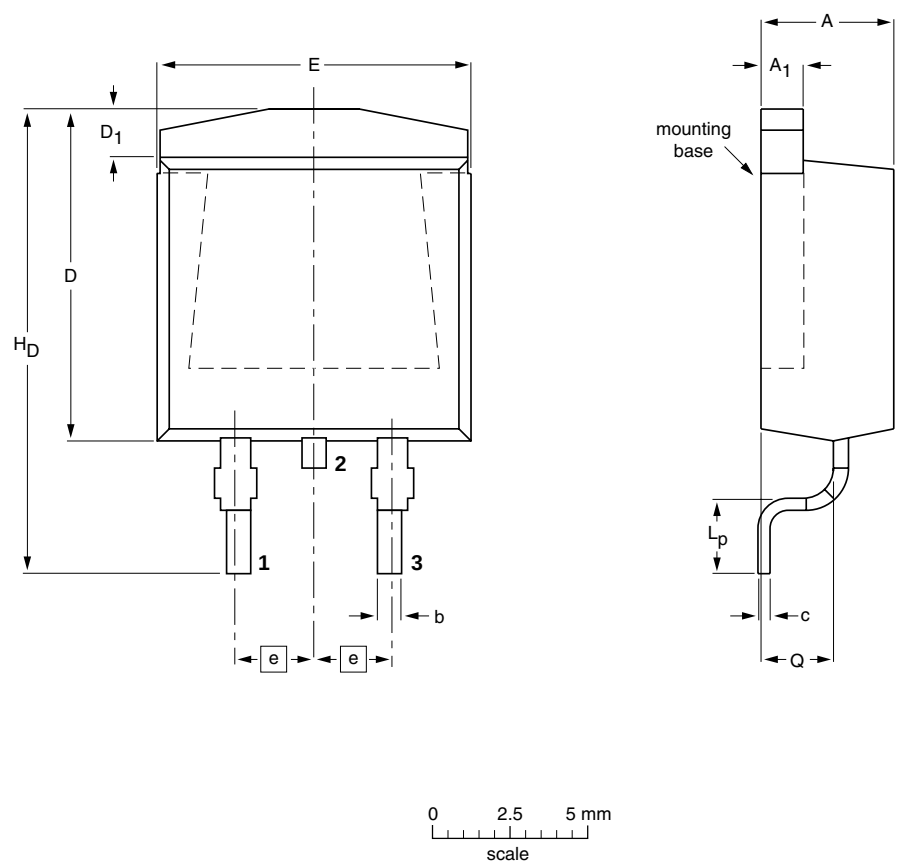
$V_{GS} = 0\text{ V}$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7607-30B v.2	20110221	Product data sheet	-	BUK75_7607_30B v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BUK7607-30B separated from data sheet BUK75_7607_30B v.1.			
BUK75_7607_30B v.1	20030407	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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