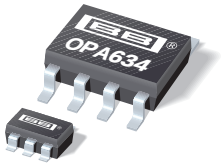
BURR-BROWN®




# OPA634
# OPA635

For most current data sheet and other product information, visit www.burr-brown.com

## SpeedPlus™ Wideband, Single Supply OPERATIONAL AMPLIFIERS

## FEATURES

- HIGH BANDWIDTH: 150MHz (G = +2)
- +3V AND +5V OPERATION
- ZERO POWER DISABLE (OPA635)
- INPUT RANGE INCLUDES GROUND
- 4.8V OUTPUT SWING ON +5V SUPPLY
- HIGH OUTPUT CURRENT: 80mA
- HIGH SLEW RATE: 250V/μs
- LOW INPUT VOLTAGE NOISE: 5.6nV/$\sqrt{Hz}$
- AVAILABLE IN SOT23 PACKAGES

## APPLICATIONS

- SINGLE SUPPLY ADC INPUT BUFFER
- SINGLE SUPPLY VIDEO LINE DRIVER
- WIRELESS LAN IF AMPLIFIER
- CCD IMAGING CHANNELS
- LOW POWER ULTRASOUND

## DESCRIPTION

The OPA634 and OPA635 are low power, voltage-feedback, high-speed amplifiers designed to operate on +3V or +5V single-supply voltages. Operation on ±5V or +10V supplies is also supported. The input range extends below ground and to within 1.2V of the positive supply. Using complementary common-emitter outputs provides an output swing to within 30mV of ground and 140mV of positive supply. The high output drive current, low differential gain and phase errors make them ideal for single-supply composite video line driving.

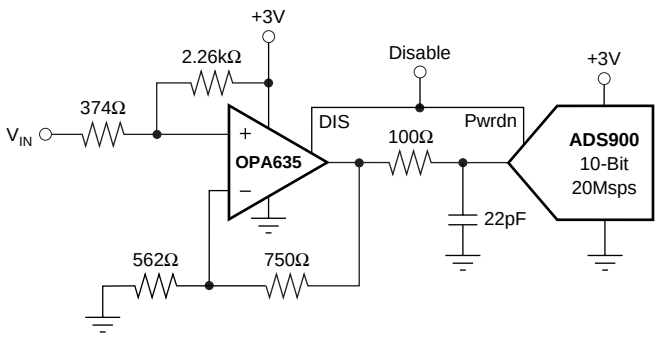
Low distortion operation is ensured by the high gain bandwidth (140MHz) and slew rate (250V/μs). This makes the OPA634 and OPA635 ideal input buffer stages to 3V and 5V CMOS converters. Unlike other low power, single-supply operational amplifiers, distortion performance improves as the signal swing is decreased.

A low 5.6nV input voltage noise supports wide dynamic range operation. Multiplexing or system power reduction can be achieved using the high-speed disable line with the OPA635. Power dissipation can be reduced to zero by taking the disable line High.

The OPA634 and OPA635 are available in an industry standard SO-8 package. The OPA634 is also available in an ultra-small SOT23-5 package, while the OPA635 is available in the SOT23-6. Where lower supply current and speed are required, consider the OPA631 and OPA632.

### RELATED PRODUCTS

| | SINGLES | DUALS |
|---|---|---|
| Medium Speed, No Disable | OPA631 | OPA2631 |
| With Disable | OPA632 | — |
| High Speed, No Disable | OPA634 | OPA2634 |
| With Disable | OPA635 | — |

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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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Printed in U.S.A. June, 1999

# SPECIFICATIONS: $V_S$ = +5V

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 1).

| PARAMETER | CONDITIONS | OPA634U, N OPA635U, N TYP +25°C | GUARANTEED +25°C | GUARANTEED 0°C to 70°C | GUARANTEED –40°C to +85°C | UNITS | MIN/ MAX | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE (Figure 1)** | | | | | | | | |
| Small-Signal Bandwidth | G = +2, $V_O$ ≤ 0.5Vp-p | 150 | 100 | 84 | 78 | MHz | min | B |
| | G = +5, $V_O$ ≤ 0.5Vp-p | 36 | 24 | 20 | 18 | MHz | min | B |
| | G = +10, $V_O$ ≤ 0.5Vp-p | 16 | 11 | 10 | 8 | MHz | min | B |
| Gain Bandwidth Product | G ≥ +10 | 140 | 100 | 82 | 75 | MHz | min | B |
| Peaking at a Gain of +1 | $V_O$ ≤ 0.5Vp-p | 5 | — | — | — | dB | typ | C |
| Slew Rate | G = +2, 2V Step | 250 | 170 | 125 | 115 | V/µs | min | B |
| Rise Time | 0.5V Step | 2.4 | 3.4 | 4.7 | 5.2 | ns | max | B |
| Fall Time | 0.5V Step | 2.4 | 3.5 | 4.5 | 4.8 | ns | max | B |
| Settling Time to 0.1% | G = +2, 1V Step | 15 | 19 | 22 | 23 | ns | max | B |
| Spurious Free Dynamic Range | $V_O$ = 2Vp-p, f = 5MHz | 63 | 56 | 51 | 50 | dBc | min | B |
| Input Voltage Noise | f > 1MHz | 5.6 | 6.2 | 7.3 | 7.7 | nV/√Hz | max | B |
| Input Current Noise | f > 1MHz | 2.8 | 3.8 | 4.2 | 5 | pA/√Hz | max | B |
| NTSC Differential Gain | | 0.10 | — | — | — | % | typ | C |
| NTSC Differential Phase | | 0.16 | — | — | — | degrees | typ | C |
| **DC PERFORMANCE** | | | | | | | | |
| Open-Loop Voltage Gain | | 66 | **63** | 60 | 53 | dB | min | A |
| Input Offset Voltage | | 3 | **7** | 8 | 10 | mV | max | A |
| Average Offset Voltage Drift | | — | — | — | 4.6 | µV/°C | max | B |
| Input Bias Current | $V_{CM}$ = 2.0V | 25 | 45 | 55 | 80 | µA | max | B |
| Input Offset Current | $V_{CM}$ = 2.0V | 0.6 | 2 | 2.3 | 4 | µA | max | B |
| Input Offset Current Drift | | — | — | — | 15 | nA/°C | max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage | | –0.24 | –0.1 | –0.05 | –0.01 | V | max | B |
| Most Positive Input Voltage | | 3.8 | **3.5** | 3.45 | 3.4 | V | min | A |
| Common-Mode Rejection (CMRR) | Input Referred | 78 | **75** | 73 | 65 | dB | min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | | 10 \|\| 2.1 | — | — | — | kΩ \|\| pF | typ | C |
| Common-Mode | | 400 \|\| 1.2 | — | — | — | kΩ \|\| pF | typ | C |
| **OUTPUT** | | | | | | | | |
| Least Positive Output Voltage | $R_L$ = 1kΩ to 2.5V | 0.03 | 0.05 | 0.06 | 0.07 | V | max | B |
| | $R_L$ = 150Ω to 2.5V | 0.1 | **0.14** | 0.15 | 0.22 | V | max | A |
| Most Positive Output Voltage | $R_L$ = 1kΩ to 2.5V | 4.86 | 4.8 | 4.75 | 4.7 | V | min | B |
| | $R_L$ = 150Ω to 2.5V | 4.65 | **4.55** | 4.5 | 4.4 | V | min | A |
| Current Output, Sourcing | | 80 | **50** | 45 | 20 | mA | min | A |
| Current Output, Sinking | | 100 | **80** | 65 | 20 | mA | min | A |
| Short-Circuit Current (output shorted to either supply) | | 100 | — | — | — | mA | typ | C |
| Closed-Loop Output Impedance | G = +2, f ≤ 100kHz | 0.2 | — | — | — | Ω | typ | C |
| **DISABLE (OPA635 only)** | | | | | | | | |
| On Voltage (device enabled Low) | | 1.0 | **1.0** | 1.0 | 1.0 | V | min | A |
| Off Voltage (device disabled High) | | 4.0 | **4.1** | 4.2 | 4.3 | V | max | A |
| On Disable Current (DIS pin) | | 70 | **110** | 120 | 120 | µA | max | A |
| Off Disable Current (DIS pin) | | 0 | — | — | — | µA | typ | C |
| Disabled Quiescent Current | | 0 | **30** | 40 | 50 | µA | max | A |
| Disable Time | | 100 | — | — | — | ns | typ | C |
| Enable Time | | 60 | — | — | — | ns | typ | C |
| Off Isolation | f = 5MHz, Input to Output | 70 | — | — | — | dB | typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Minimum Operating Voltage | | — | **2.7** | 2.7 | 2.7 | V | min | A |
| Maximum Operating Voltage | | — | **10.5** | 10.5 | 10.5 | V | max | A |
| Maximum Quiescent Current | | 12 | **12.5** | 13 | 13.25 | mA | max | A |
| Minimum Quiescent Current | | 12 | **11.3** | 9.75 | 8.5 | mA | min | A |
| Power Supply Rejection Ratio (PSRR) | Input Referred | 55 | **52** | 50 | 49 | dB | min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specification: U, N | | –40 to +85 | | | | °C | typ | C |
| Thermal Resistance | | | | | | | | |
| U SO-8 | | 125 | | | | °C/W | typ | C |
| N SOT23-5, SOT23-6 | | 150 | | | | °C/W | typ | C |

NOTE: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

# SPECIFICATIONS: $V_S$ = +3V

At $T_A$ = 25°C, G = +2 and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 2).

| PARAMETER | CONDITIONS | OPA634U, N OPA635U, N | | | | UNITS | MIN/ MAX | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|---|
| | | TYP | GUARANTEED | | | | | |
| | | +25°C | +25°C | 0°C to 70°C | –40°C to +85°C | | | |
| **AC PERFORMANCE (Figure 2)** | | | | | | | | |
| Small-Signal Bandwidth | G = +2, $V_O$ ≤ 0.5Vp-p | 110 | 77 | 65 | 58 | MHz | min | B |
| | G = +5, $V_O$ ≤ 0.5Vp-p | 39 | 24 | 20 | 19 | MHz | min | B |
| | G = +10, $V_O$ ≤ 0.5Vp-p | 16 | 12 | 10 | 8 | MHz | min | B |
| Gain Bandwidth Product | G ≥ +10 | 150 | 100 | 85 | 80 | MHz | min | B |
| Peaking at a Gain of +1 | $V_O$ ≤ 0.5Vp-p | 5 | — | — | — | dB | typ | C |
| Slew Rate | 1V Step | 215 | 160 | 123 | 82 | V/µs | min | B |
| Rise Time | 0.5V Step | 2.8 | 4.3 | 4.5 | 6.3 | ns | max | B |
| Fall Time | 0.5V Step | 3.0 | 4.4 | 4.6 | 6.0 | ns | max | B |
| Settling Time to 0.1% | 1V Step | 14 | 30 | 32 | 38 | ns | max | B |
| Spurious Free Dynamic Range | $V_O$ = 1Vp-p, f = 5MHz | 65 | 56 | 52 | 47 | dBc | min | B |
| Input Voltage Noise | f > 1MHz | 5.6 | 6.2 | 7.3 | 7.7 | nV/√Hz | max | B |
| Input Current Noise | f > 1MHz | 2.8 | 3.7 | 4.2 | 4.4 | pA/√Hz | max | B |
| **DC PERFORMANCE** | | | | | | | | |
| Open-Loop Voltage Gain | | 67 | **64** | 60 | 56 | dB | min | A |
| Input Offset Voltage | | 1.5 | **4** | 5 | 6 | mV | max | A |
| Average Offset Voltage Drift | | — | — | — | 46 | µV/°C | max | B |
| Input Bias Current | $V_{CM}$ = 1.0V | 25 | 42 | 55 | 60 | µA | max | B |
| Input Offset Current | $V_{CM}$ = 1.0V | 0.6 | 2 | 2.3 | 4 | µA | max | B |
| Input Offset Current Drift | | — | — | — | 40 | nA/°C | max | B |
| **INPUT** | | | | | | | | |
| Least Positive Input Voltage | | –0.25 | –0.1 | –0.05 | –0.01 | V | max | B |
| Most Positive Input Voltage | | 1.8 | **1.6** | 1.55 | 1.5 | V | min | A |
| Common-Mode Rejection (CMRR) | Input Referred | 75 | **67** | 64 | 61 | dB | min | A |
| Input Impedance | | | | | | | | |
| Differential-Mode | | 10 \|\| 2.1 | — | — | — | kΩ \|\| p | typ | C |
| Common-Mode | | 400 \|\| 1.2 | — | — | — | kΩ \|\| p | typ | C |
| **OUTPUT** | | | | | | | | |
| Least Positive Output Voltage | $R_L$ = 1kΩ to 1.5V | 0.035 | **0.043** | 0.045 | 0.06 | V | max | A |
| | $R_L$ = 150Ω to 1.5V | 0.06 | **0.08** | 0.09 | 0.13 | V | max | A |
| Most Positive Output Voltage | $R_L$ = 1kΩ to 1.5V | 2.9 | **2.86** | 2.85 | 2.45 | V | min | A |
| | $R_L$ = 150Ω to 1.5V | 2.8 | **2.70** | 2.69 | 2.65 | V | min | A |
| Current Output, Sourcing | | 45 | **35** | 30 | 12 | mA | min | A |
| Current Output, Sinking | | 65 | **30** | 27 | 10 | mA | min | A |
| Short Circuit Current (output shorted to either supply) | | 100 | — | — | — | mA | typ | C |
| Closed-Loop Output Impedance | Figure 2, f < 100kHz | 0.2 | — | — | — | Ω | typ | C |
| **DISABLE (OPA635 only)** | | | | | | | | |
| On Voltage (device enabled Low) | | 1.0 | **0.5** | 0.5 | 0.5 | V | min | A |
| Off Voltage (device disabled High) | | 1.8 | **1.9** | 2.1 | 2.2 | V | max | A |
| On Disable Current (DIS pin) | | 66 | **100** | 110 | 110 | µA | max | A |
| Off Disable Current (DIS pin) | | 0 | — | — | — | µA | typ | C |
| Disabled Quiescent Current | | 0 | **30** | 40 | 50 | µA | max | A |
| Disable Time | | 100 | — | — | — | ns | typ | C |
| Enable Time | | 60 | — | — | — | ns | typ | C |
| Off Isolation | f = 5MHz, Input to Output | 70 | — | — | — | dB | typ | C |
| **POWER SUPPLY** | | | | | | | | |
| Minimum Operating Voltage | | — | **2.7** | 2.7 | 2.7 | V | min | A |
| Maximum Operating Voltage | | — | **10.5** | 10.5 | 10.5 | V | max | A |
| Maximum Quiescent Current | | 10.8 | **11.1** | 11.4 | 11.6 | mA | max | A |
| Minimum Quiescent Current | | 10.8 | **10.1** | 8.6 | 8.0 | mA | min | A |
| Power Supply Rejection Ratio (PSRR) | Input Referred | 50 | **49** | 45 | 44 | dB | min | A |
| **THERMAL CHARACTERISTICS** | | | | | | | | |
| Specification: U, N | | –40 to +85 | | | | °C | typ | C |
| Thermal Resistance | | | | | | | | |
| U SO-8 | | 125 | | | | °C/W | typ | C |
| N SOT23-5, SOT23-6 | | 150 | | | | °C/W | typ | C |

NOTE: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | +11$V_{DC}$ |
| Internal Power Dissipation | See Thermal Analysis |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | –0.5 to +$V_S$ |
| Storage Temperature Range: P, U, N | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature ($T_J$) | +175°C |

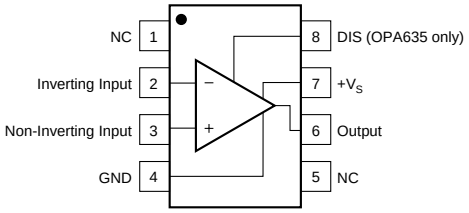
## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

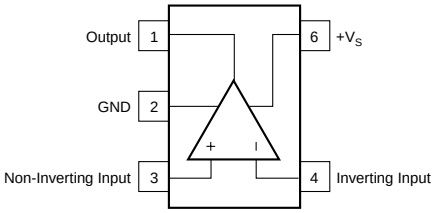
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

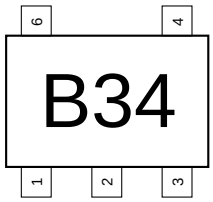
## PIN CONFIGURATIONS

**Top View—OPA634, OPA635** **SO-8**



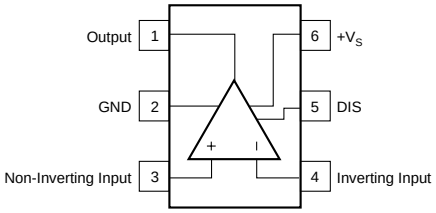

**Top View—OPA634** **SOT23-5**

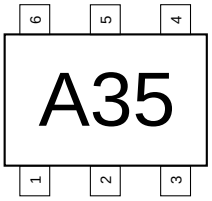



Pin Orientation/Package Marking

**Top View—OPA635** **SOT23-6**




Pin Orientation/Package Marking

## PACKAGE/ORDERING INFORMATION

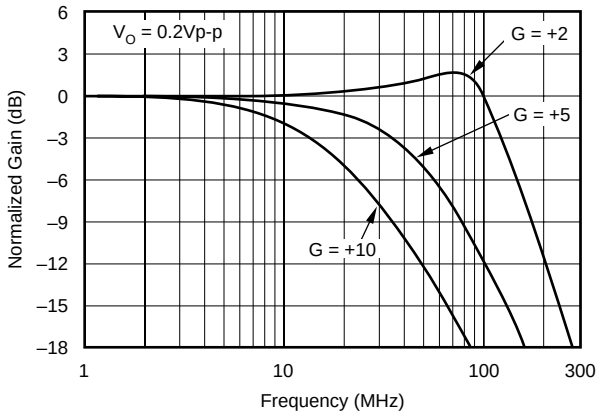
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER[1] | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| OPA635U | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA635U | OPA635U | Rails |
| " | " | " | " | " | OPA635U/2K5 | Tape and Reel |
| OPA635N | 6-Lead SOT23-6 | 332 | –40°C to +85°C | A35 | OPA635N/250 | Tape and Reel |
| " | " | " | " | " | OPA635N/3K | Tape and Reel |
| OPA634U | SO-8 Surface-Mount | 182 | –40°C to +85°C | OPA634U | OPA634U | Rails |
| " | " | " | " | " | OPA634U/2K5 | Tape and Reel |
| OPA634N | 5-Lead SOT23-5 | 331 | –40°C to +85°C | B34 | OPA634N/250 | Tape and Reel |
| " | " | " | " | " | OPA634N/3K | Tape and Reel |

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 3000 pieces of "OPA635N/3K" will get a single 3000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

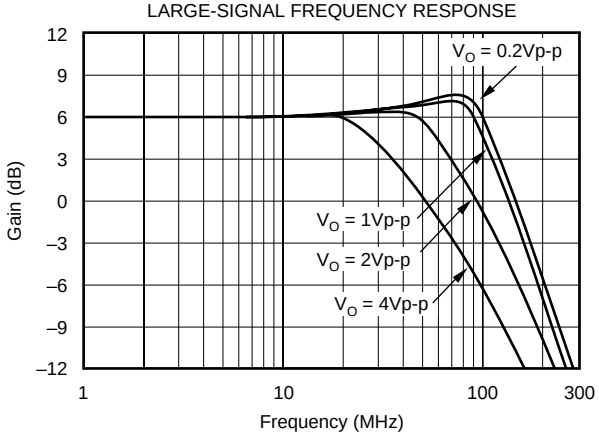
# TYPICAL PERFORMANCE CURVES: $V_S$ = +5V

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 1).

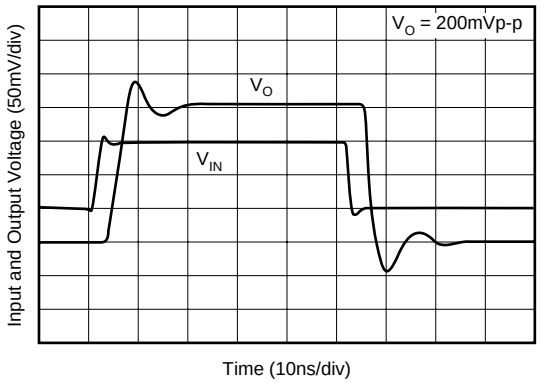
SMALL-SIGNAL FREQUENCY RESPONSE



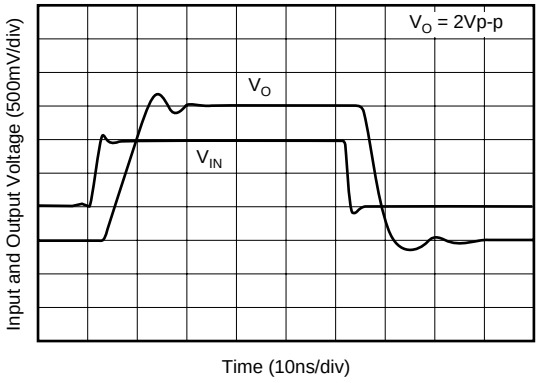

LARGE-SIGNAL FREQUENCY RESPONSE



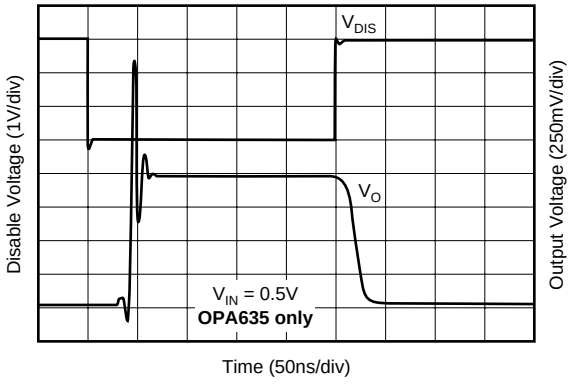

SMALL-SIGNAL PULSE RESPONSE



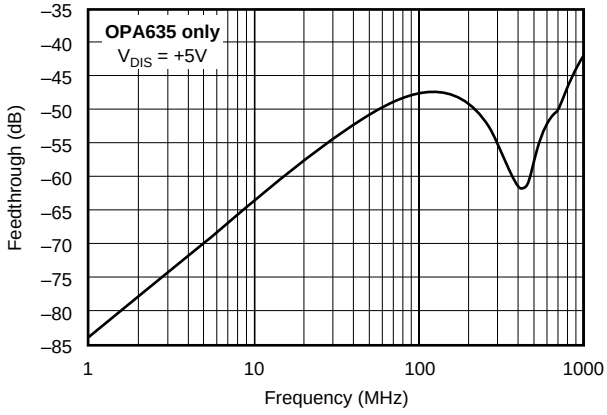

LARGE-SIGNAL DISABLE/ENABLE RESPONSE




LARGE-SIGNAL DISABLE/ENABLE RESPONSE



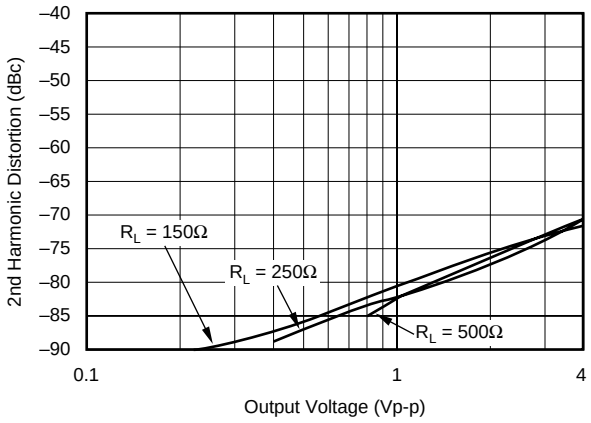

DISABLE FEEDTHROUGH vs FREQUENCY



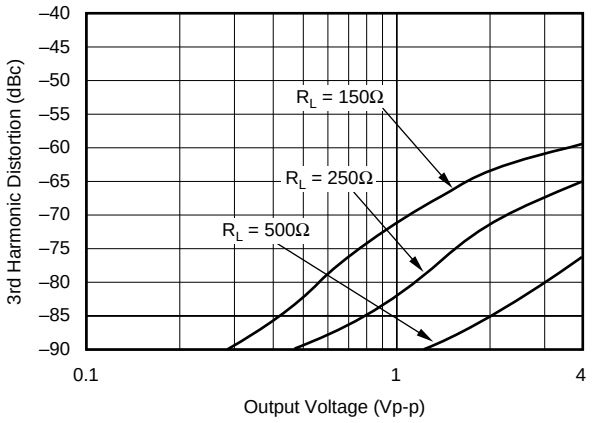
# TYPICAL PERFORMANCE CURVES: $V_S$ = +5V (CONT)

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 1).

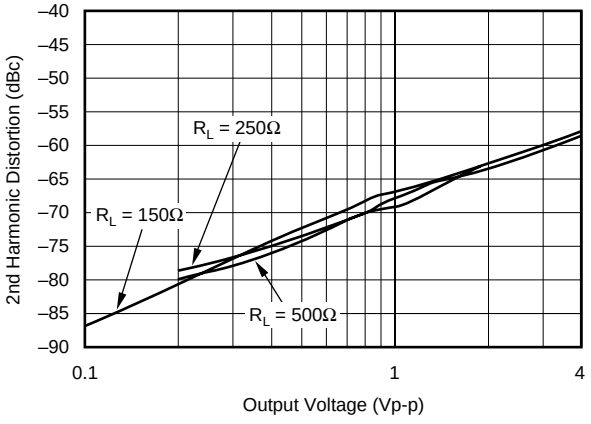
5MHz 2nd HARMONIC DISTORTION vs OUTPUT VOLTAGE



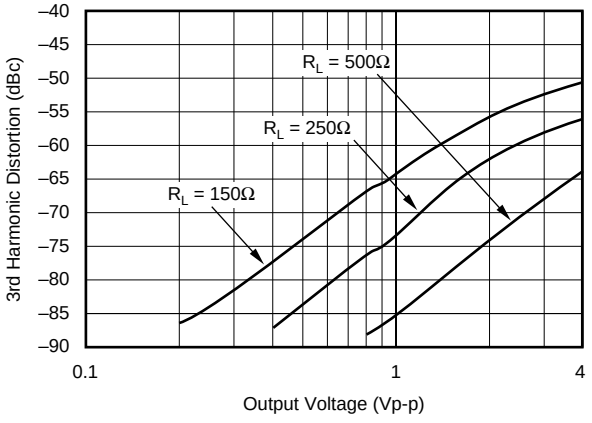

5MHz 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE



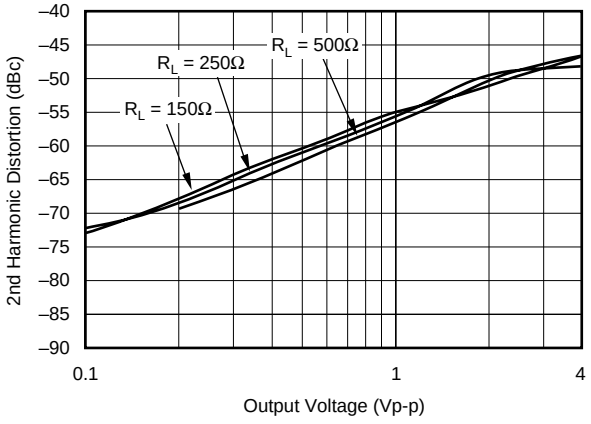

10MHz 2nd HARMONIC DISTORTION vs OUTPUT VOLTAGE



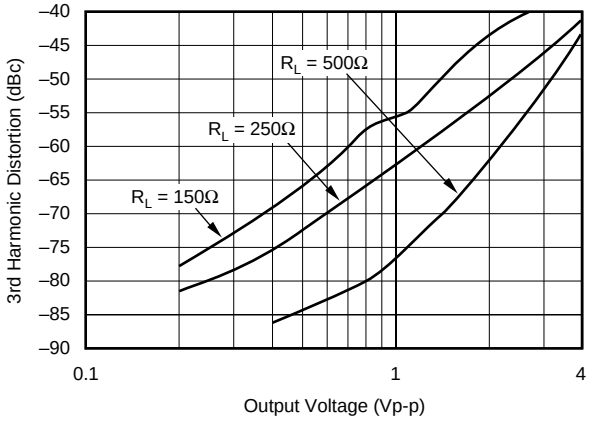

10MHz 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE




20MHz 2nd HARMONIC DISTORTION vs OUTPUT VOLTAGE



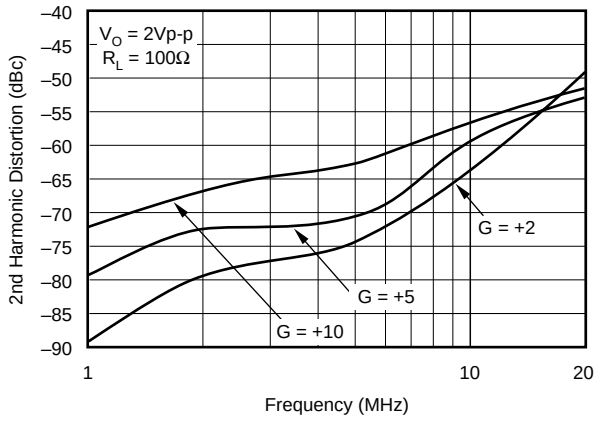

20MHz 3rd HARMONIC DISTORTION vs OUTPUT VOLTAGE



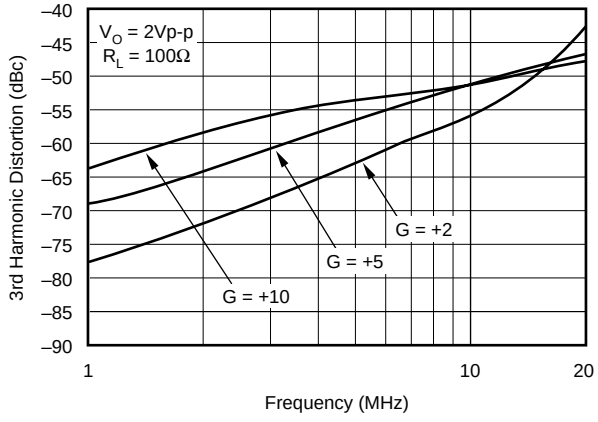
# TYPICAL PERFORMANCE CURVES: $V_S$ = +5V (CONT)

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 1).

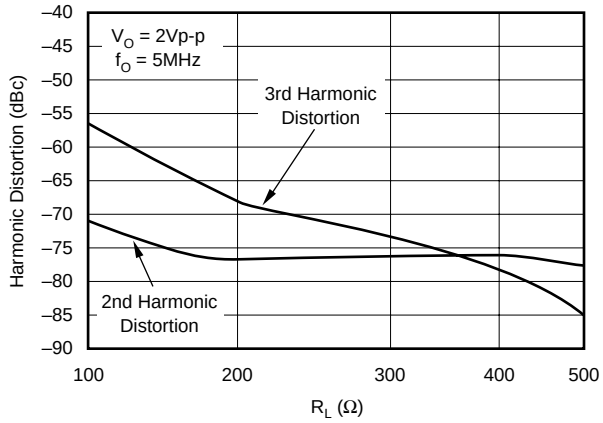
2nd HARMONIC DISTORTION vs FREQUENCY



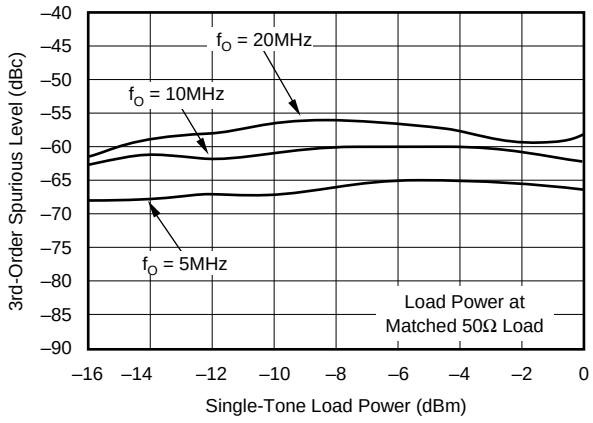

3rd HARMONIC DISTORTION vs FREQUENCY



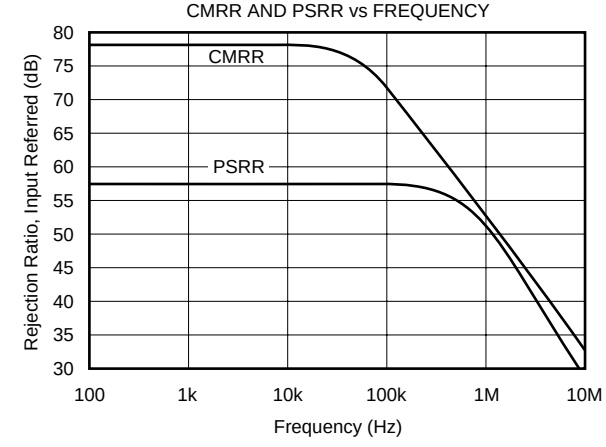

HARMONIC DISTORTION vs LOAD RESISTANCE



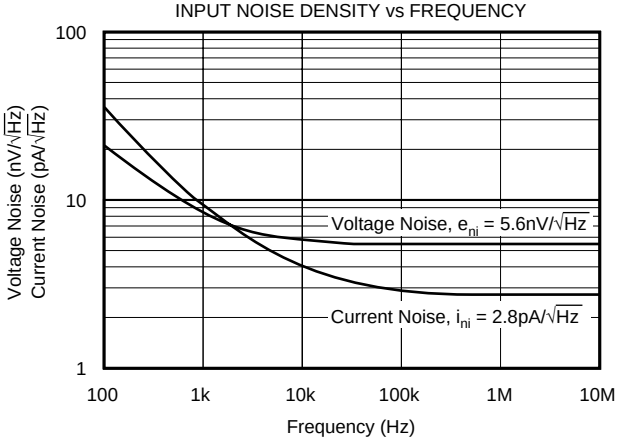

TWO-TONE, 3rd-ORDER INTERMODULATION SPURIOUS




CMRR AND PSRR vs FREQUENCY



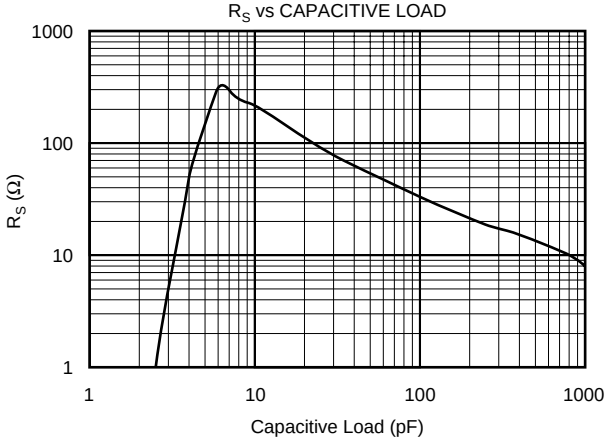

INPUT NOISE DENSITY vs FREQUENCY



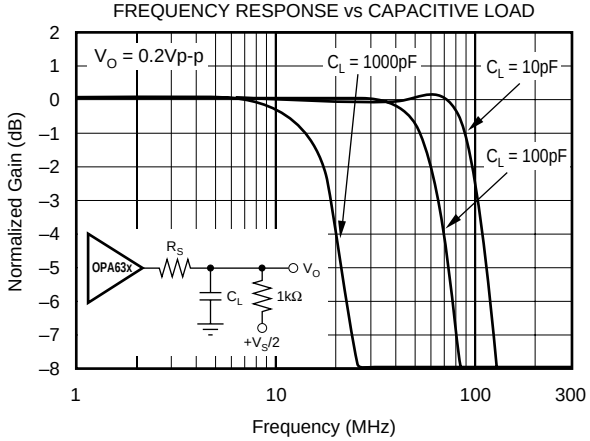
# TYPICAL PERFORMANCE CURVES: $V_S$ = +5V (CONT)

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 1).

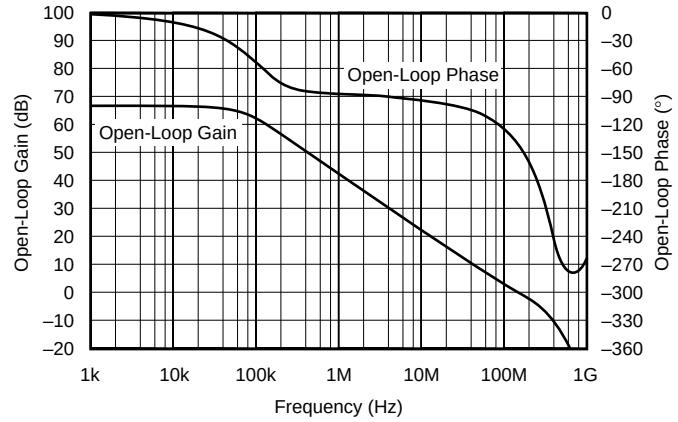
$R_S$ vs CAPACITIVE LOAD



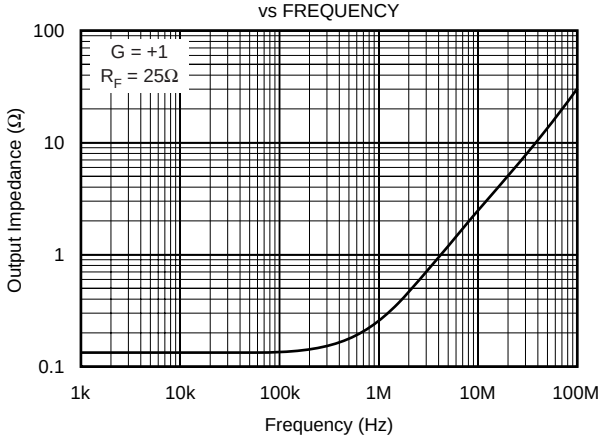

FREQUENCY RESPONSE vs CAPACITIVE LOAD



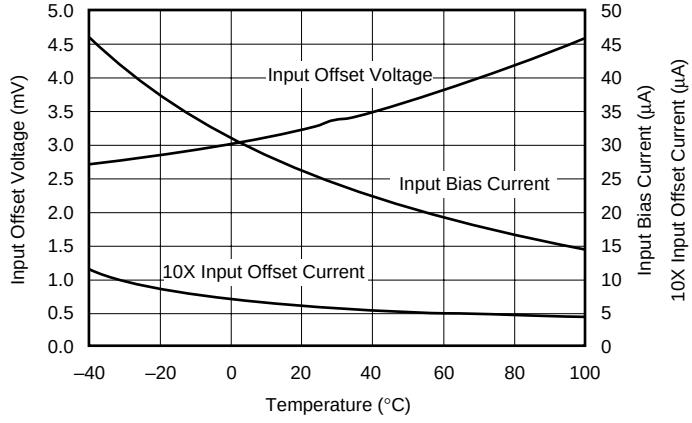

OPEN-LOOP GAIN AND PHASE



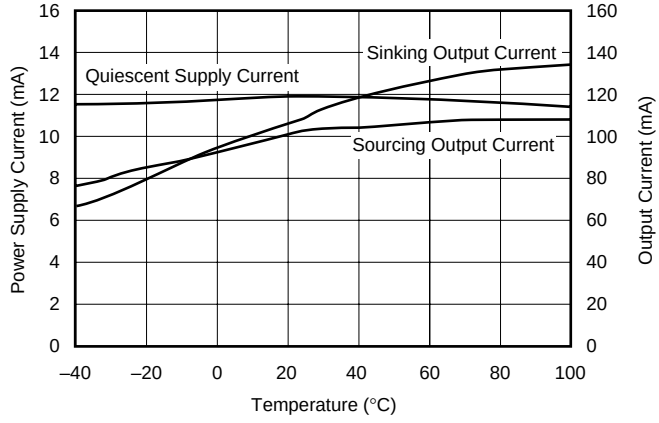

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY




INPUT DC ERRORS vs TEMPERATURE



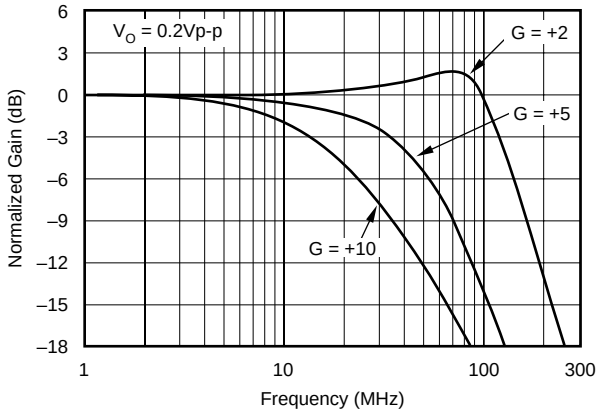

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



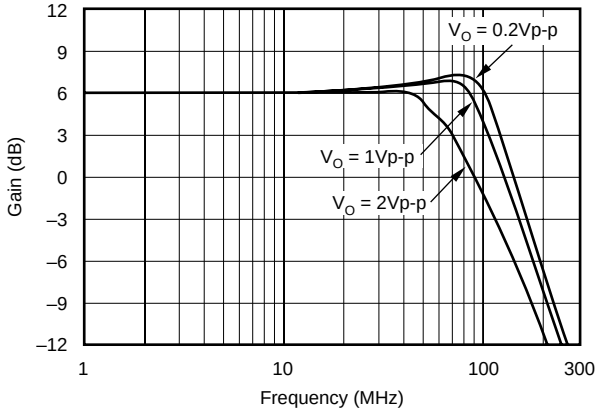
# TYPICAL PERFORMANCE CURVES: $V_S$ = +3V

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 2).

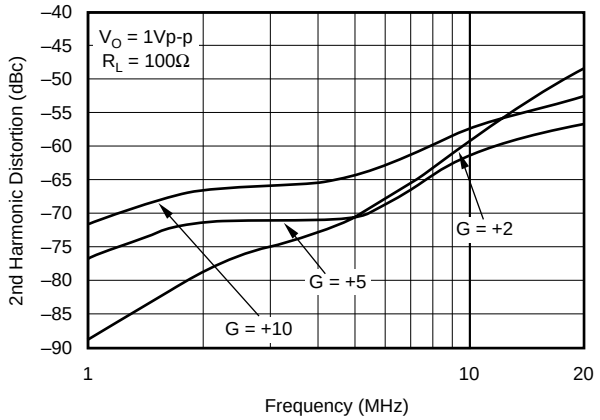
SMALL-SIGNAL FREQUENCY RESPONSE



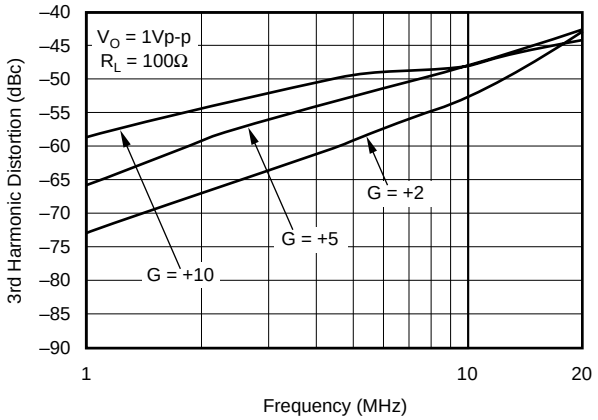

LARGE-SIGNAL FREQUENCY RESPONSE



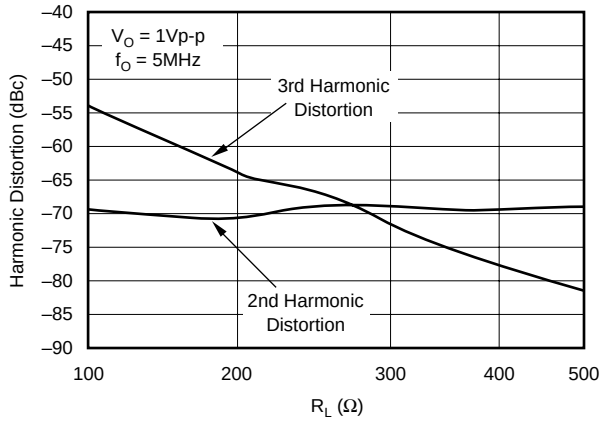

2nd HARMONIC DISTORTION vs FREQUENCY



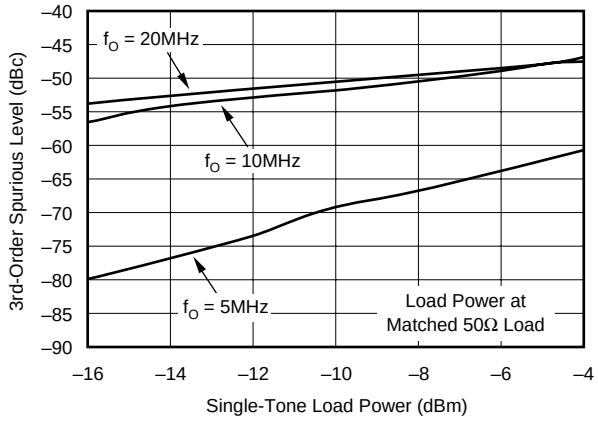

3rd HARMONIC DISTORTION vs FREQUENCY




HARMONIC DISTORTION vs LOAD RESISTANCE



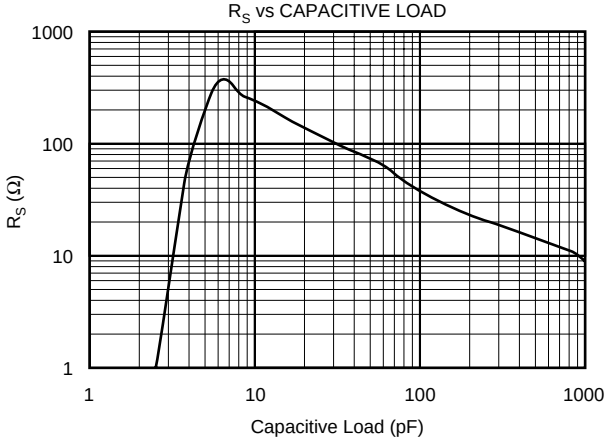

TWO-TONE, 3rd-ORDER INTERMODULATION SPURIOUS



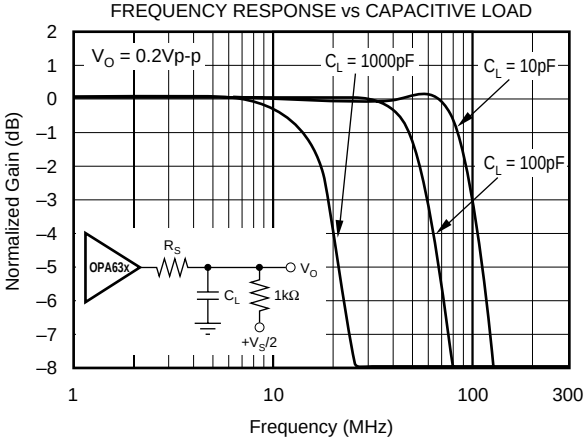
# TYPICAL PERFORMANCE CURVES: $V_S$ = +3V (CONT)

At $T_A$ = 25°C, G = +2, $R_F$ = 750Ω, and $R_L$ = 150Ω to $V_S$/2, unless otherwise noted (see Figure 2).

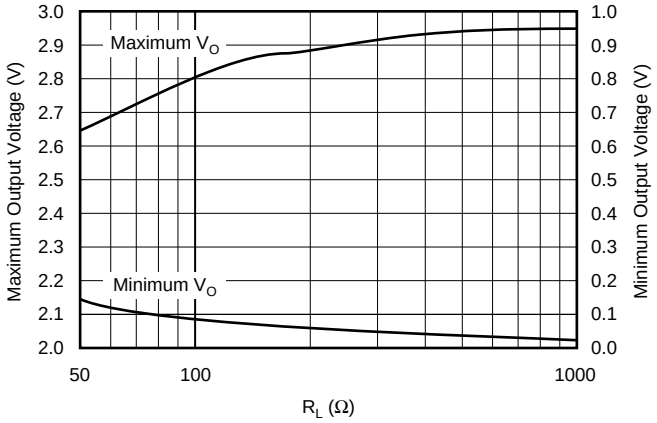
$R_S$ vs CAPACITIVE LOAD




FREQUENCY RESPONSE vs CAPACITIVE LOAD




OUTPUT SWING vs LOAD RESISTANCE



# APPLICATIONS INFORMATION

## WIDEBAND VOLTAGE FEEDBACK OPERATION

The OPA634 and OPA635 are unity-gain stable, very high speed voltage feedback op amps designed for single supply operation (+3V to +5V). The input stage supports input voltages below ground, and within 1.2V of the positive supply. The complementary common-emitter output stage provides an output swing to within 30mV of ground and 140mV of the positive supply. They are compensated to provide stable operation with a wide range of resistive loads. The OPA635's internal disable circuitry is designed to minimize supply current when disabled.

Figure 1 shows the AC-coupled, gain of +2 configuration used for the +5V Specifications and Typical Performance Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Specifications are taken directly at the input and output pins. For the circuit of Figure 1, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The disable pin needs to be driven by a low impedance source, such as a CMOS inverter. The 1.50kΩ resistors at the non-inverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input, minimizing the DC offset.

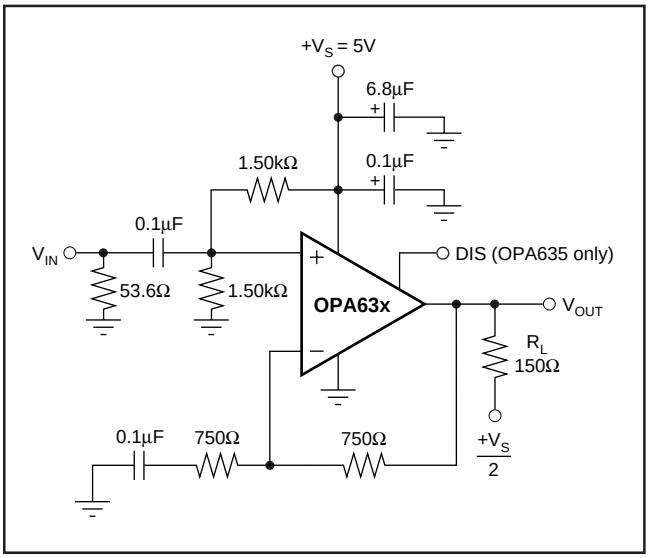



FIGURE 1. AC-Coupled Signal—Resistive Load to Supply Midpoint.

Figure 2 shows the DC-coupled, gain of +2 configuration used for the +3V Specifications and Typical Performance Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Though not strictly a "rail-to-rail" design, these parts come very close, while maintaining excellent performance. They will deliver ≤ 2.8Vp-p on a single +3V supply with 110MHz bandwidth. The 374Ω and 2.26kΩ resistors at the input level-shift $V_{IN}$ so that $V_{OUT}$ is within the allowed output voltage range when $V_{IN}$ = 0. See the Typical Performance Curves for information on driving capacitive loads.

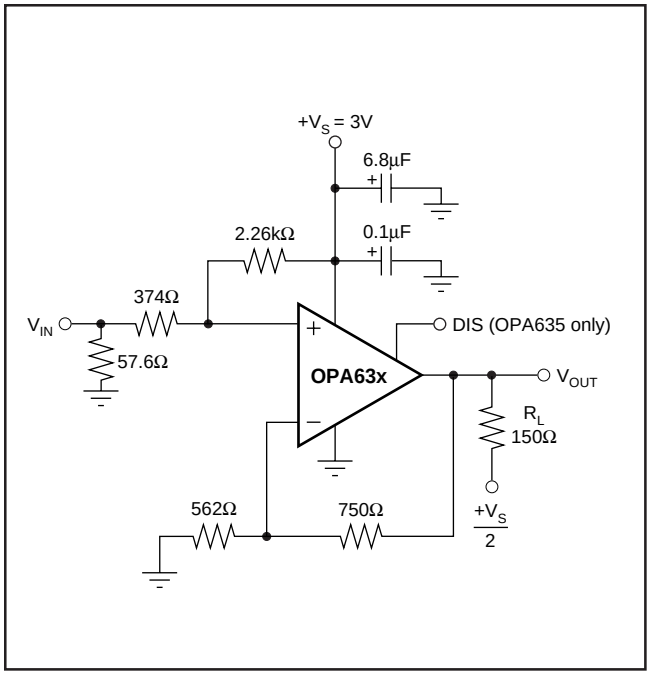



FIGURE 2. DC-Coupled Signal—Resistive Load to Supply Midpoint.

## SINGLE SUPPLY ADC CONVERTER INTERFACE

The front page shows a DC-coupled, single supply ADC driver circuit. Many systems are now requiring +3V supply capability of both the ADC and its driver. The OPA635 provides excellent performance in this demanding application. Its large input and output voltage ranges, and low distortion, support converters such as the ADS900 shown in this figure. The input level-shifting circuitry was designed so that $V_{IN}$ can be between 0V and 0.5V, while delivering an output voltage of 1V to 2V for the ADS900. Both the OPA635 and ADS900 have power reduction pins with the same polarity for those systems that need to conserve power.

## DC LEVEL SHIFTING

Figure 3 shows a DC-coupled non-inverting amplifier that level-shifts the input up to accommodate the desired output voltage range. Given the desired signal gain (G), and the amount $V_{OUT}$ needs to be shifted up ($\Delta V_{OUT}$) when $V_{IN}$ is at the center of its range, the following equations give the resistor values that produce the best DC offset.

$$NG = G + \Delta V_{OUT}/V_S$$

$$R_1 = R_4/G$$

$$R_2 = R_4/(NG - G)$$

$$R_3 = R_4/(NG - 1)$$

where:

$$NG = 1 + R_4/R_3$$

$$V_{OUT} = (G)V_{IN} + (NG - G)V_S$$

Make sure that $V_{IN}$ and $V_{OUT}$ stay within the specified input and output voltage ranges.

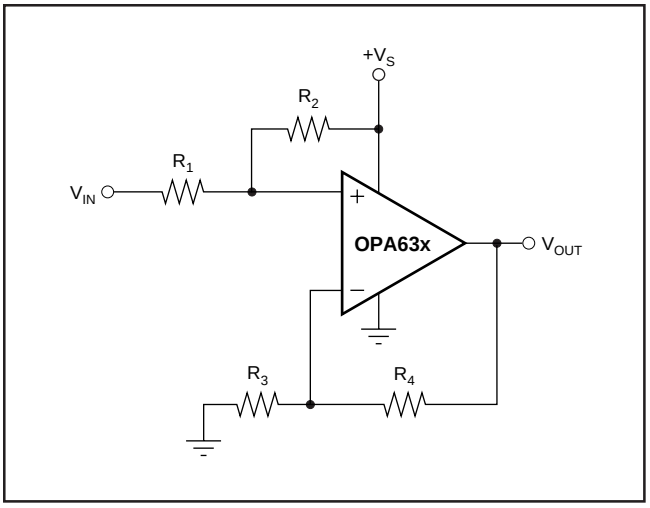



FIGURE 3. DC Level-Shifting Circuit.

The front page circuit is a good example of this type of application. It was designed to take $V_{IN}$ between 0V and 0.5V, and produce $V_{OUT}$ between 1V and 2V, when using a +3V supply. This means G = 2.00, and $\Delta V_{OUT}$ = 1.50V – G • 0.25V = 1.00V. Plugging into the above equations gives: NG = 2.33, $R_1$ = 375Ω, $R_2$ = 2.25kΩ, and $R_3$ = 563Ω. The resistors were changed to the nearest standard values.

### NON-INVERTING AMPLIFIER WITH REDUCED PEAKING

Figure 4 shows a non-inverting amplifier that reduces peaking at low gains. The resistor $R_C$ compensates the OPA634 or OPA635 to have higher Noise Gain (NG), which reduces the AC response peaking (typically 5dB at G = +1 without $R_C$) without changing the DC gain. $V_{IN}$ needs to be a low impedance source, such as an op amp. The resistor values are low to reduce noise. Using both $R_T$ and $R_F$ helps minimize the impact of parasitic impedances.

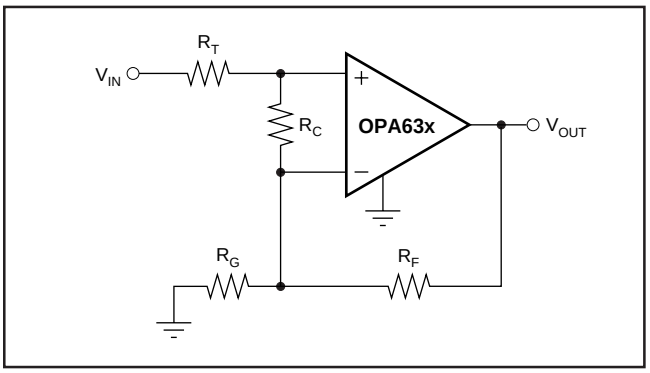



FIGURE 4. Compensated Non-Inverting Amplifier.

The Noise Gain can be calculated as follows:

$$G_1 = 1 + \frac{R_F}{R_G}$$

$$G_2 = 1 + \frac{R_T + R_F / G_1}{R_C}$$

$$NG = G_1 G_2$$

A unity gain buffer can be designed by selecting $R_T = R_F$ = 20.0Ω and $R_C$ = 40.2Ω (do not use $R_G$). This gives a Noise Gain of 2, so its response will be similar to the Characteristics Plots with G = +2. Decreasing $R_C$ to 20.0Ω will increase the Noise Gain to 3, which typically gives a flat frequency response, but with less bandwidth.

The circuit in Figure 1 can be redesigned to have less peaking by increasing the noise gain to 3. This is accomplished by adding $R_C$ = 2.55kΩ between the op amps inputs.

# DESIGN-IN TOOLS

### DEMONSTRATION BOARDS

Two PC boards are available to assist in the initial evaluation of circuit performance using the OPA634 and OPA635 in their three package styles. These are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown below:

| PRODUCT | PACKAGE | BOARD PART NUMBER | LITERATURE REQUEST NUMBER |
|---|---|---|---|
| OPA63xU<br>OPA63xN | 8-Pin SO-8<br>5-Pin SOT23-5<br>6-Pin SOT23-6 | DEM-OPA68xU<br>DEM-OPA6xxN | MKT-351<br>MKT-348 |

Contact the Burr-Brown Applications support line to request any of these boards.

# OPERATING SUGGESTIONS

### OPTIMIZING RESISTOR VALUES

Since the OPA634 and OPA635 are voltage feedback op amps, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a non-inverting unity gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short (see Figure 4). This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, for G > 1 application, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of $R_F$ and $R_G$ (Figure 1) to be less than approximately 400Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus, a zero in the forward response. Assuming a 3pF total parasitic on the inverting node, holding $R_F \parallel R_G$ <400Ω will keep this pole above 130MHz. By

itself, this constraint implies that the feedback resistor $R_F$ can increase to several kΩ at high gains. This is acceptable as long as the pole formed by $R_F$ and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

## BANDWIDTH VS GAIN: NON-INVERTING OPERATION

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the non-inverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factors), most amplifiers will exhibit a more complex response with lower phase margin. The OPA634 and OPA635 are compensated to give a slightly peaked response in a non-inverting gain of 2 (Figure 1). This results in a typical gain of +2 bandwidth of 150MHz, far exceeding that predicted by dividing the 140MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 16MHz bandwidth shown in the Typical Specifications is close to that predicted using the simple formula and the typical GBP.

The OPA634 and OPA635 exhibit minimal bandwidth reduction going to +3V single supply operation as compared with +5V supply. This is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

## INVERTING AMPLIFIER OPERATION

Since the OPA634 and OPA635 are general purpose, wideband voltage feedback op amps, all of the familiar op amp application circuits are available to the designer. Figure 5 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rate and distortion. It also allows the input to be biased at $V_S/2$ without any headroom issues. The output voltage can be independently moved to be within the output voltage range with coupling capacitors, or bias adjustment resistors.

In the inverting configuration, three key design consideration must be noted. The first is that the gain resistor ($R_G$) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace or other transmission line conductor), $R_G$ may be set equal to the required termination value and $R_F$ adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting $R_G$ to

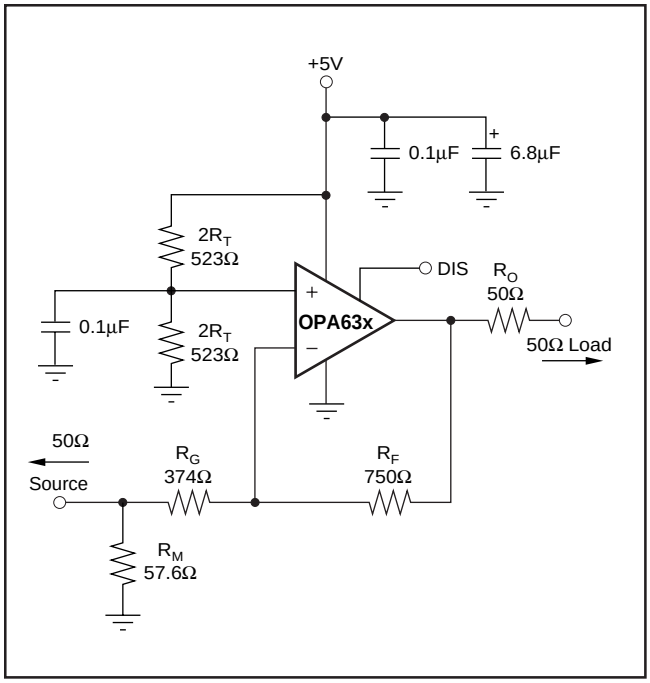



FIGURE 5. Gain of –2 Example Circuit.

50Ω for input matching eliminates the need for $R_M$ but requires a 100Ω feedback resistor. This has the interesting advantage that the noise gain becomes equal to 2 for a 50Ω source impedance—the same as the non-inverting circuits considered above. However, the amplifier output will now see the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the $R_F$ and $R_G$ values as shown in Figure 5, and then achieve the input matching impedance with a third resistor ($R_M$) to ground. The total input impedance becomes the parallel combination of $R_G$ and $R_M$.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For the example in Figure 5, the $R_M$ value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 576Ω = 26.8Ω. This impedance is added in series with $R_G$ for calculating the noise gain. The resultant is 2.87 for Figure 5, as opposed to only 2 if $R_M$ could be eliminated as discussed above. The bandwidth will therefore be lower for the gain of –2 circuit of Figure 5 (NG = +3) than for the gain of +2 circuit of Figure 1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistors on the non-inverting input (a parallel combination of $R_T$ = 263Ω). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC error, due to the input bias currents, will be reduced to (Input Offset Current) • $R_F$. If the 50Ω source impedance is DC-coupled in Figure 5, the total resistance to ground between the inverting input and the source will be 401Ω. Combining this in parallel with the feedback resistor gives the $R_T$ = 263Ω used in this

example. To reduce the additional high frequency noise introduced by this resistor, and power supply feedthrough, $R_T$ is bypassed with a capacitor. As long as $R_T < 400\Omega$, its noise contribution will be minimal. As a minimum, the OPA634 and OPA635 require an $R_T$ value of 50Ω to damp out parasitic-induced peaking—a direct short to ground on the non-inverting input runs the risk of a very high frequency instability in the input stage.

## OUTPUT CURRENT AND VOLTAGE

The OPA634 and OPA635 provide outstanding output voltage capability. Under no-load conditions at +25°C, the output voltage typically swings closer than 140mV to either supply rail; the guaranteed swing limit is within 450mV of either rail ($V_S$ = +5V).

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold start-up will the output current and voltage decrease to the numbers shown in the guaranteed tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their $V_{BE}$'s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power supply pin (8-pin packages) will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power supply leads. This will, under heavy output loads, reduce the available output voltage swing.

## DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter—including additional external capacitance which may be recommended to improve A/D linearity. A high speed, high open-loop gain amplifier like the OPA634 and OPA635 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Performance Curves show the recommended $R_S$ versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA634 and OPA635. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see Board Layout Guidelines).

The criterion for setting this $R_S$ resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of $R_S$ to flatten the response at the load. Increasing the noise gain will also reduce the peaking (see Figure 4).

## DISTORTION PERFORMANCE

The OPA634 and OPA635 provide good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic will dominate the distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the non-inverting configuration (Figure 1) this is sum of $R_F + R_G$, while in the inverting configuration, it is just $R_F$.

## NOISE PERFORMANCE

High slew rate, unity gain stable, voltage feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 5.6nV/$\sqrt{Hz}$ input voltage noise for the OPA634 and OPA635 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms (2.8pA/$\sqrt{Hz}$), combine to give low output noise under a wide variety of operating conditions. Figure 6 shows the op amp noise analysis model with all the noise terms included. In this

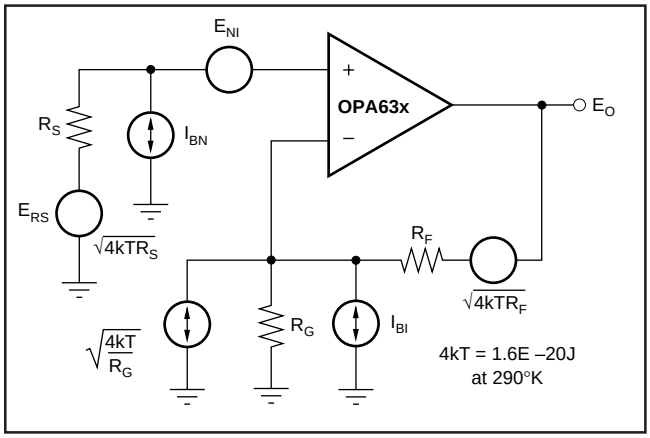



FIGURE 6. Noise Analysis Model.

model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 6.

**Equation 1:**

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1+$R_F/R_G$)) will give the equivalent input-referred spot noise voltage at the non-inverting input, as shown in Equation 2.

**Equation 2:**

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the circuit and component values shown in Figure 1 will give a total output spot noise voltage of 12.5nV/√Hz and a total equivalent input spot noise voltage of 6.3nV/√Hz. This is including the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 5.6nV/√Hz specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 400Ω, and the input attenuation is low. Since the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor ($R_T$) for the inverting op amp configuration of Figure 5 is not required.

## DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage feedback op amp allows good output DC accuracy in a wide variety of applications. The power supply current trim for the OPA634 and OPA635 gives even tighter control than comparable products. Although the high speed input stage does require relatively high input bias current (typically 25µA out of each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. This is done by matching the DC source resistances appearing at the two inputs. Evaluating the configuration of Figure 1 (which has matched DC input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to: (NG = non-inverting signal gain at DC)

$\pm(NG \bullet V_{OS(MAX)}) \pm (R_F \bullet I_{OS(MAX)})$
$= \pm(1 \bullet 7.0mV) \pm (750\Omega \bullet 2.0\mu A)$
$= \pm 8.5mV$

A fine scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques are based on adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be non-inverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the non-inverting input may be considered. Bring the DC offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

## DISABLE OPERATION

The OPA635 provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. To disable, the control pin must be asserted HIGH. Figure 7 shows a simplified internal circuit for the disable control feature.

In normal operation, base current to Q1 is provided through the 50kΩ resistor.

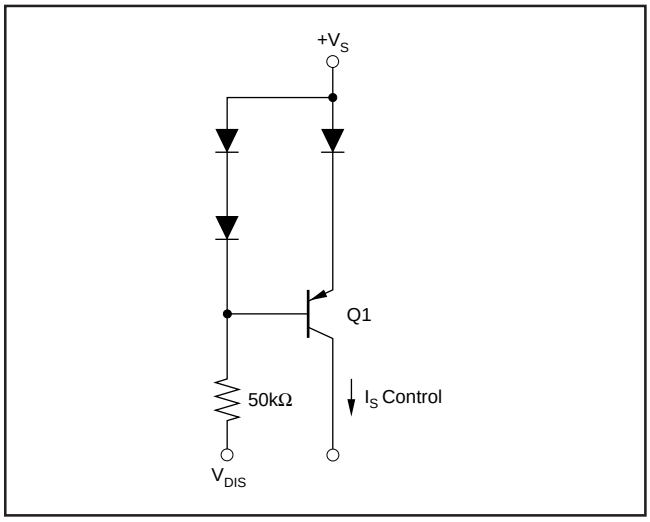



FIGURE 7. Simplified Disable Control Circuit (OPA635).

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode.

The transition edge rate (dv/dt) of the DIS control line will influence this glitch. Adding a simple RC filter into the DIS pin from a higher speed logic line will reduce the glitch. If extremely fast transition logic is used, a 1kΩ series resistor will provide adequate bandlimiting using just the parasitic input capacitance on the DIS pin while still ensuring adequate logic level swing.

## THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature ($T_J$) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation ($P_D$) is the sum of quiescent power ($P_{DQ}$) and additional power dissipated in the output stage ($P_{DL}$) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. $P_{DL}$ will depend on the required output signal and load but would, for resistive load connected to mid-supply ($V_S/2$), be at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(16 \bullet R_L)$, where $R_L$ includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum $T_J$ using an OPA635 (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a 150Ω load at mid-supply.

$P_D = 10V \bullet 13.25mA + 5^2/(16 \bullet (150\Omega \parallel 1500\Omega)) = 144mW$

Maximum $T_J = +85°C + (0.14W \bullet 150°C/W) = 107°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower guaranteed junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This puts a high current through a large internal voltage drop in the output transistors.

# BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA634 and OPA635 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

**a) Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

**b) Minimize the distance** (<0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

**c) Careful selection and placement of external components will preserve the high frequency performance.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values >1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the typical performance specifications is a good starting point for design. See Figure 4 for the unity gain follower application.

**d) Connections to other wideband devices** on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set $R_S$ from the plot of Recommended $R_S$ vs Capacitive Load. Low parasitic capacitive loads (<5pF) may not need an $R_S$ since the OPA634 and OPA635 are nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an $R_S$ are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is required, and the 6dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA634 and OPA635 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device;

this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Recommended $R_S$ vs Capacitive Load. This will not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

**e) Socketing a high speed part is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA634 and OPA635 onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g., McKenzie Technology #710C) can give good results.

## INPUT AND ESD PROTECTION

The OPA634 and OPA635 are is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 8.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA634 and OPA635), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

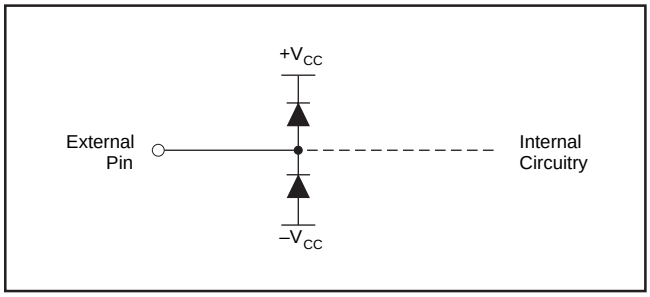



FIGURE 8. Internal ESD Protection.