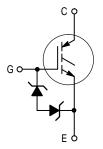
Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N-Channel Enhancement-Mode Silicon Gate

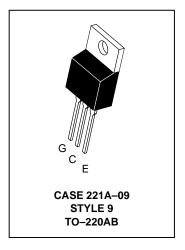
This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage—blocking capability. It also provides low on–voltage which results in efficient operation at high current.

- Industry Standard TO–220 Package
- High Speed E_{off}: 63 μJ/A typical at 125°C
- Low On-Voltage 1.7 V typical at 10 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes



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IGBT IN TO-220 20 A @ 90°C 31 A @ 25°C 600 VOLTS VERY LOW ON-VOLTAGE



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	VCES	600	Vdc
Collector–Gate Voltage (R _{GE} = 1.0 MΩ)	VCGR	600	Vdc
Gate-Emitter Voltage — Continuous	V _{GE}	±20	Vdc
Collector Current — Continuous @ T _C = 25°C — Continuous @ T _C = 90°C — Repetitive Pulsed Current (1)	IC25 IC90 ICM	31 20 62	Adc Apk
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	112 0.89	Watts W/°C
Operating and Storage Junction Temperature Range	TJ, T _{stg}	-55 to 150	°C
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	R _θ JC R _θ JA	1.12 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

⁽¹⁾ Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Ch	aracteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown \ (V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positiv	V(BR)CES	600 —	— 870	_	Vdc mV/°C	
Emitter–to–Collector Breakdown Voltage (V _{GE} = 0 Vdc, I _{EC} = 100 mAdc)		V _{(BR)ECS}	15	_	_	Vdc
Zero Gate Voltage Collector Curre (VCE = 600 Vdc, VGE = 0 Vdc) (VCE = 600 Vdc, VGE = 0 Vdc,	ICES	_		10 200	μAdc	
Gate-Body Leakage Current (VGE = ± 20 Vdc, VCE = 0 Vdc)		IGES	_	_	50	μAdc
ON CHARACTERISTICS (1)				•		•
Collector-to-Emitter On-State Vo (V _{GE} = 15 Vdc, I _C = 5.0 Adc) (V _{GE} = 15 Vdc, I _C = 5.0 Adc, T (V _{GE} = 15 Vdc, I _C = 10 Adc)	VCE(on)	_ _ _	1.4 1.3 1.7	1.7 — 2.0	Vdc	
Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1.0 mAdc) Threshold Temperature Coeffici	ent (Negative)	VGE(th)	3.0	5.0 10	7.0 —	Vdc mV/°C
Forward Transconductance (VCE	= 10 Vdc, I _C = 10 Adc)	9fe	_	7.0	_	Mhos
DYNAMIC CHARACTERISTICS				•		•
Input Capacitance		C _{ies}	_	1060	_	pF
Output Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{oes}	_	99	_	
Transfer Capacitance	1	C _{res}	_	15	_	
SWITCHING CHARACTERISTICS	(1)					
Turn-On Delay Time		td(on)	_	43	_	ns
Rise Time	$(V_{CC} = 360 \text{ Vdc}, I_{C} = 10 \text{ Adc},$	t _r	_	45	_]
Turn-Off Delay Time	V_{GE} = 15 Vdc, L = 300 μH, R_{G} = 20 Ω)	td(off)	_	144	_]
Fall Time	Energy losses include "tail"	t _f	_	175	_	
Turn-Off Switching Loss		E _{off}	_	340	_	μJ
Turn-On Delay Time		^t d(on)	_	43	_	ns
Rise Time	(V _{CC} = 360 Vdc, I _C = 10 Adc,	t _r	_	56	_	
Turn-Off Delay Time	V_{GE} = 15 Vdc, L = 300 μH, R_{G} = 20 Ω, T_{J} = 125°C) Energy losses include "tail"	t _d (off)	_	235	_	1
Fall Time		t _f	_	220	_	1
Turn-Off Switching Loss		E _{off}	_	625	_	μJ
Gate Charge	(V _{CC} = 360 Vdc, I _C = 10 Adc, V _{GE} = 15 Vdc)	QT	_	57	_	nC
		Q ₁	_	12	_	1
		Q ₂	_	25	_	
INTERNAL PACKAGE INDUCTAN	CE					
Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)		LE	_	7.5		nH

⁽¹⁾ Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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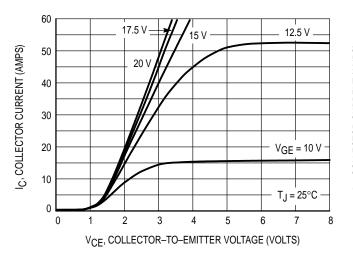


Figure 1. Output Characteristics

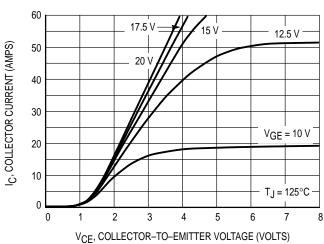


Figure 2. Output Characteristics

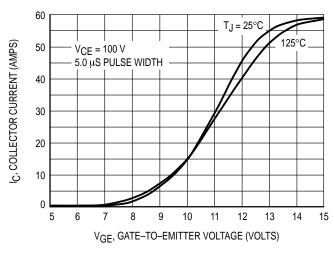


Figure 3. Transfer Characteristics

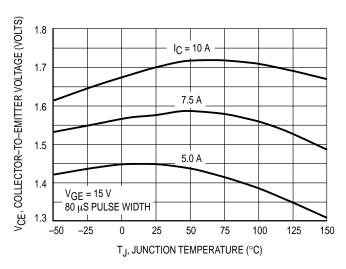


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

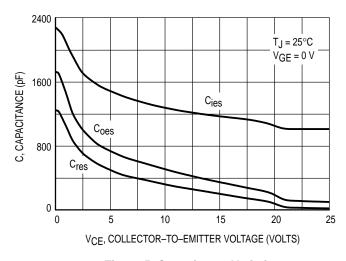


Figure 5. Capacitance Variation

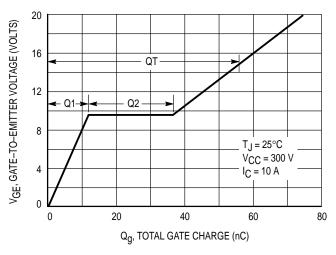


Figure 6. Gate-To-Emitter Voltage versus
Total Charge

Motorola IGBT Device Data 3

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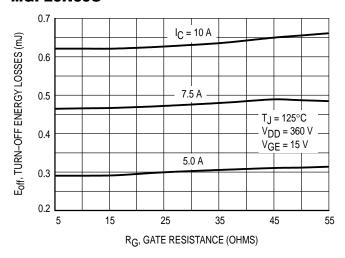


Figure 7. Turn-Off Energy Losses versus Gate Resistance

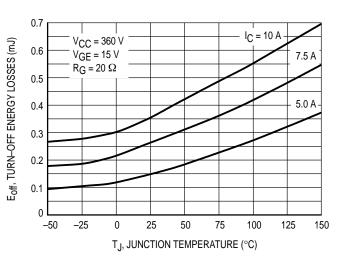


Figure 8. Turn-Off Energy Losses versus Junction Temperature

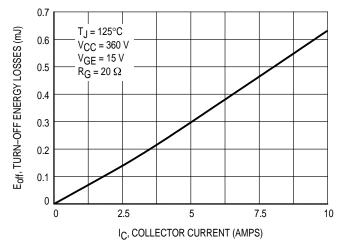


Figure 9. Turn-Off Energy Losses versus Collector Current

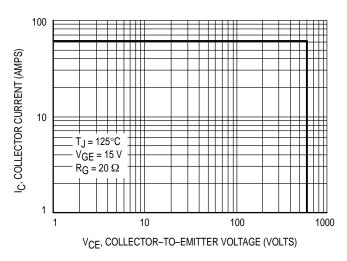
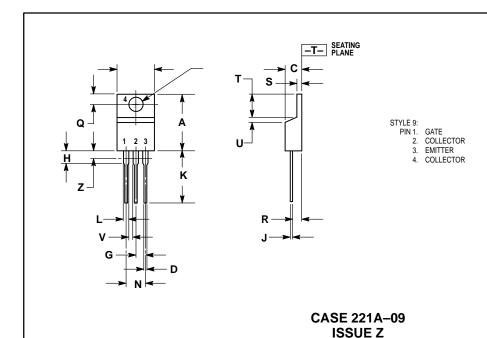


Figure 10. Reverse Biased Safe Operating Area

4 Motorola IGBT Device Data

PACKAGE DIMENSIONS



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
 DIMENSION Z DEFINES A ZONE WHERE ALL
 BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
7		0.080		2 04

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