

AO5800E

Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

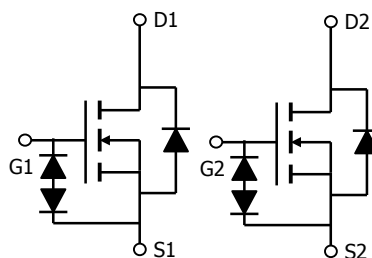
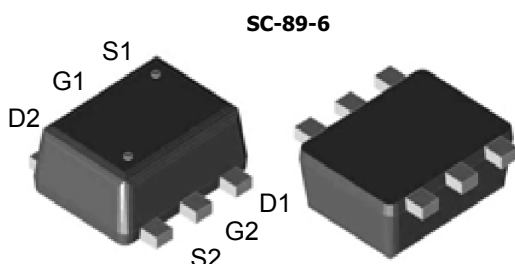
The AO5800E uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge, and operation with gate voltages as low as 4.5V, in the small SC89-6L footprint. It can be used for a wide variety of applications, including load switching, low current inverters and low current DC-DC converters. AO5800E and AO5800EL are electrically identical.

- RoHS compliant
- AO5800EL is Halogen Free

Features

- V_{DS} (V) = 60V
- I_D = 0.4A (V_{GS} = 10V)
- $R_{DS(ON)} < 1.6\Omega$ (V_{GS} = 10V)
- $R_{DS(ON)} < 1.9\Omega$ (V_{GS} = 4.5V)

ESD PROTECTED!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{A, F}	$T_A=25^\circ\text{C}$	0.4	A
	$T_A=70^\circ\text{C}$	0.3	
Pulsed Drain Current ^B	I_{DM}	1.6	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	0.4	W
	$T_A=70^\circ\text{C}$	0.24	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	275	330	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		360	450	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	300	350	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±10V V _{DS} =0V, V _{GS} =±4.5V			±1 ±100	μA nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	1.6	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	1.6			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =0.4A T _J =125°C V _{GS} =4.5V, I _D =0.3A		1.3 2.45 1.5	1.6 3 1.9	Ω Ω
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =0.4A		0.5		S
V _{SD}	Diode Forward Voltage	I _S =0.1A,V _{GS} =0V		0.8	1	V
I _S	Maximum Body-Diode Continuous Current				0.4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		41	50	pF
C _{oss}	Output Capacitance			9		pF
C _{rss}	Reverse Transfer Capacitance			6		pF
SWITCHING PARAMETERS						
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =75Ω, R _{GEN} =3Ω		39.2		ns
t _r	Turn-On Rise Time			35.7		ns
t _{D(off)}	Turn-Off DelayTime			261		ns
t _f	Turn-Off Fall Time			79		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =0.4A, dI/dt=100A/μs, V _{GS} =-9V		11.3	14	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =0.4A, dI/dt=100A/μs, V _{GS} =-9V		7.5		nC

A: The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

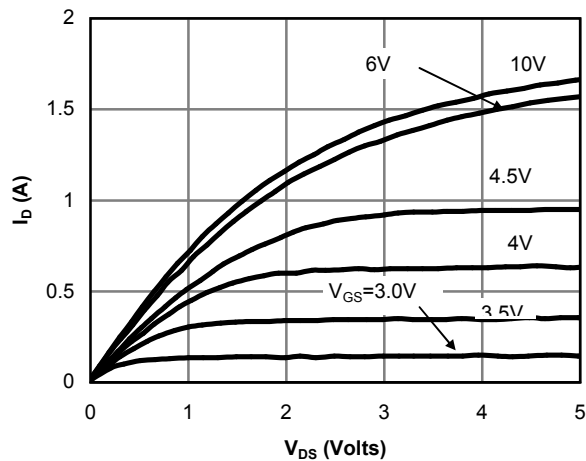


Figure 1: On-Region Characteristics

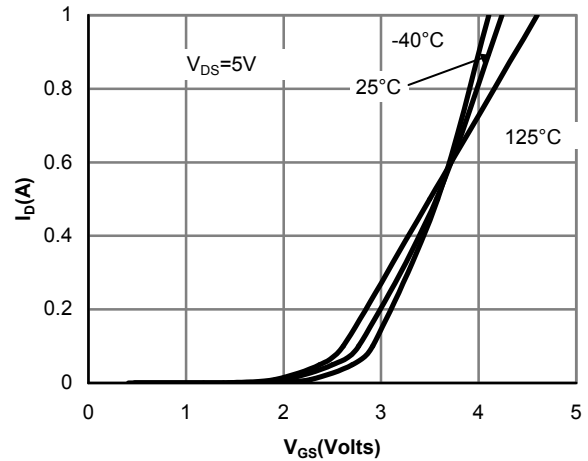


Figure 2: Transfer Characteristics

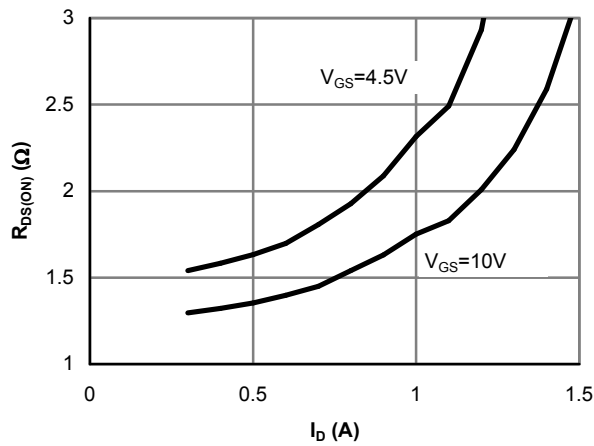


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

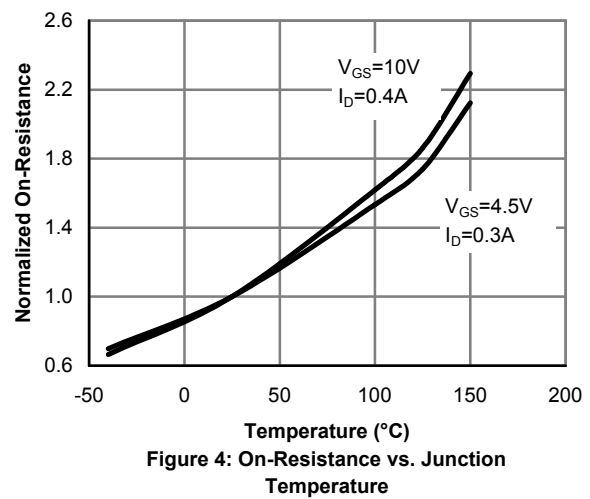


Figure 4: On-Resistance vs. Junction Temperature

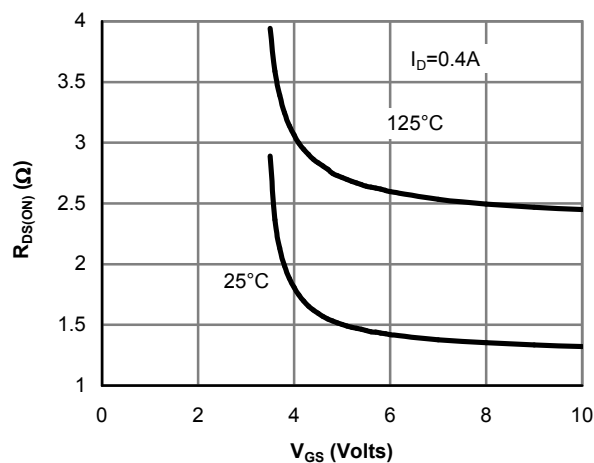


Figure 5: On-Resistance vs. Gate-Source Voltage

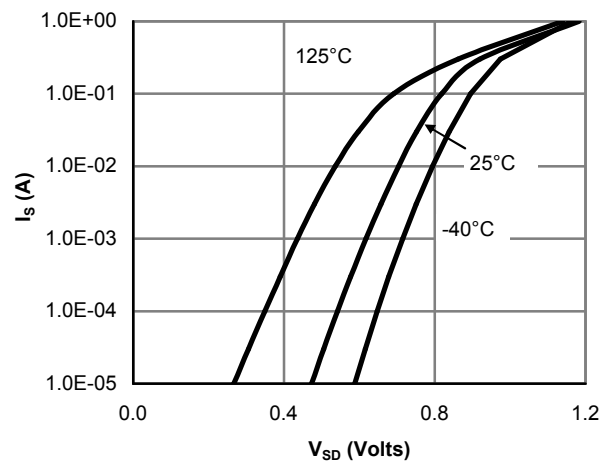


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

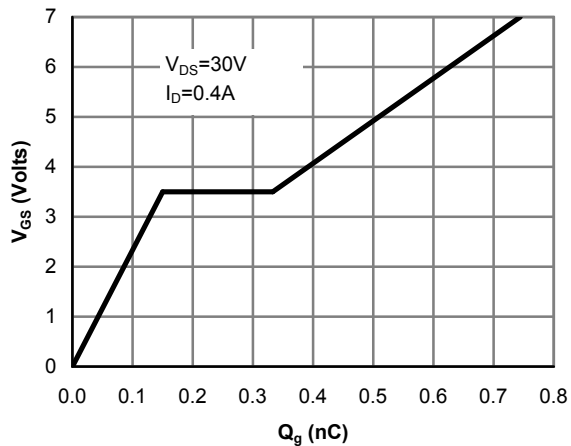


Figure 7: Gate-Charge Characteristics

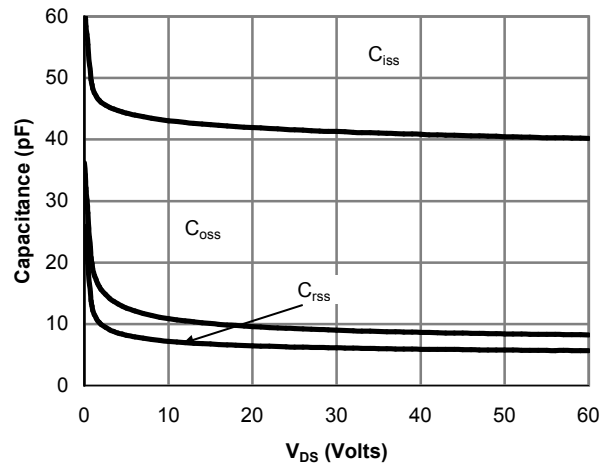


Figure 8: Capacitance Characteristics

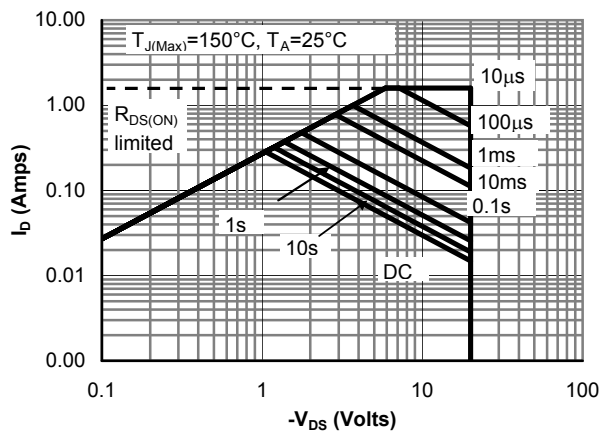


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

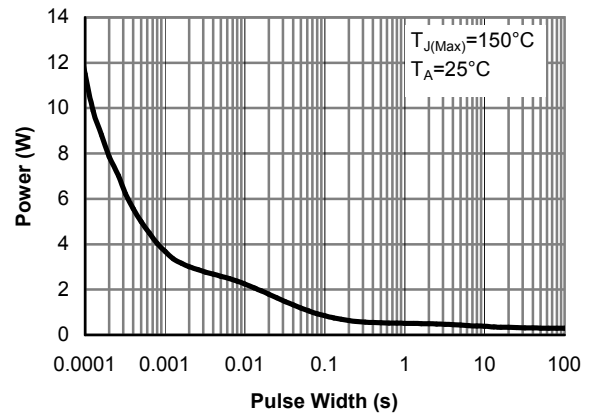


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

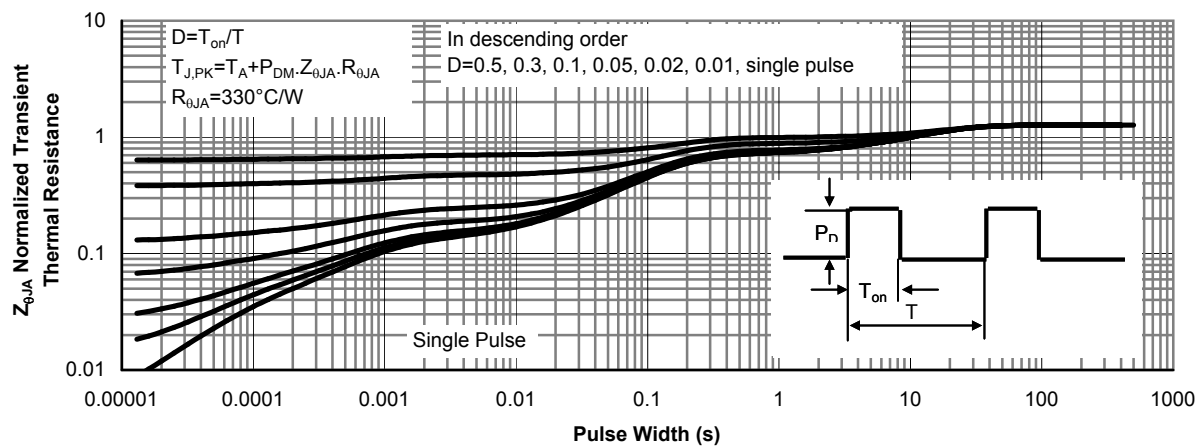
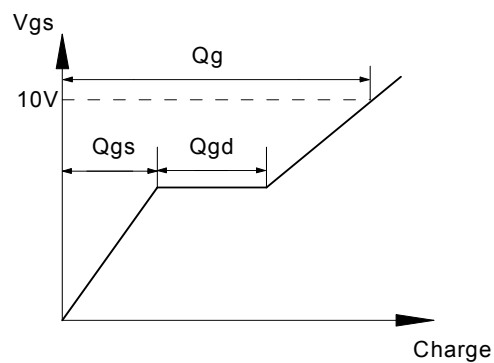
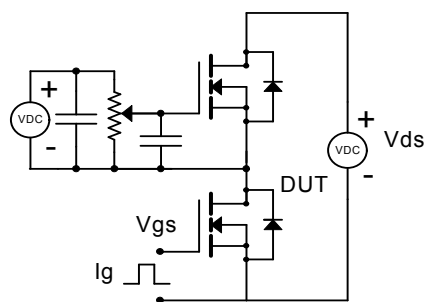
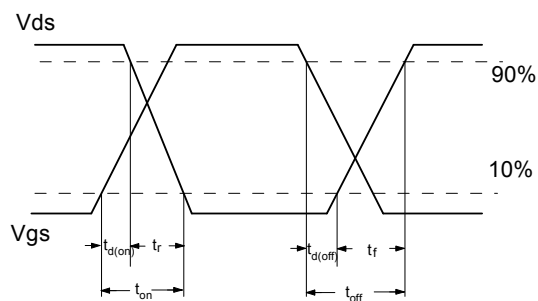
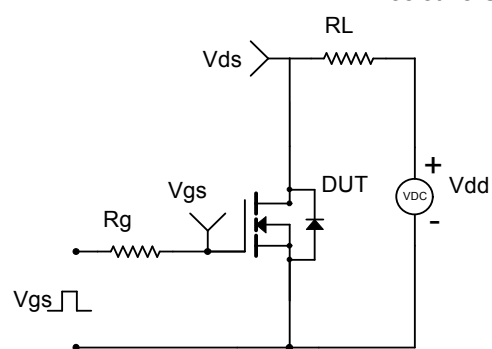


Figure 11: Normalized Maximum Transient Thermal Impedance

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

