

SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983—REVISED JANUARY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

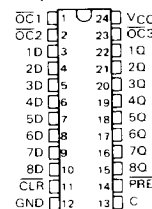
These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting $\bar{D}$ inputs. Since $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ are independent of the clock, taking the $\overline{\text{CLR}}$ input low will cause the eight Q outputs to go low. Taking the $\overline{\text{PRE}}$ input low will cause the eight Q outputs to go high. When both $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{\text{OC1}}$, $\overline{\text{OC2}}$, and $\overline{\text{OC3}}$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

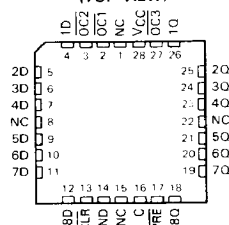
SN54ALS845, SN54AS845 . . . JT PACKAGE
SN74ALS845, SN74AS845 . . . DW OR NT PACKAGE

(TOP VIEW)



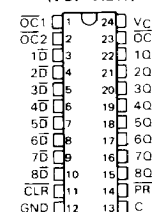
SN54ALS846, SN54AS846 . . . FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE

(TOP VIEW)



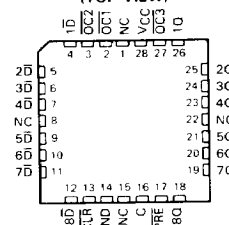
SN54ALS846, SN54AS846 . . . JT PACKAGE
SN74ALS846, SN74AS846 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS846, SN54AS846 . . . FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 **SN74ALS845, SN74AS845, SN74ALS846, SN74AS846** **8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

The -1 versions of the SN74ALS845 and SN74ALS846 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS845 and SN54ALS846.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C .

FUNCTION TABLES

'ALS845, 'AS845

INPUTS							OUTPUT
PRE	CLR	OC1	OC2	OC3	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'ALS846, 'AS846

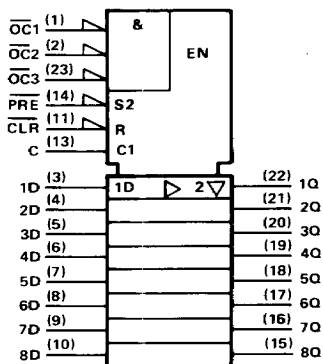
INPUTS							OUTPUT
PRE	CLR	OC1	OC2	OC3	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

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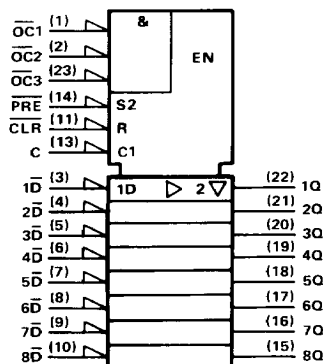
LSI Devices

logic symbols†

'ALS845, 'AS845



'ALS846, 'AS846



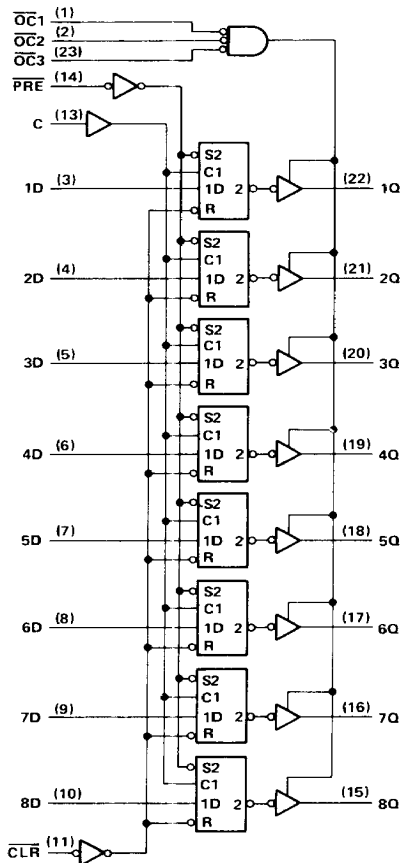
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

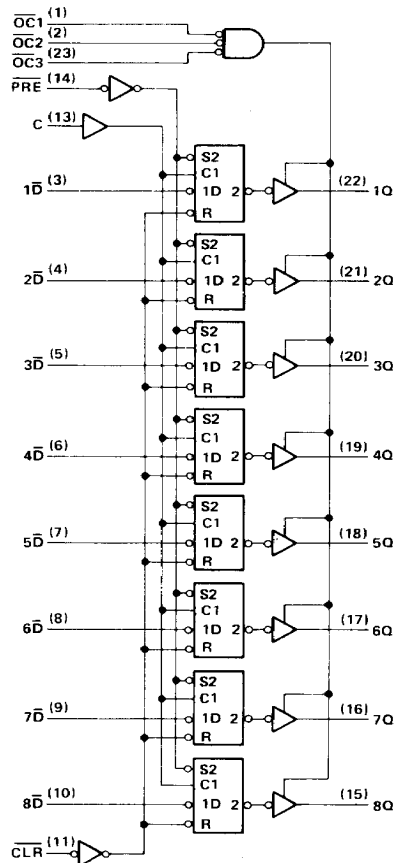
**SN54ALS845, SN54AS845, SN54ALS846, SN54AS846
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



Pin numbers shown are for D'W, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range:	
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846	-55°C to 125°C
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846	-0°C to 70°C
Storage temperature range	-65°C to 150°C

SN54ALS845, SN74ALS845

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54ALS845			SN74ALS845			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		-1			-2.6			mA
I _{OL}	Low-level output current		12			24			mA
			48†						
t _w	Pulse duration	CLR or PRE low	40			35			ns
		C high	25			20			
t _{su}	Setup time, data before enable C _I		16			10			ns
t _h	Hold time, data after enable C _I		7			5			ns
T _A	Operating free-air temperature		-55			0			70 °C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS845-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS845			SN74ALS845			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V _{CC} - 2			V
	V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4 3.3						
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA					2.4 3.2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25 0.4			0.25 0.4			V
	V _{CC} = 4.5 V, I _{OL} = 24 mA								
	(I _{OL} = 48 mA for .1 versions)					0.35 0.5			
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		20			20			µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		-20			-20			µA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			µA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		-0.1			-0.1			mA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V		-30 -112			-30 -112			mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	21 36		21 36				mA
		Outputs low	41 67		41 67				
		Outputs disabled	25 42		25 42				

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS845, SN74ALS845

8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS845			SN54ALS845		SN74ALS845		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q		7	11	2	15	2	13	ns
t _{PHL}				11	15	4	20	4	18	
t _{PLH}	C	Q		12	18	5	25	5	21	ns
t _{PHL}				16	23	8	30	8	26	
t _{PLH}	PRE	Q		13	19	5	25	6	22	ns
t _{PHL}				19	26	4	35	6	30	
t _{PLH}	CLR	Q		19	26	4	35	6	30	ns
t _{PHL}				16	22	6	28	6	24	
t _{PZH}	OC	Q		9	14	2	18	3	16	ns
t _{PZL}				12	17	4	20	5	18	
t _{PHZ}	OC	Q		4	9	1	12	1	11	ns
t _{PLZ}				6	11	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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recommended operating conditions

			SN54ALS846			SN74ALS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				− 1			− 2.6	mA
I _{OL}	Low-level output current				12			24	mA
								48†	
t _w	Pulse duration	CLR or PRE low							ns
		C high							
t _{su}	Setup time, data before enable C _I								ns
t _h	Hold time, data after enable C _I								ns
T _A	Operating free-air temperature		− 55		125	0		70	°C

† The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS846-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

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LSI Devices

PARAMETER	TEST CONDITIONS		SN54ALS846			SN74ALS846			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA				-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V _{CC} - 2			V
	V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4 3.3						
	V _{CC} = 4.5 V, I _{OH} = -2.6 mA					2.4 3.2			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25 0.4						V
	V _{CC} = 4.5 V, I _{OL} = 24 mA								
	I _{OL} = 48 mA for -1 versions)					0.35 0.5			
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		20			20			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		-20			-20			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		-0.1			-0.1			mA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V		-30		-112	-30		-112	mA
I _{CC}	V _{CC} = 5.5 V	Outputs high							mA
		Outputs low							
		Outputs disabled							

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS846			SN54ALS846		SN74ALS846		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH}	D	Q							ns	
t _{PHL}										
t _{PLH}	C	Q							ns	
t _{PHL}										
t _{PLH}	PRE	Q							ns	
t _{PHL}										
t _{PLH}	CLR	Q							ns	
t _{PHL}										
t _{PZH}	OC	Q							ns	
t _{PZL}										
t _{PHZ}	OC	Q							ns	
t _{PLZ}										

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

**SN54AS845, SN54AS846
SN74AS845, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

recommended operating conditions

			SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage					0.8			V
I _{OH}	High-level output current					- 24			mA
I _{OL}	Low-level output current					48			mA
t _w	Pulse duration	CLR or PRE low	5			4			ns
		C high	5			4			
t _{su}	Setup time, data before enable C _I		3.5			2.5			ns
t _h	Hold time, data after enable C _I		3.5			2.5			ns
t _r	Recovery time	PRE	17			15			ns
		CLR	16			14			
T _A	Operating free-air temperature		- 55			0			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

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LSI Devices

PARAMETER		TEST CONDITIONS		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V
V _{OH}		V _{CC} = 4.5 V,	I _{OH} = -2 mA	V _{CC} 2			V _{CC} -2			V
		V _{CC} = 4.5 V,	I _{OH} = -15 mA	2.4	3.2		2.4	3.2		
		V _{CC} = 4.5 V,	I _{OH} = -24 mA	2			2			
V _{OL}		V _{CC} = 4.5 V,	I _{OL} = 32 mA		0.25	0.5				V
		V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5	
I _{OZH}		V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μA
I _{OZL}		V _{CC} = 5.5 V,	V _O = 0.4 V			-50			-50	μA
I _I		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
I _{IH}		V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μA
I _{IL}		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
I _O ‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
I _{CC}	'AS845	V _{CC} = 5.5 V	Outputs high	35	58		35	58	mA	
			Outputs low	52	85		52	85		
	Outputs disabled		52	85		52	85			
	'AS846		Outputs high	36	59		36	59		
			Outputs low	53	87		53	87		
			Outputs disabled	53	87		53	87		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{O5}.

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SN54AS845, SN54AS846
SN74AS845, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX				UNIT
			SN54AS845		SN74AS845		
			MIN	MAX	MIN	MAX	
tPLH	D	Q	1	8.5	1	6.5	ns
tPHL			1	10	1	9	
tPLH	C	Q	2	13	2	12	ns
tPHL			2	13	2	12	
tPLH	PRE	Q	2	12	2	10	ns
tPHL	CLR	Q	2	14	2	13	ns
tPHL	OC	Q	2	13.5	2	10.5	ns
tPZL			2	15	2	13.5	
tPHZ	OC	Q	1	10	1	8	ns
tPLZ			1	10	1	8	

'AS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX				UNIT
			SN54AS846		SN74AS846		
			MIN	MAX	MIN	MAX	
tPLH	D	Q	1	11	1	8.5	ns
tPHL			1	11	1	10	
tPLH	C	Q	2	14	2	12.5	ns
tPHL			2	14	2	13	
tPLH	PRE	Q	2	12	2	10	ns
tPHL	CLR	Q	2	14.5	2	13.5	ns
tPHL	OC	Q	2	14.5	2	12	ns
tPZL			2	15	2	13.5	
tPHZ	OC	Q	1	10	1	8	ns
tPLZ			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 **SN74ALS845, SN74AS845, SN74ALS846, SN74AS846** **8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS**

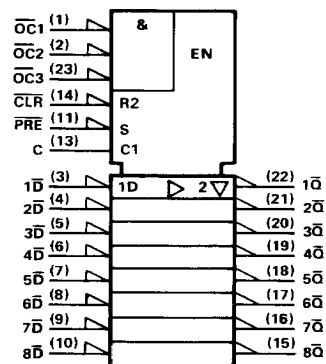
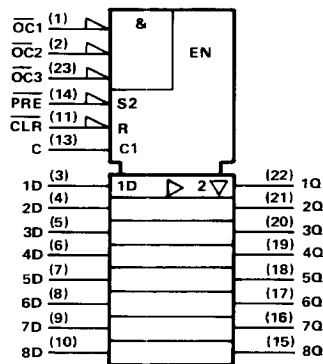
D latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\bar{Q}$. An input that causes a Q output to go high or a $\bar{Q}$ output to go low is called Preset; and input that causes a $\bar{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{\text{PRE}}$ and $\overline{\text{CLR}}$) if they are active low. The devices on this data sheet are second-source designs and the pin-name conventions used by the original manufacturer have been retained. That makes it necessary to designate the data inputs and outputs of the inverting circuit $\bar{D}$ and Q.

In some applications it may be advantageous to redesignate the inputs and outputs $\bar{D}$ and $\bar{Q}$ for the noninverting circuits or D and $\bar{Q}$ for the inverting circuits. In that case signal names should change as shown below. Also shown are corresponding changes in the logic symbols.

Notice that Q becoming $\bar{Q}$ causes $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ to exchange their names and their S and R function labels. The presence or absence of polarity indicators ($\triangle$) changes at the data inputs and outputs, but not at $\overline{\text{CLR}}/\overline{\text{PRE}}$, $\overline{\text{OC1}}$, $\overline{\text{OC2}}$, and $\overline{\text{OC3}}$ since these inputs are still active-low.

'ALS845, 'AS845



'ALS846, 'AS846

