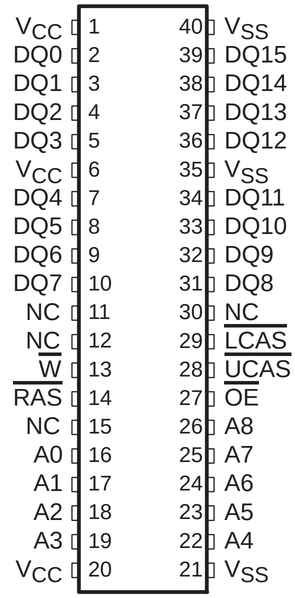
This data sheet is applicable to all TMS45160/Ps symbolized with Revision "D" and subsequent revisions as described on page 21.

- **Organization . . . 262 144 × 16**
- **5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

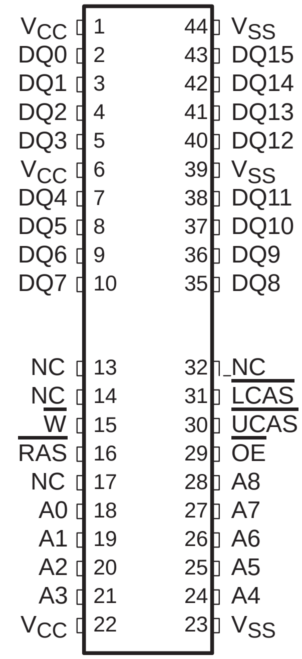
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45160/P-60	60 ns	15 ns	30 ns	110 ns
'45160/P-70	70 ns	20 ns	35 ns	130 ns
'45160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced-Page-Mode Operation With $\overline{\text{xCAS}}$-Before-$\overline{\text{RAS}}$ (xCBR) Refresh**
- **Long Refresh Period**
  512-Cycle Refresh in 8 ms (Max)
  64 ms Max for Low Power With Self-Refresh Version (TMS45160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs, and Clocks Are TTL Compatible**
- **High-Reliability, 40-Lead, 400-Mil-Wide Plastic Surface-Mount (SOJ) Package and 40/44-Lead Thin Small-Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low Power With Self-Refresh Version**
- **Upper and Lower Byte Control During Read and Write Operations**

DZ PACKAGE (TOP VIEW)



DGE PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0−A8	Address Inputs
DQ0−DQ15	Data In / Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

description

The TMS45160 series are high-speed, 4 194 304-bit dynamic random-access memories organized as 262 144 words of 16 bits each. The TMS45160P series are high-speed, low-power, self-refresh 4 194 304-bit dynamic random-access memories organized as 262 144 words of 16 bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 770 mW operating and 11 mW standby on 80-ns devices. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS45160 and TMS45160P are each offered in a 40-lead plastic surface-mount SOJ package (DZ suffix) and a 40/44-lead plastic surface-mount small-outline (TSOP) package (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

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operation

dual $\overline{\text{CAS}}$

Two $\overline{\text{CAS}}$ pins ($\overline{\text{LCAS}}$−$\overline{\text{UCAS}}$) are provided to give independent control of the 16 data I/O pins (DQ0−DQ15) with $\overline{\text{LCAS}}$ corresponding to DQ0−DQ7 and $\overline{\text{UCAS}}$ corresponding to DQ8−DQ15. For read or write cycles, the column address is latched on the first $\overline{\text{xCAS}}$ falling edge. Each $\overline{\text{xCAS}}$ going low enables its corresponding DQx pins with data associated with the column address latched on the first falling $\overline{\text{xCAS}}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{\text{xCAS}}$ edge.The delay time from $\overline{\text{xCAS}}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{\text{xCAS}}$ to its corresponding DQx pins.

In order to latch in a new column address, both $\overline{\text{xCAS}}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{\text{xCAS}}$ rising edge to the first falling $\overline{\text{xCAS}}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{\text{xCAS}}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{\text{xCAS}}$ must be brought low before the other $\overline{\text{xCAS}}$ is taken high.

For early-write cycles, the data is latched on the first falling edge of $\overline{\text{xCAS}}$. Only the DQs that have the corresponding $\overline{\text{xCAS}}$ low are written into. Each $\overline{\text{xCAS}}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, both $\overline{\text{xCAS}}$ pins must go high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{\text{RAS}}$ low time and the $\overline{\text{xCAS}}$ page-mode cycle time used. With minimum $\overline{\text{xCAS}}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{\text{RAS}}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{\text{RAS}}$. The buffers act as transparent or flow-through latches while $\overline{\text{xCAS}}$ is high. The first falling edge of $\overline{\text{xCAS}}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as column address is valid rather than when $\overline{\text{xCAS}}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after t_{RAH} (row-address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{\text{xCAS}}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{\text{xCAS}}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{\text{xCAS}}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{\text{xCAS}}$).

address (A0−A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on A0 through A8 and latched onto the chip by $\overline{\text{RAS}}$. Then, nine column-address bits are set up on A0 through A8 and latched onto the chip by the first $\overline{\text{xCAS}}$. All addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{xCAS}}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through $\overline{\text{W}}$. A logic high on $\overline{\text{W}}$ selects the read mode and a logic low selects the write mode. $\overline{\text{W}}$ can be driven from the standard TTL circuits without a pullup resistor. The data input lines are disabled when the read mode is selected. When $\overline{\text{W}}$ goes low prior to $\overline{\text{xCAS}}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{\text{OE}}$ grounded.

data in (DQ0−DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of xCAS or W strobes data into the on-chip data latch. In an early-write cycle, W is brought low prior to xCAS and the data is strobed in by the first occurring xCAS with setup and hold times referenced to data in. In a delayed-write or read-modify-write cycle, xCAS is already low and the data is strobed in by W with setup and hold times referenced to data in. In a delayed-write or read-modify-write cycle, OE must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0−DQ15)

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until xCAS and OE are brought low. In a read cycle, the output becomes valid after the access-time interval t_{CAC} (which begins with the negative transition of xCAS) as long as t_{RAC} and t_{AA} are satisfied.

output enable (OE)

OE controls the impedance of the output buffers. When OE is high, the buffers remain in the high-impedance state. Bringing OE low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both RAS and xCAS to be brought low for the output buffers to go into the low-impedance state. They remain in the low-impedance state until either OE or xCAS is brought high.

RAS-only refresh

A refresh operation must be performed at least once every 8 ms (64 ms for TMS45160P) to retain data. This can be achieved by strobing each of the 512 rows (A0−A8). A normal read or write cycle refreshes all bits in each row that is selected. A RAS-only operation can be used by holding all xCAS at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a RAS-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding xCAS at V_{IL} after a read operation and cycling RAS after a specified precharge period, similar to a RAS-only refresh cycle. The external address is ignored and the refresh address is generated internally.

xCAS-before-RAS (xCBR) refresh

xCBR refresh is utilized by bringing at least one xCAS low earlier than RAS (see parameter t_{CSR}) and holding it low after RAS falls (see parameter t_{CHR}). For successive xCBR refresh cycles, xCAS can remain low while cycling RAS. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500-µA refresh current is available on the TMS45160P. Data integrity is maintained using xCBR refresh with a period of 125 µs holding RAS low for less than 1 µs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \le 0.2$ V, $V_{IH} \ge V_{CC} - 0.2$ V).

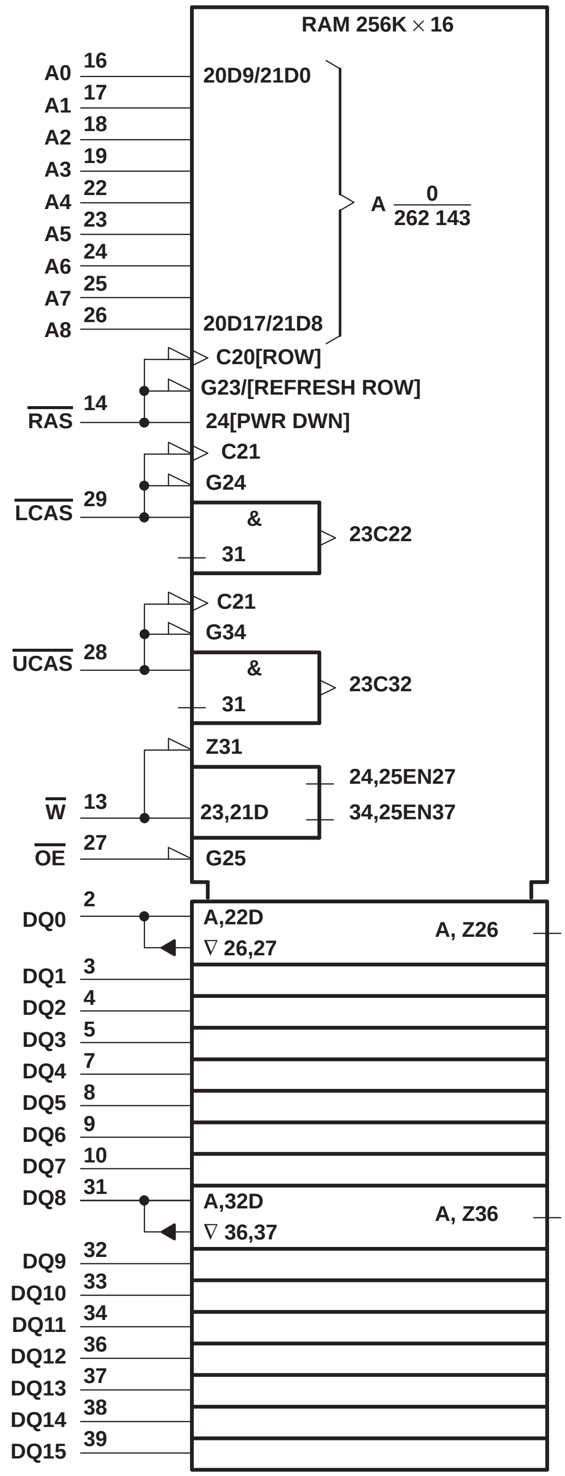
self refresh (TMS45160P)

The self-refresh mode is entered by dropping xCAS low prior to RAS going low. Then xCAS and RAS are both held low for a minimum of 100 µs. The chip is refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both RAS and xCAS are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures that the DRAM is fully refreshed.

power up

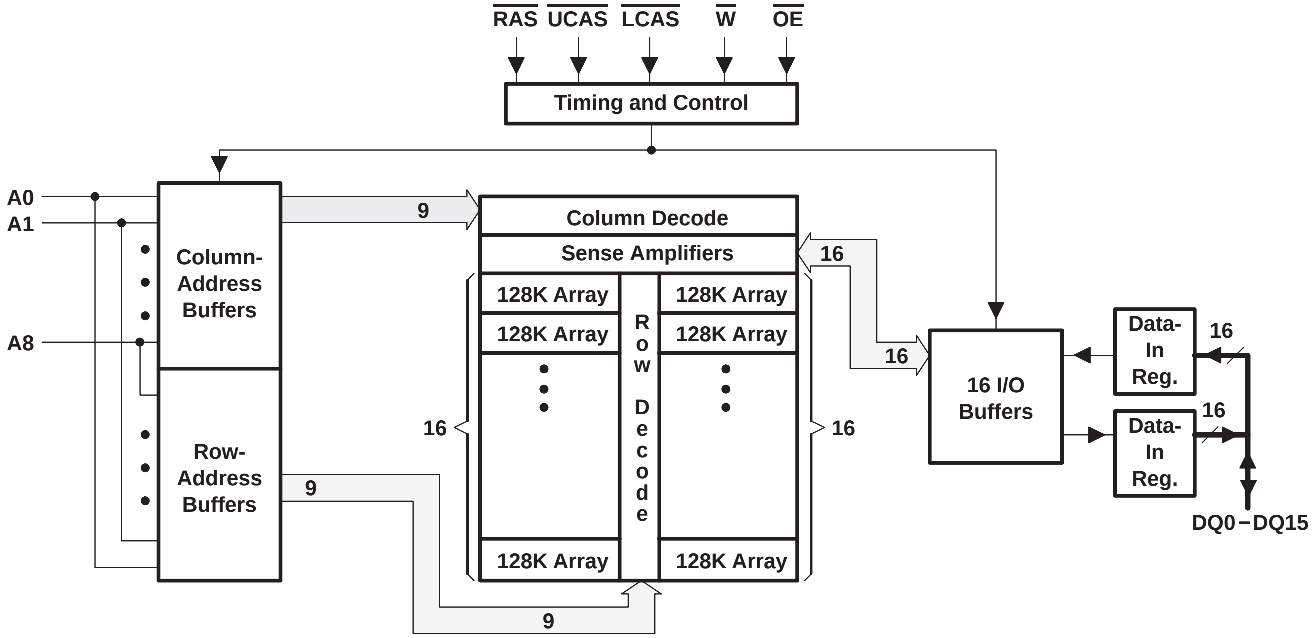
To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight $\overline{RAS}$ cycles is required after power up to the full V_{CC} level.These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or $\overline{xCBR}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	− 1 V to 7 V
Voltage range on any pin (see Note 1)	− 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	− 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	− 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'45160-60 '45160P-60		'45160-70 '45160P-70		'45160-80 '45160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{\text{CAS}}$ high			± 10		± 10		± 10	µA
I_{CC1}†§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle			180		160		140	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ high			2		2		2	mA
		$V_{IH} = V_{CC}$ − 0.2 V (CMOS), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ high	'45160		1		1		1	mA
			'45160P		350		350		350	µA
I_{CC3}‡	Average refresh current ($\overline{\text{RAS}}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, ($\overline{\text{RAS}}$ only), $\overline{\text{RAS}}$ cycling, $\overline{\text{xCAS}}$ high (CBR only), $\overline{\text{RAS}}$ low after $\overline{\text{xCAS}}$ low			180		160		140	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{\text{RAS}}$ low, $\overline{\text{xCAS}}$ cycling			160		140		120	mA
I_{CC5}¶	Battery-backup operating current (equivalent refresh time is 64 ms); CBR only	t_{RC} = 125 µs, $t_{RAS} \le$ 1 µs, V_{CC} − 0.2 V $\le V_{IH} \le$ 6.5 V, 0 V $\le V_{IL} \le$ 0.2 V, $\overline{\text{W}}$ and $\overline{\text{OE}}$ = V_{IH}, Address and data stable			500		500		500	µA
I_{CC6}†¶	Self-refresh current	$\overline{\text{xCAS}}$ < 0.2 V, $\overline{\text{RAS}}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			400		400		400	µA

† Measured with outputs open
‡ Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}
§ Measured with a maximum of one address change while $\overline{\text{xCAS}}$ = V_{IH}
¶ For TMS45160P only

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz# (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 − A8		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{\text{OE}}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{\text{W}}$		7	pF
C_o	Output capacitance		7	pF

Capacitance measurements are made on a sample basis only.
NOTE 3: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		’45160-60 ’45160P-60		’45160-70 ’45160P-70		’45160-80 ’45160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{\text{xCAS}}$ low		15		20		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{\text{RAS}}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{\text{OE}}$ low		15		20		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	Delay time, $\overline{\text{xCAS}}$ low to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{\text{xCAS}}$ high (see Note 4)	0	15	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{\text{OE}}$ high (see Note 4)	0	15	0	20	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		’45160-60 ’45160P-60		’45160-70 ’45160P-70		’45160-80 ’45160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 6)	110		130		150		ns
t_{WC}	Cycle time, write	110		130		150		ns
t_{RWC}	Cycle time, read-write/read-modify-write	155		185		205		ns
t_{PC}	Cycle time, page-mode read or write (see Note 7)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-modify-write	85		90		105		ns
t_{RASP}	Pulse duration, $\overline{\text{RAS}}$ low, page mode (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{\text{RAS}}$ low, nonpage mode (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{\text{xCAS}}$ low (see Note 9)	15	10 000	20	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{\text{xCAS}}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{\text{xCAS}}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{\text{W}}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{\text{xCAS}}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{\text{W}}$ low before $\overline{\text{xCAS}}$ high	15		20		20		ns
t_{RWL}	Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		20		20		ns
t_{WCS}	Setup time, $\overline{\text{W}}$ low before $\overline{\text{xCAS}}$ low (see Note 11)	0		0		0		ns

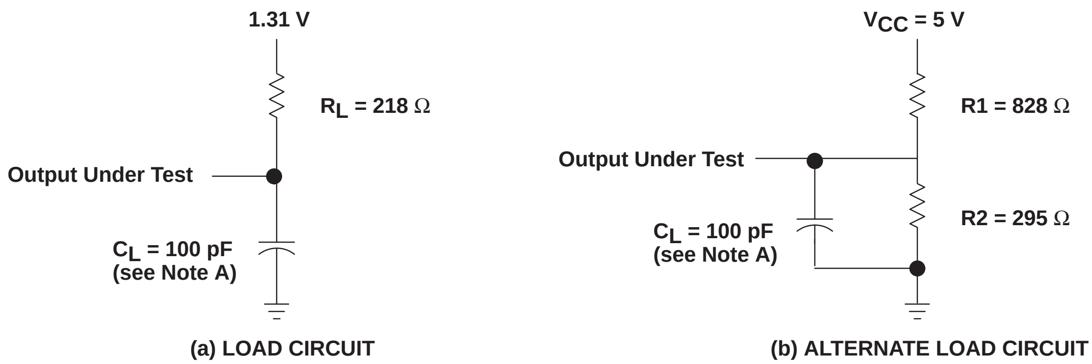
NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be $\geq t_{CP}$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ in write operations
11. Early-write operation only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

			’45160-60 ’45160P-60		’45160-70 ’45160P-70		’45160-80 ’45160P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{\text{xCAS}}$ low (see Note 10)		10		15		15		ns
t_{DHR}	Hold time, data after $\overline{\text{RAS}}$ low (see Note 12)		30		35		35		ns
t_{DH}	Hold time, data after $\overline{\text{xCAS}}$ low (see Note 10)		10		15		15		ns
t_{AR}	Hold time, column address after $\overline{\text{RAS}}$ low (see Note 12)		30		35		35		ns
t_{RAH}	Hold time, row address after $\overline{\text{RAS}}$ low		10		10		10		ns
t_{RCH}	Hold time, read after $\overline{\text{xCAS}}$ high (see Note 13)		0		0		0		ns
t_{RRH}	Hold time, read after $\overline{\text{RAS}}$ high (see Note 13)		0		0		0		ns
t_{WCH}	Hold time, write after $\overline{\text{xCAS}}$ low (see Note 13)		10		15		15		ns
t_{WCR}	Hold time, write after $\overline{\text{RAS}}$ low (see Note 14)		30		35		35		ns
t_{CLCH}	Hold time, $\overline{\text{xCAS}}$ low to $\overline{\text{xCAS}}$ high		5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{\text{W}}$ low (see Note 15)		55		65		70		ns
t_{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{xCAS}}$ high (see Note 11)		15		15		20		ns
t_{CRP}	Delay time, $\overline{\text{xCAS}}$ high to $\overline{\text{RAS}}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{xCAS}}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{\text{xCAS}}$ low to $\overline{\text{RAS}}$ low (see Note 11)		10		10		10		ns
t_{CWD}	Delay time, $\overline{\text{xCAS}}$ low to $\overline{\text{W}}$ low (see Note 15)		40		50		50		ns
t_{OEH}	Hold time, $\overline{\text{OE}}$ command		15		20		20		ns
t_{OED}	Delay time, $\overline{\text{OE}}$ high before data at DQ		15		20		20		ns
t_{ROH}	Delay time, $\overline{\text{OE}}$ low to $\overline{\text{RAS}}$ high		10		10		10		ns
t_{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 16)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{\text{xCAS}}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{xCAS}}$ low (see Note 16)		20	45	20	50	20	60	ns
t_{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{xCAS}}$ low (see Note 11)		0		0		0		ns
t_{RSH}	Delay time, $\overline{\text{xCAS}}$ low to $\overline{\text{RAS}}$ high		15		20		20		ns
t_{RWD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (see Note 15)		85		100		110		ns
t_{CPR}	Pulse duration, $\overline{\text{xCAS}}$ precharge before self refresh		0		0		0		ns
t_{RPS}	Pulse duration, $\overline{\text{RAS}}$ precharge after self refresh		110		130		150		ns
t_{RASS}	Pulse duration, self refresh entry from $\overline{\text{RAS}}$ low		100		100		100		µs
t_{CHS}	Hold time, $\overline{\text{xCAS}}$ low after $\overline{\text{RAS}}$ high (for self refresh)		− 50		− 50		− 50		ns
t_{REF}	Refresh time interval	’45160		8		8		8	ms
		’45160P		64		64		64	
t_T	Transition time		2	50	2	50	2	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Referenced in the later of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ in write operations.
11. Early-write operation only
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. xCBR refresh only
15. Read-modify-write operation only
16. Maximum value specified only to assure access time

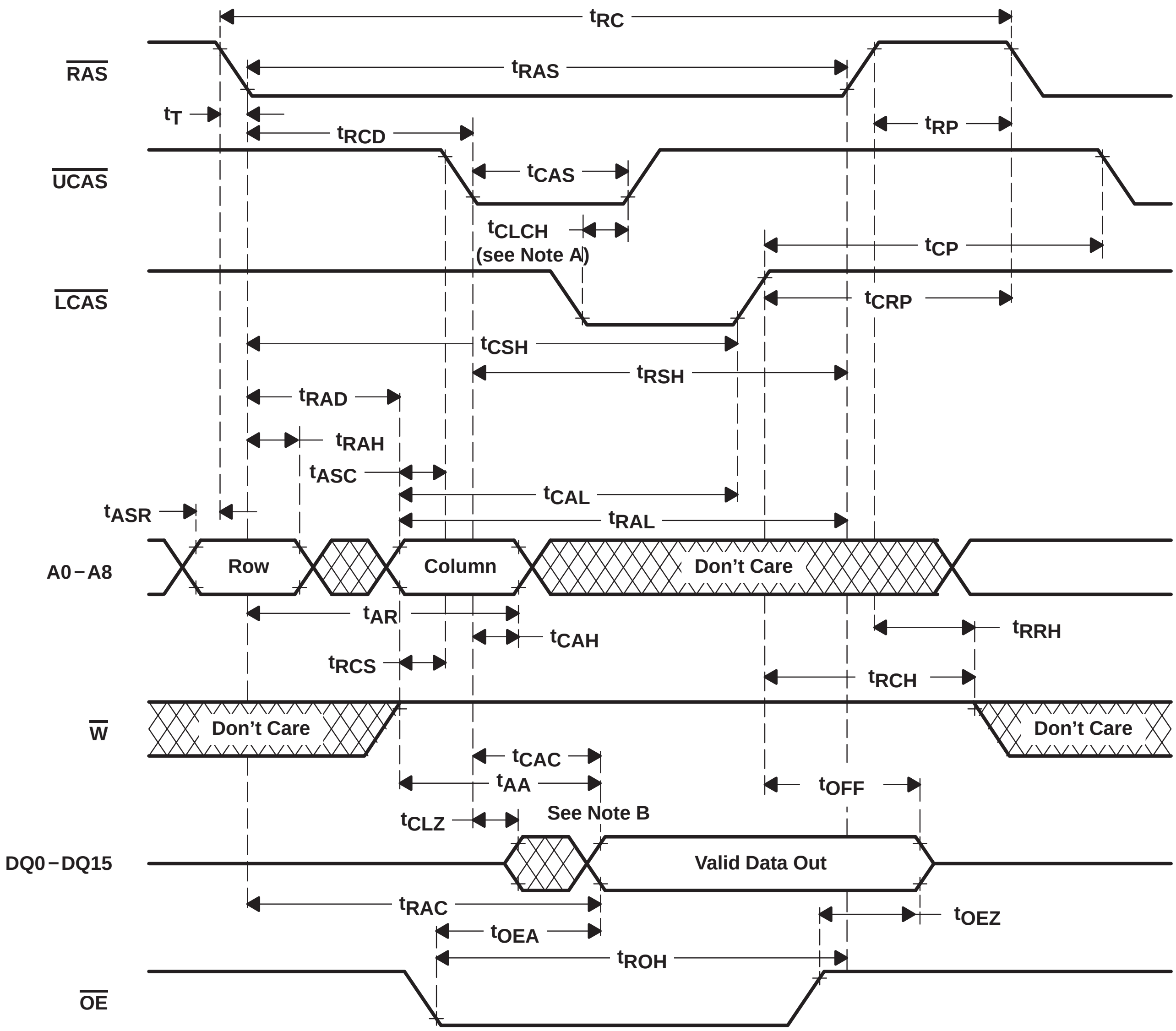
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

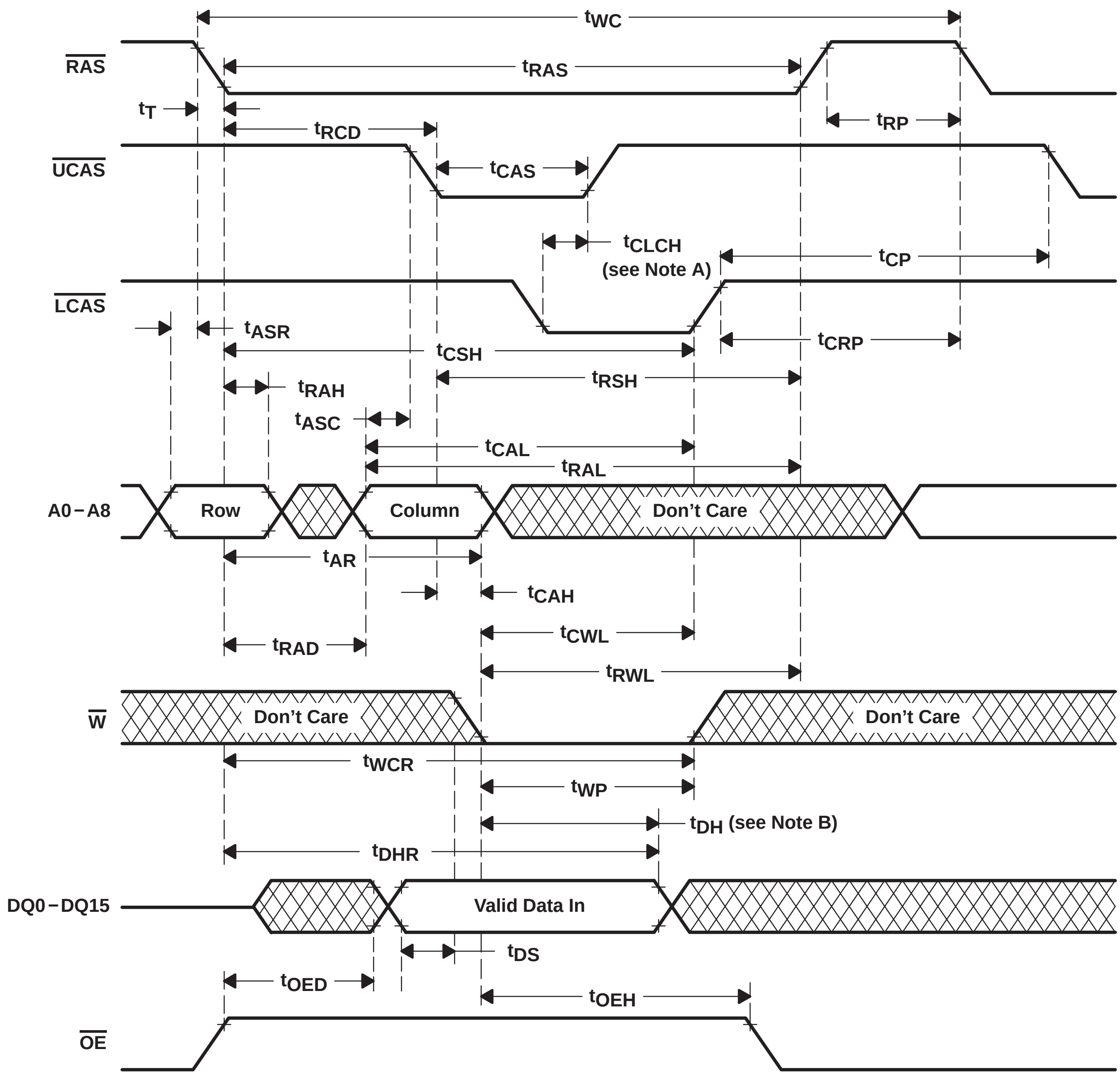
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from xCAS to its corresponding DQx.
D. xCAS order is arbitrary.

Figure 2. Read-Cycle Timing

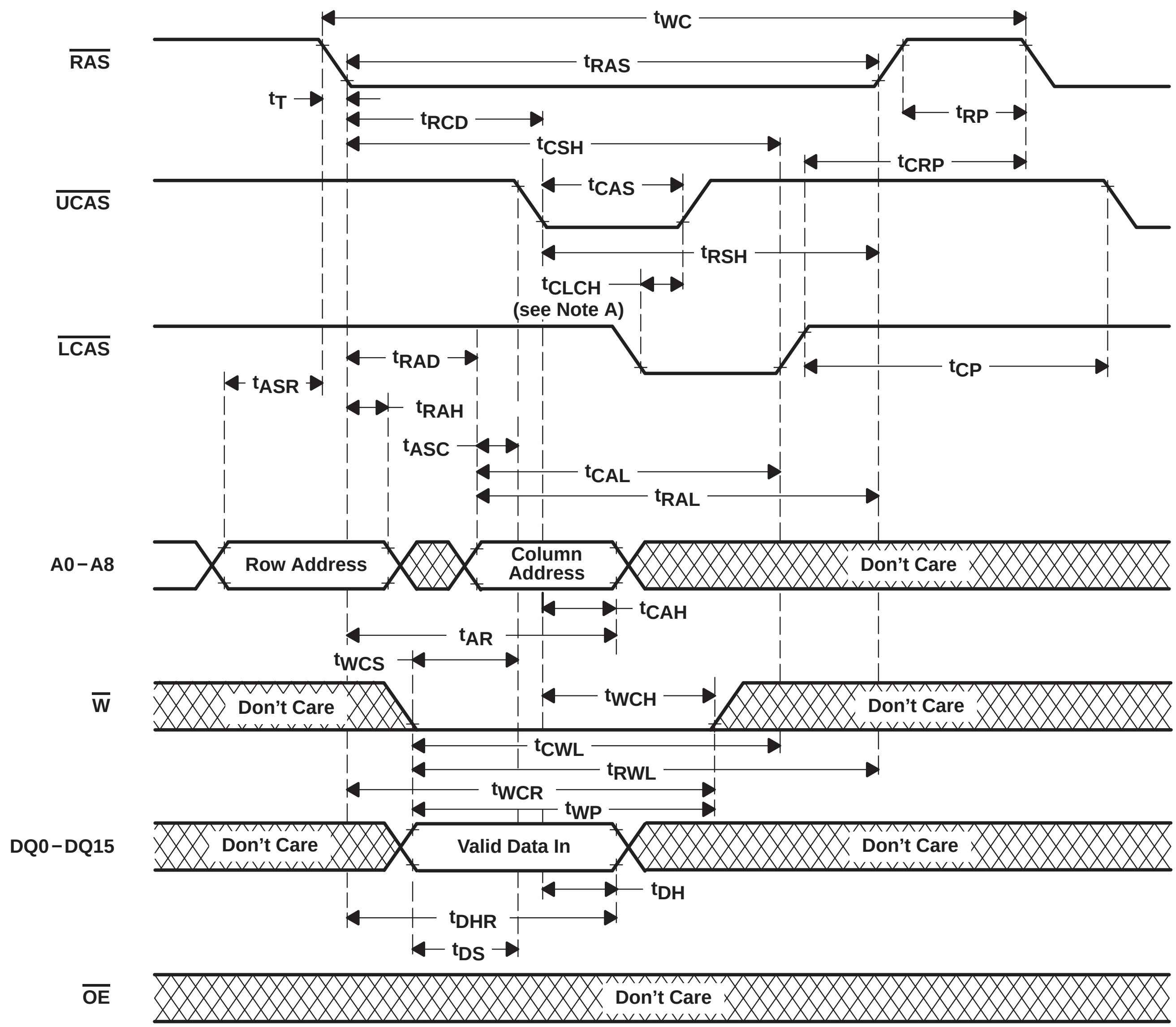
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Later of xCAS or W in write operations
C. xCAS order is arbitrary.

Figure 3. Write-Cycle Timing

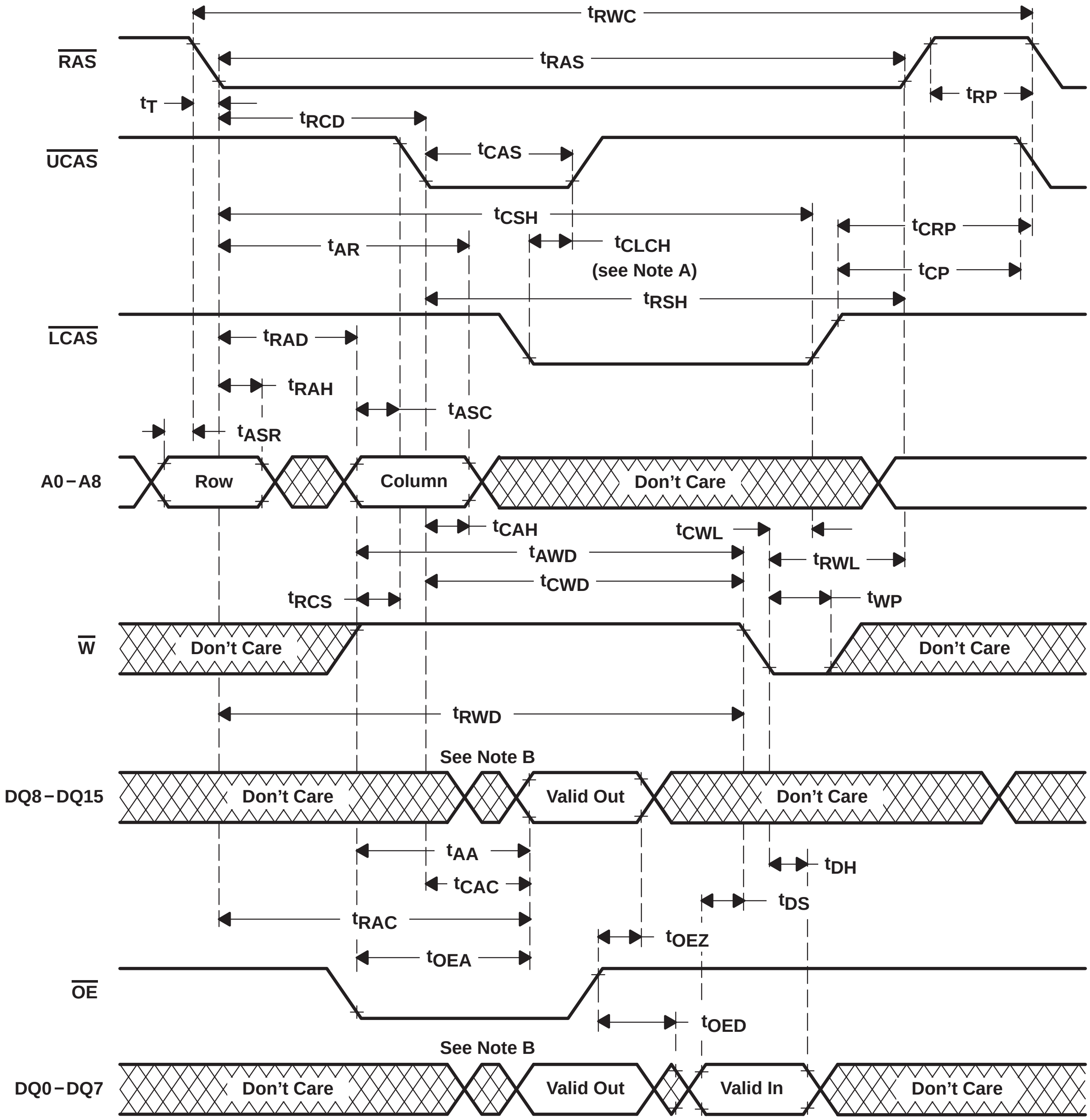
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 4. Early-Write-Cycle Timing

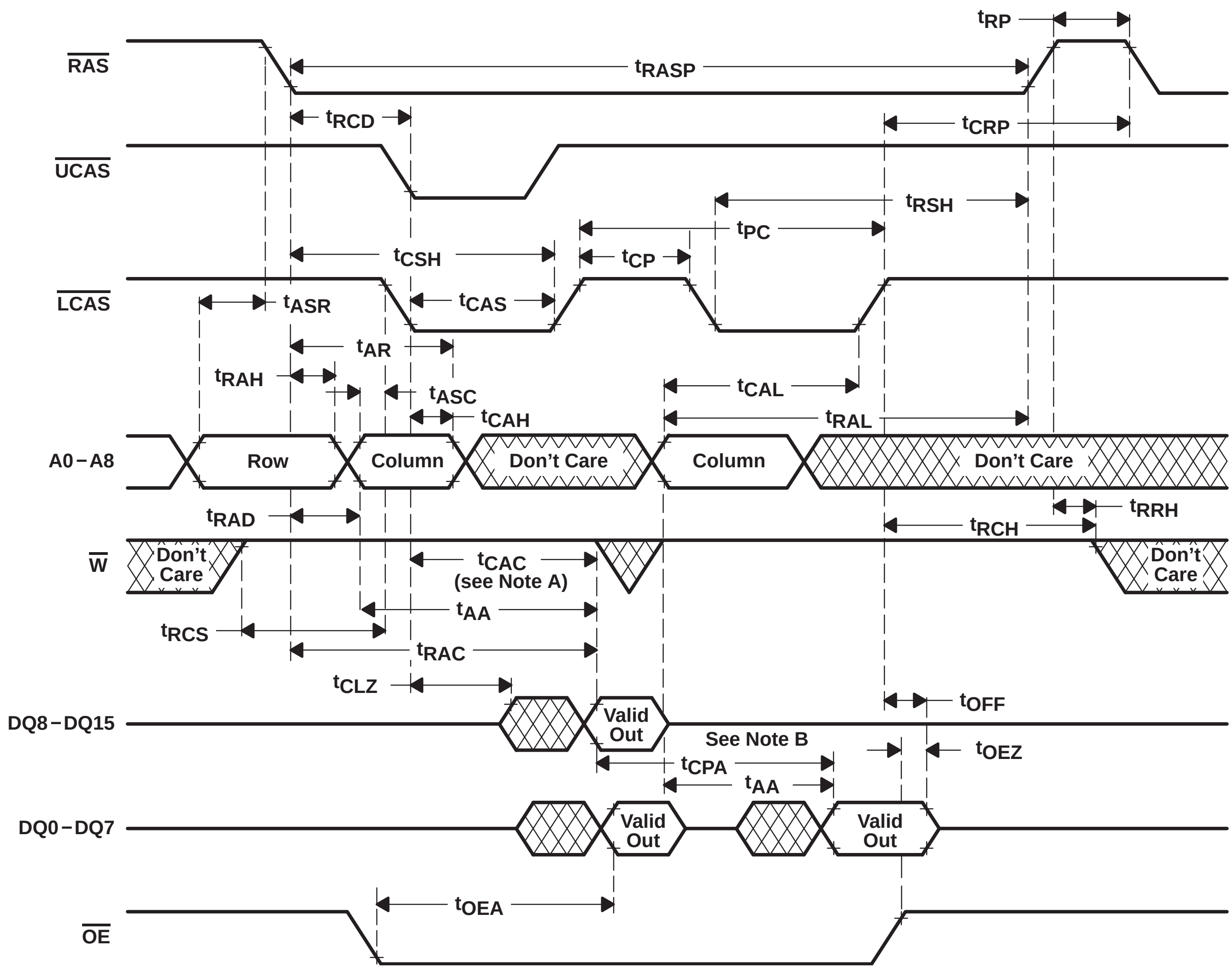
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

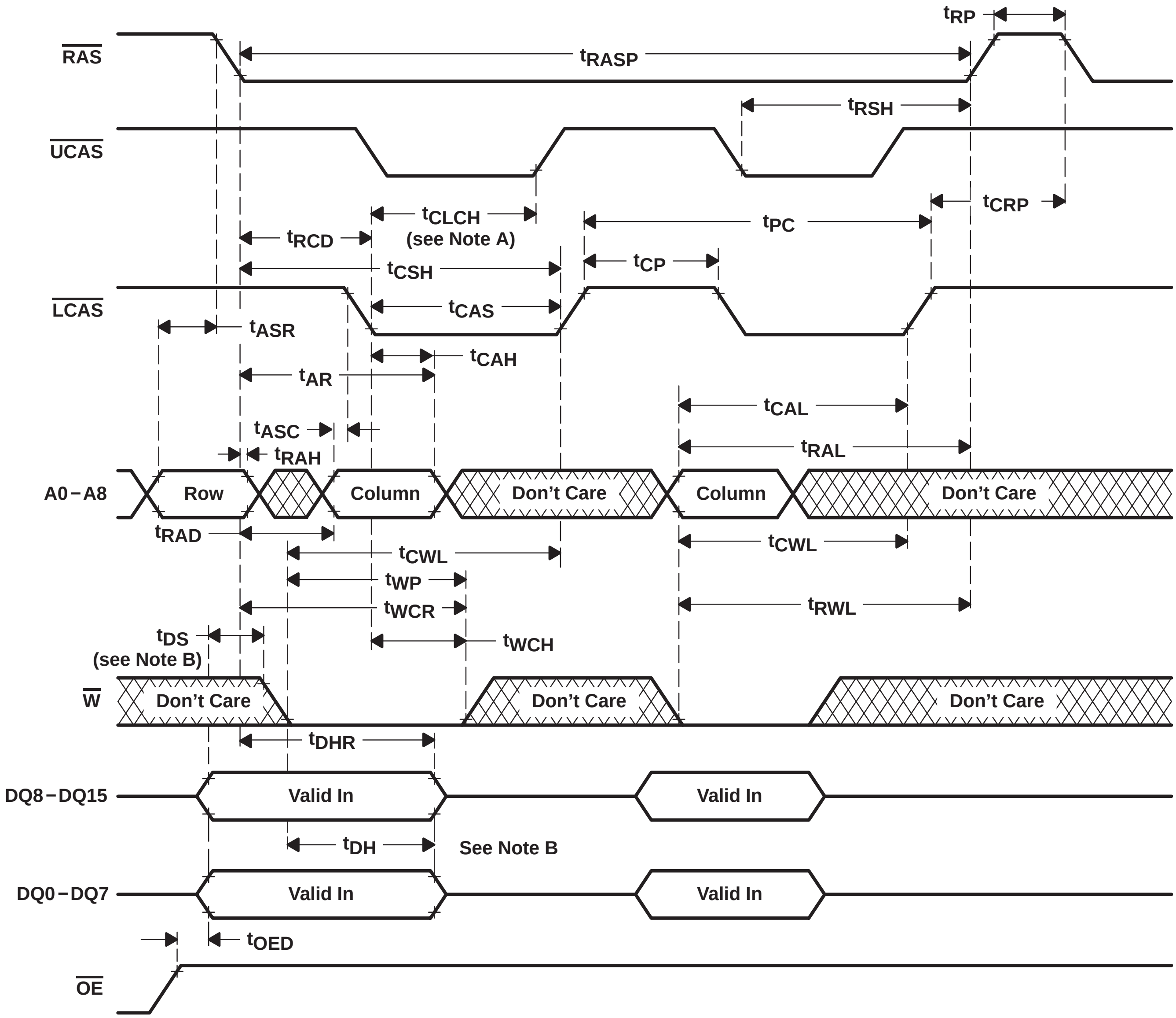
PARAMETER MEASUREMENT INFORMATION



NOTES: A. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
D. $\overline{xCAS}$ order is arbitrary.
E. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to $\overline{\text{xCAS}}$ or $\overline{\text{W}}$, whichever occurs last
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Write-Cycle Timing

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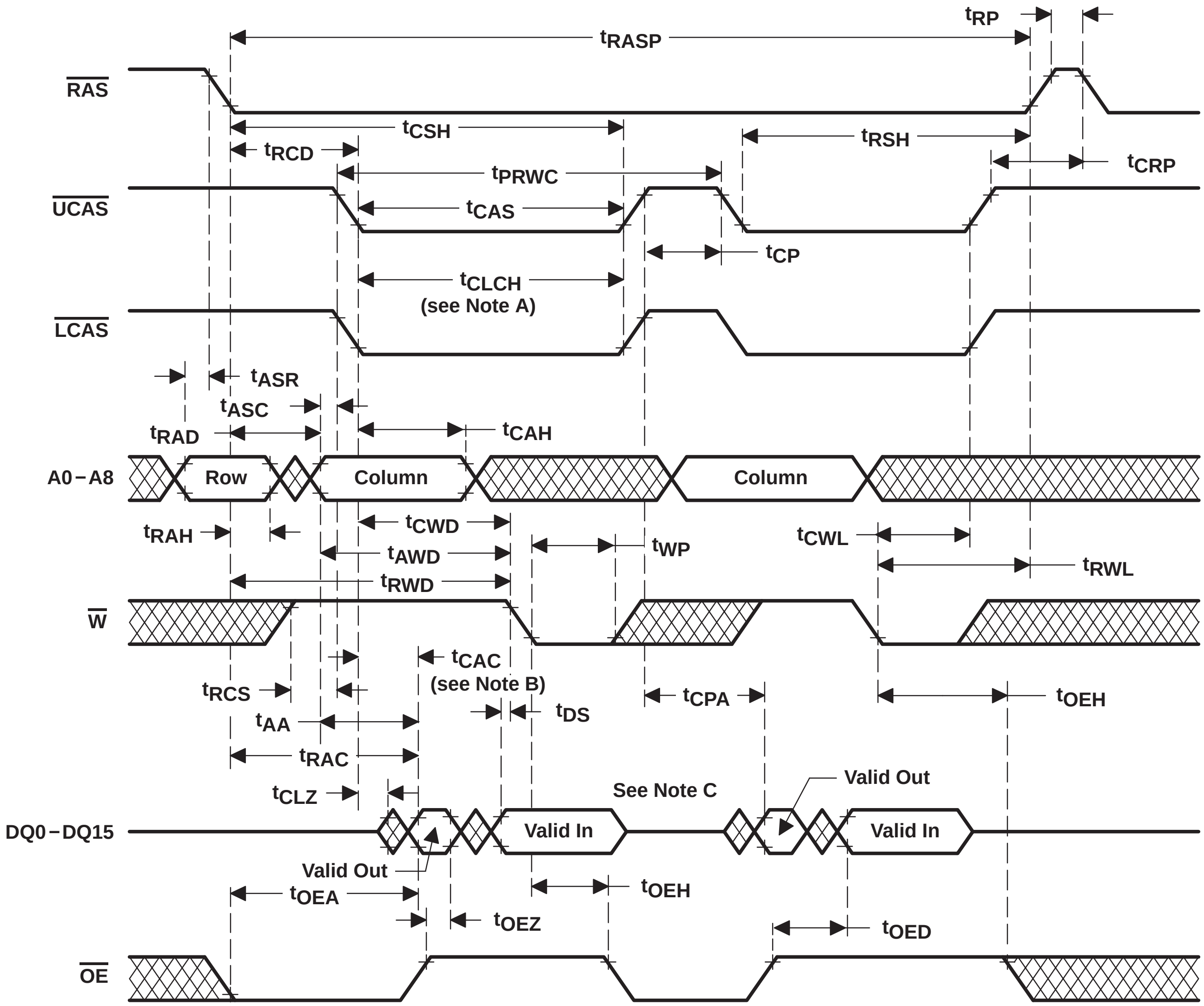
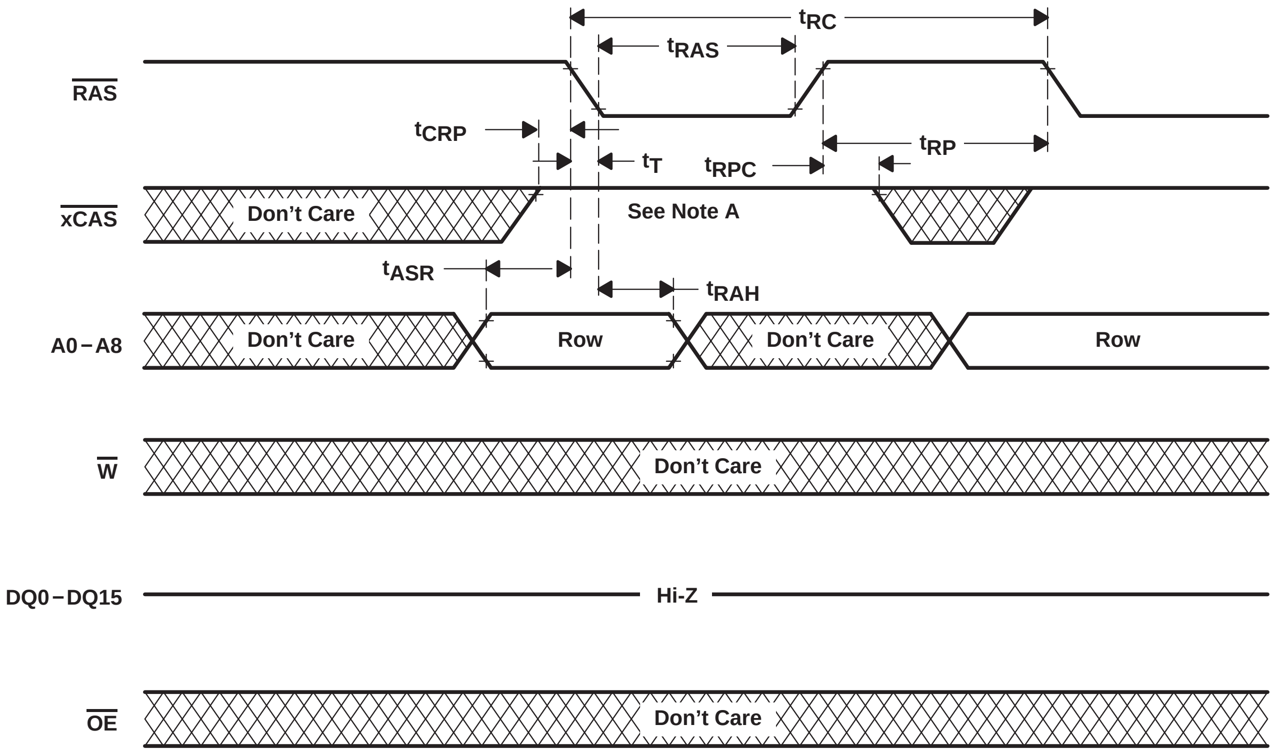
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from xCAS to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid data state prior to the specified access time.
D. xCAS order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All xCAS must be high.

Figure 9. RAS-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

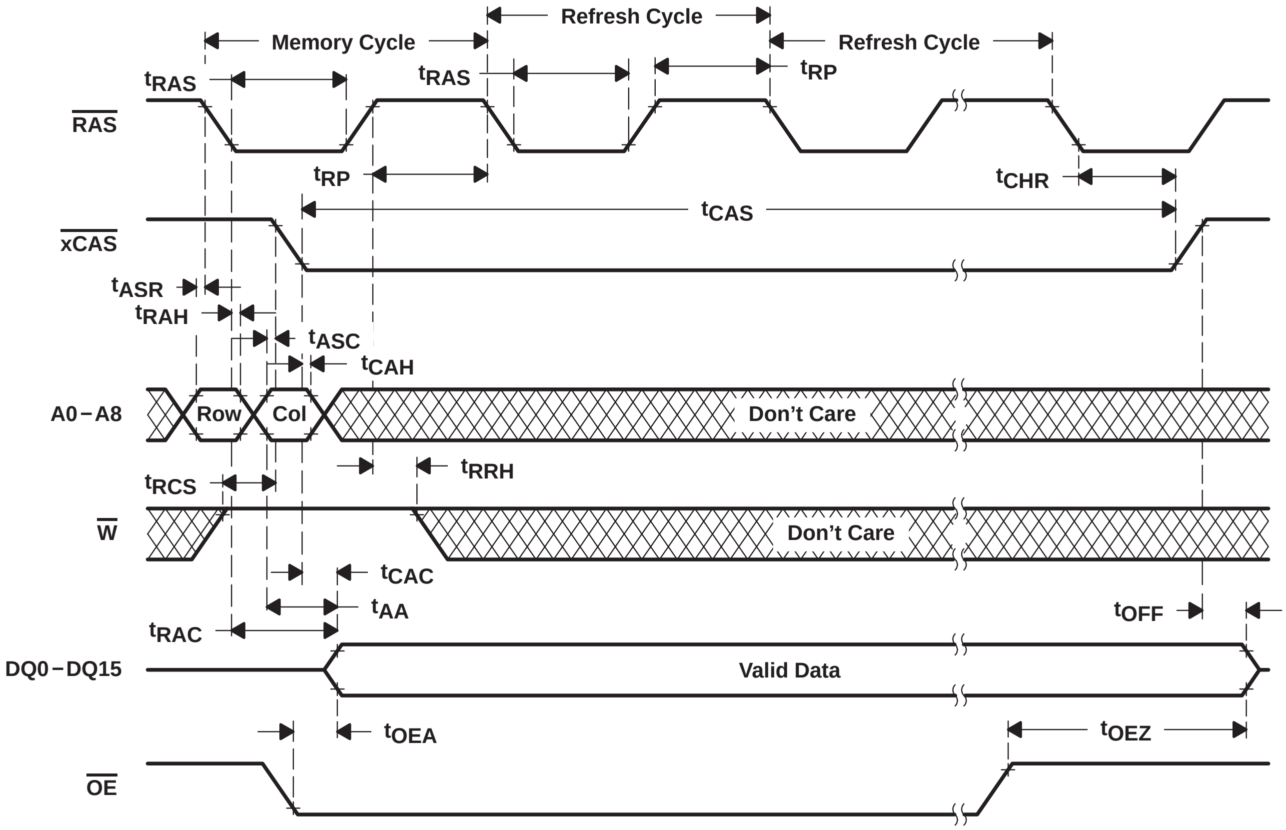
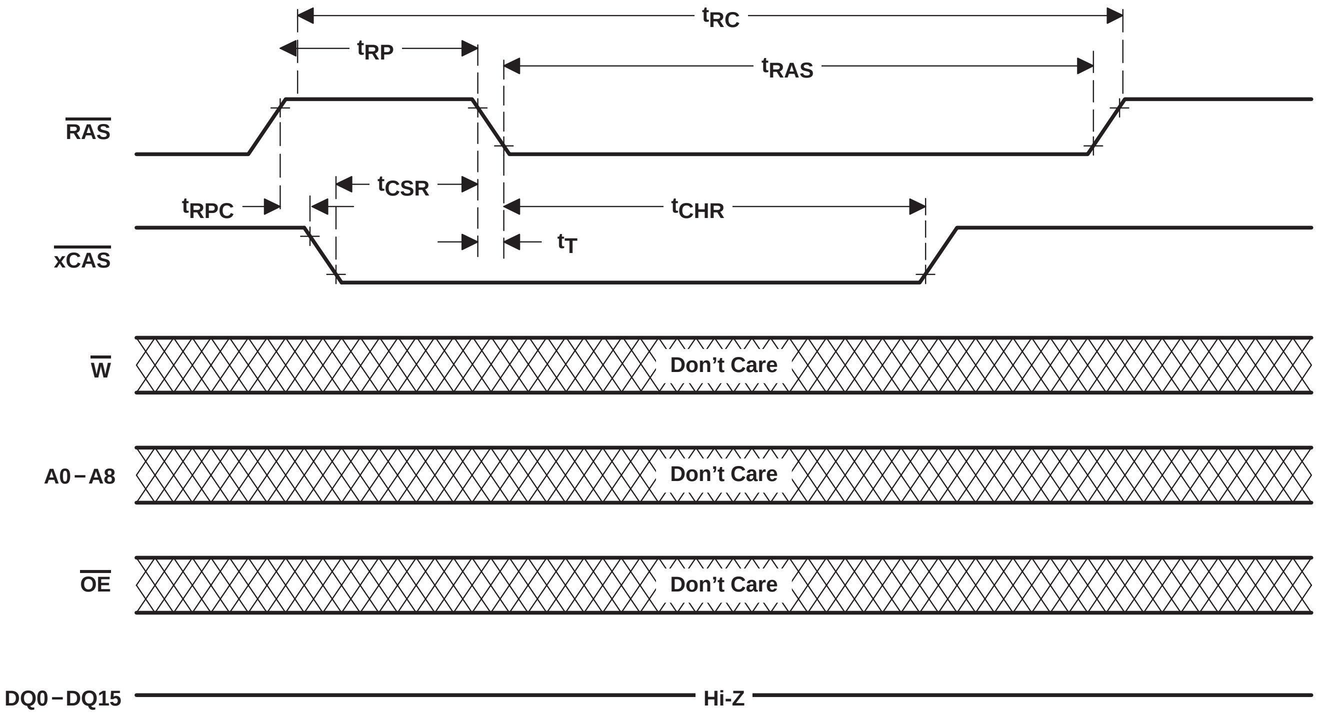


Figure 10. Hidden-Refresh-Cycle Timing

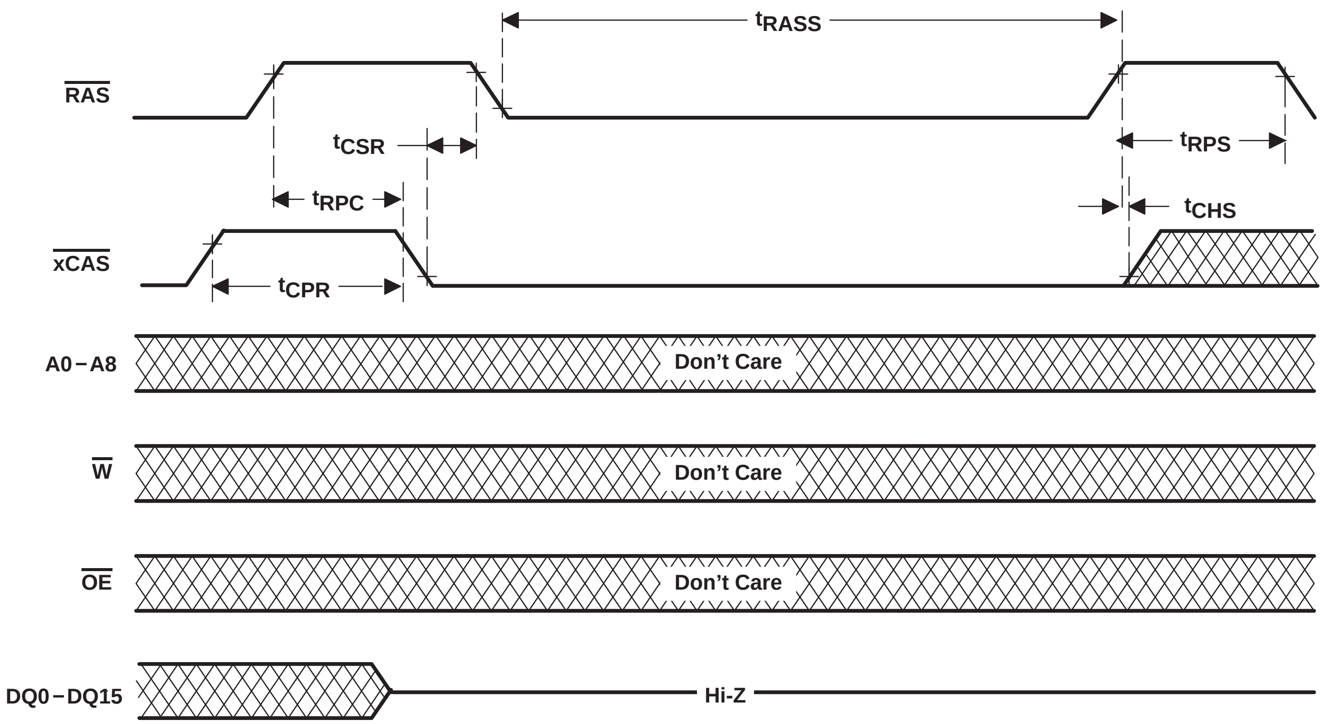
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{\text{xCAS}}$ can be used.

Figure 11. Automatic-CBR- Refresh-Cycle Timing

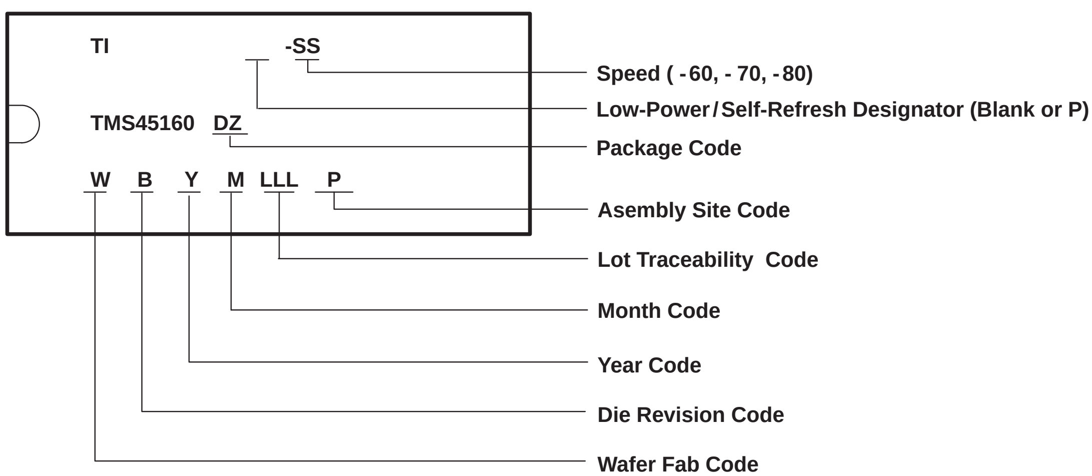
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any xCAS can be used.

Figure 12. Self-Refresh-Cycle Timing

device symbolization (TMS45160 illustrated)



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