



0.05 $\mu\text{V}/^\circ\text{C}$ max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

FEATURES

- LOW OFFSET VOLTAGE: 5 μV (max)
- ZERO DRIFT: 0.05 $\mu\text{V}/^\circ\text{C}$ max
- QUIESCENT CURRENT: 750 μA (max)
- SINGLE-SUPPLY OPERATION
- LOW BIAS CURRENT: 200pA (max)
- SHUTDOWN
- MicroSIZE PACKAGES
- WIDE SUPPLY RANGE: 2.7V to 12V

APPLICATIONS

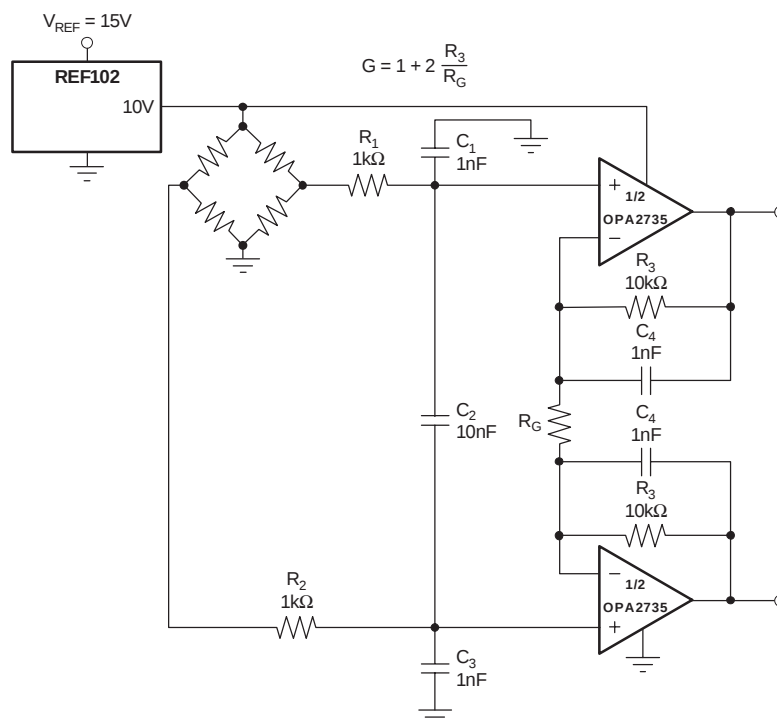
- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENTS
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

DESCRIPTION

The OPA734 and OPA735 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide low offset voltage (5 μV max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 50mV of the rails. Either single or bipolar supplies can be used in the range of +2.7V to +12V ($\pm 1.35\text{V}$ to $\pm 6\text{V}$). They are optimized for low-voltage, single-supply operation.

The OPA734 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is 9 μA (max) and the output placed in a high-impedance state.

The single version is available in the MicroSIZE SOT23-5 (SOT23-6 for shutdown version) and the SO-8 packages. The dual version is available in the MSOP-8 and SO-8 packages (MSOP-10 only for the shutdown version). All versions are specified for operation from -40°C to $+85^\circ\text{C}$.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	+13.2V
Signal Input Terminals, Voltage ⁽²⁾	(V-) – 0.5V to (V+) + 0.5V
Current ⁽²⁾	±10mA
Output Short Circuit ⁽³⁾	Continuous
Operating Temperature	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating (Human Body Model), OPA734	1000V
ESD Rating (Human Body Model), OPA735, OPA2734, OPA2735	2000V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA734	SOT23-6	DBV	–40°C to +85°C	NSB	OPA734AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA734AIDBVR	Tape and Reel, 3000
OPA734	SO-8	D	–40°C to +85°C	OPA734A	OPA734AID	Rails, 100
"	"	"	"	"	OPA734AIDR	Tape and Reel, 2500
OPA2734	MSOP-10	DGS	–40°C to +85°C	BGO	OPA2734AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2734AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA735	SOT23-5	DBV	–40°C to +85°C	NSC	OPA735AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA735AIDBVR	Tape and Reel, 3000
OPA735	SO-8	D	–40°C to +85°C	OPA735A	OPA735AID	Rails, 100
"	"	"	"	"	OPA735AIDR	Tape and Reel, 2500
OPA2735	SO-8	D	–40°C to +85°C	OPA2735A	OPA2735AID	Rails, 100
"	"	"	"	"	OPA2735AIDR	Tape and Reel, 2500
OPA2735	MSOP-8	DGK	–40°C to +85°C	BGN	OPA2735AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2735AIDGKR	Tape and Reel, 2500

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ ($V_S = +10V$)
Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

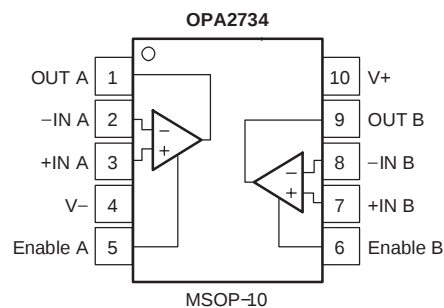
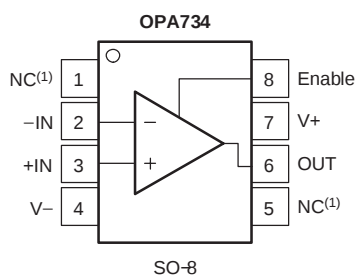
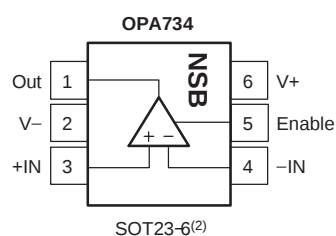
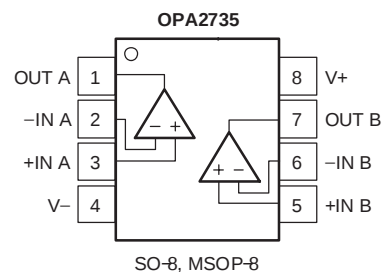
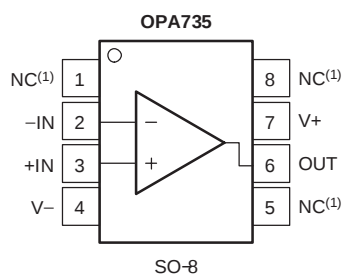
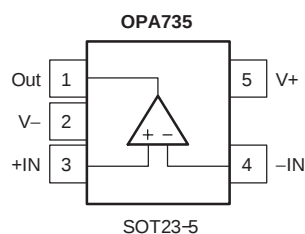
At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA734, OPA2734, OPA735, OPA2735			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply Long-Term Stability Channel Separation, dc	V_{OS} dV_{OS}/dT PSRR $V_S = 2.7V$ to $12V$, $V_{CM} = 0V$		1 0.01 0.2 Note (1) 0.1	5 0.05 1.8	μV $\mu V/^\circ\text{C}$ $\mu V/V$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current over Temperature Input Offset Current	I_B $V_{CM} = V_S/2$ I_{OS} $V_{CM} = V_S/2$		± 100 See Typical Characteristics ± 200	± 200 ± 300	pA pA pA
NOISE Input Voltage Noise, $f = 0.01\text{Hz}$ to 1Hz Input Voltage Noise, $f = 0.1\text{Hz}$ to 10Hz Input Voltage Noise Density, $f = 1\text{kHz}$ Input Current Noise Density, $f = 1\text{kHz}$	e_n e_n e_n i_n		0.8 2.5 135 40		μV_{PP} μV_{PP} $nV/\sqrt{\text{Hz}}$ $fA/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	V_{CM} CMRR $(V-) - 0.1V < V_{CM} < (V+) - 1.5V$	$(V-) - 0.1$ 115	130	$(V+) - 1.5$	V dB
INPUT CAPACITANCE Differential Common-Mode			2 10		pF pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	A_{OL} $(V-) + 100\text{mV} < V_O < (V+) - 100\text{mV}$	115	130		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate	GBW SR $G = +1$		1.6 1.5		MHz V/ μs
OUTPUT Voltage Output Swing from Rail Short-Circuit Current Open-Loop Output Impedance Capacitive Load Drive	$R_L = 10\text{k}\Omega$ I_{SC} $f = 1\text{MHz}$, $I_O = 0$ C_{LOAD}		20 ± 20 125 See Typical Characteristics	50	mV mA Ω
ENABLE/SHUTDOWN t_{OFF} $t_{ON}^{(2)}$ V_L (amplifier is shutdown) V_H (amplifier is active) I_{QSD} (per amplifier) Input Bias Current of Enable Pin		$V-$ $(V-) + 2$	1.5 150 4 3	$(V-) + 0.8$ $V+$ 9	μs μs V V μA μA
POWER SUPPLY Operating Voltage Range Quiescent Current (per amplifier)	V_S I_Q $I_O = 0$		2.7 to 12 (± 1.35 to ± 6) 0.6		V mA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT23-5, SOT23-6 MSOP-8, MSOP-10, SO-8	θ_{JA}	-40 -40 -65		+85 +150 +150	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$

(1) 300-hour life test at 150°C demonstrated randomly distributed variation in the range of measurement limits—approximately $1\mu\text{V}$.

(2) Device requires one complete auto-zero cycle to return to V_{OS} accuracy.

PIN CONFIGURATIONS



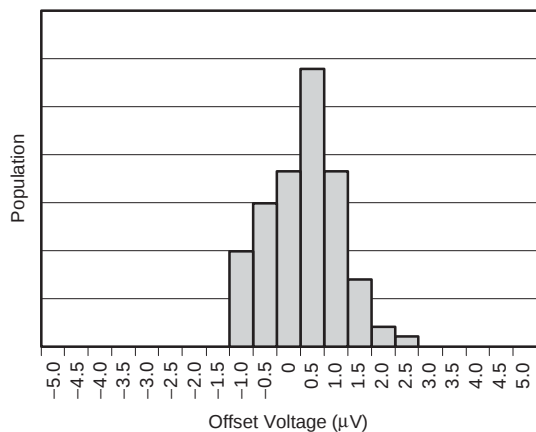
(1) NC = No Connection

(2) Pin 1 of the SOT23-6 is determined by orienting the package marking as shown in the diagram.

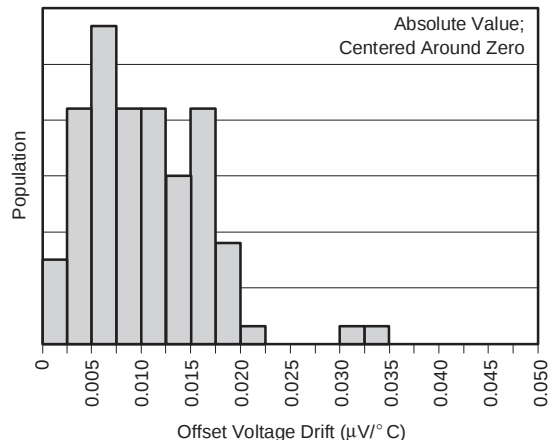
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as $\pm 10\text{V}$).

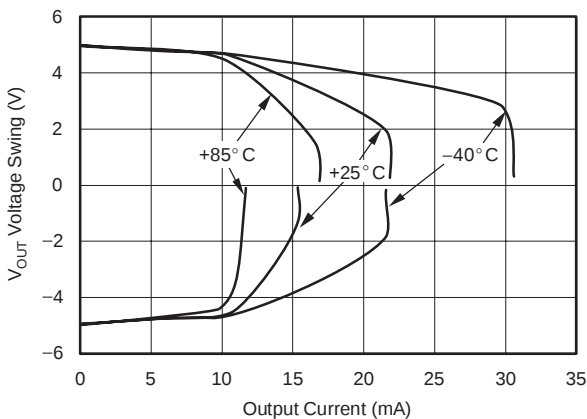
OUTPUT VOLTAGE PRODUCTION DISTRIBUTION



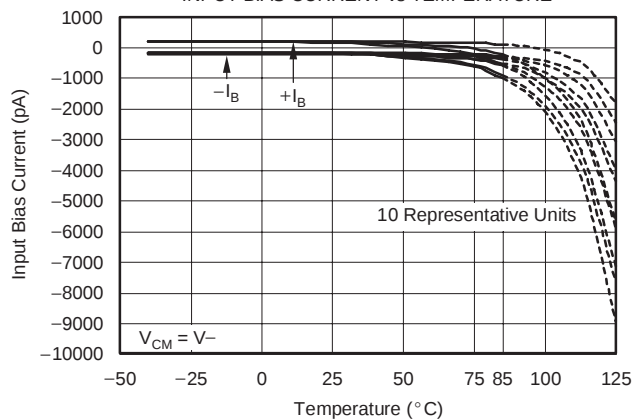
OUTPUT VOLTAGE DRIFT PRODUCTION DISTRIBUTION



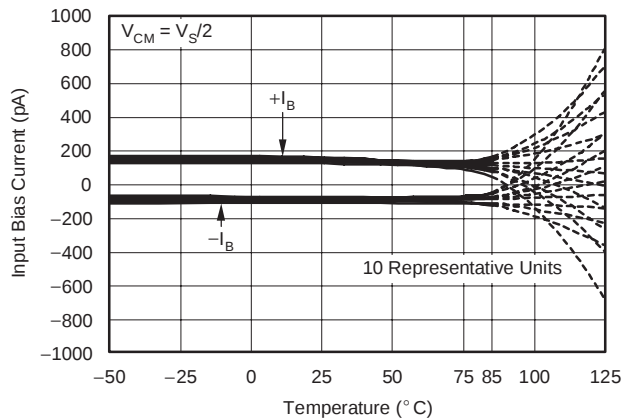
OUTPUT VOLTAGE SWING TO RAIL
vs OUTPUT CURRENT



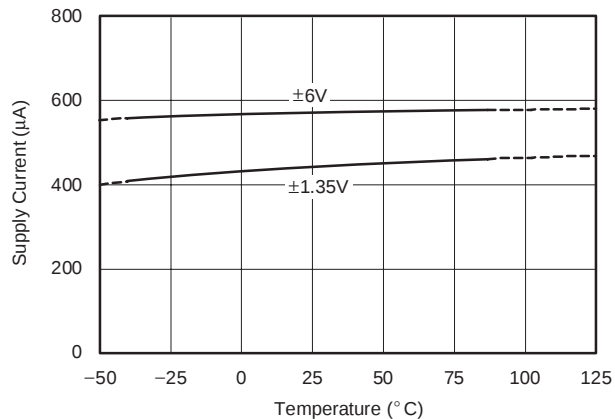
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE

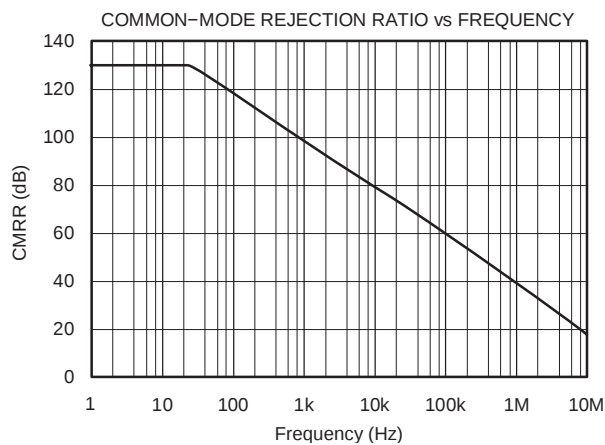
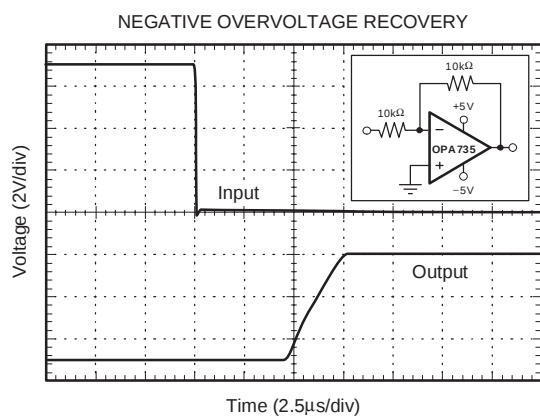
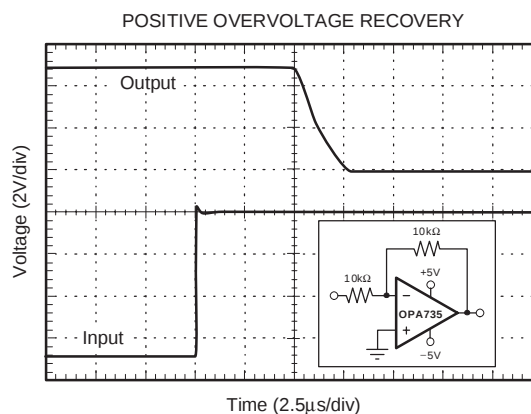
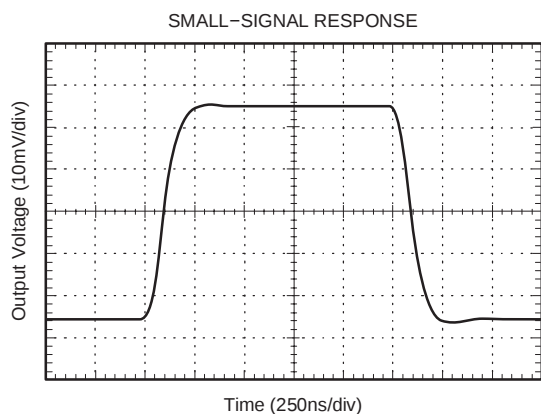
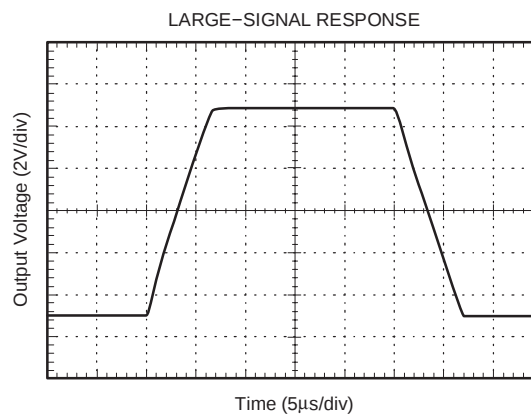
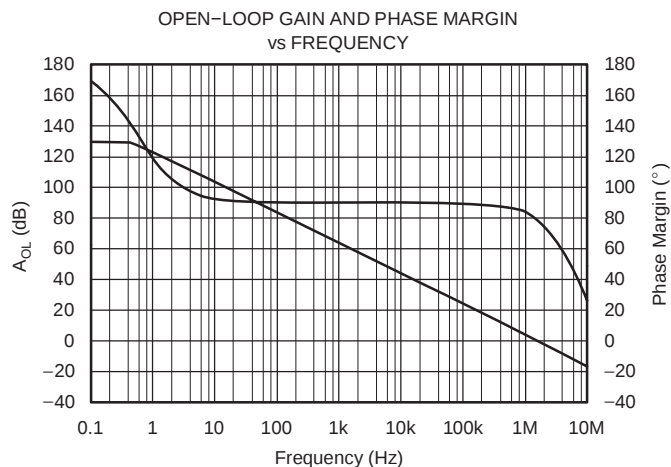


SUPPLY CURRENT vs TEMPERATURE



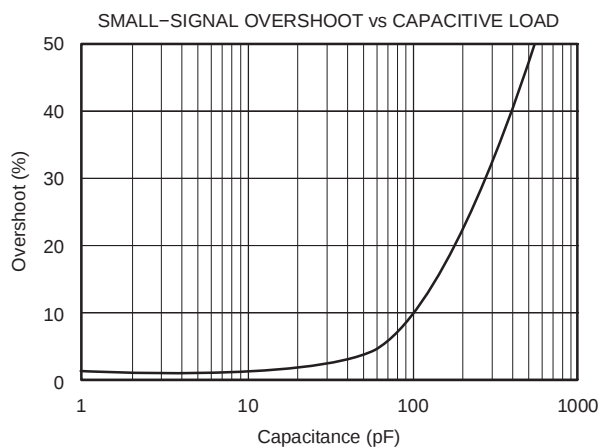
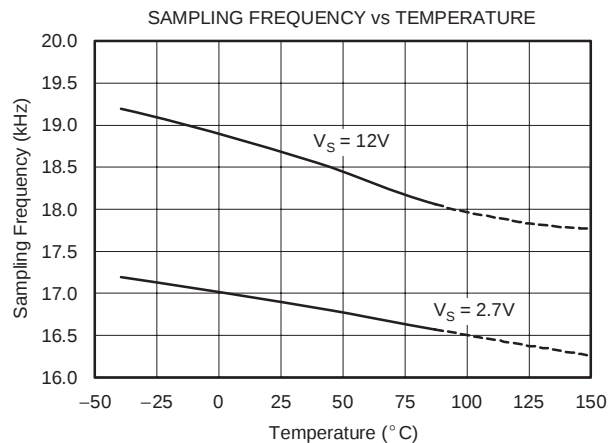
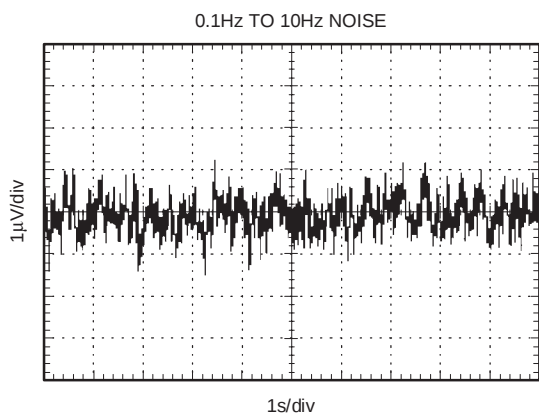
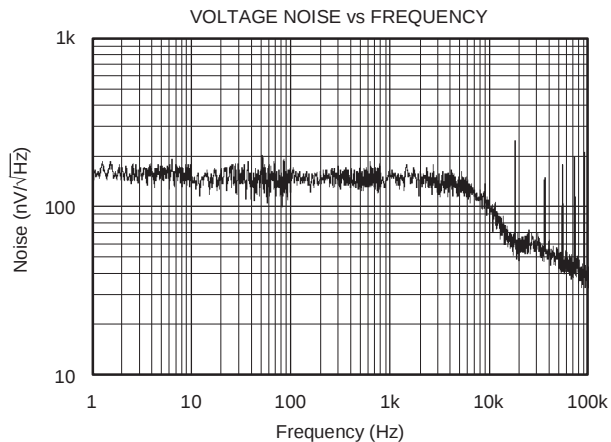
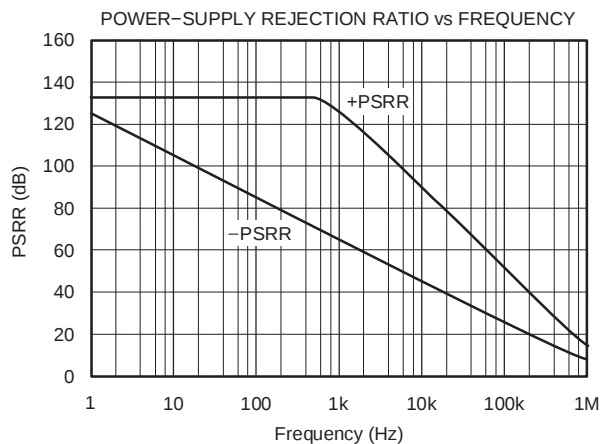
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as $\pm 10\text{V}$).



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as $+10\text{V}$).



APPLICATIONS INFORMATION

The OPA734 and OPA735 series of op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and demonstrate very low drift over time and temperature.

Good layout practice mandates the use of a 0.1μF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals:

1. Use low thermoelectric-coefficient connections (avoid dissimilar metals).
2. Thermally isolate components from power supplies or other heat sources.
3. Shield op amp and input circuitry from air currents such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on the materials used.

OPERATING VOLTAGE

The OPA734 and OPA735 op amp family operates with a power-supply range of +2.7V to +12V (±1.35V to ±6V). Supply voltages higher than +13.2V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA734 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V₋ supply voltage of the op amp. A logic HIGH enables the op amp. A valid logic HIGH is defined as > (V₋) + 2V. The valid logic HIGH signal can be up to the positive supply, independent of the negative power supply voltage. A valid logic LOW is defined as < 0.8V above the V₋ supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin is connected to internal pull-up circuitry and will enable the device if this pin is left open circuit.

The logic input is a CMOS input. Separate logic inputs are provided for each op amp on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is 150μs, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to returning to full accuracy, the amplifier may function properly, but with unspecified offset voltage.

Disable time is 1.5μs. When disabled, the output assumes a high-impedance state. The disable state allows the OPA734 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from (V₋) – 0.1V to (V₊) – 1.5V. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the specified input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 100pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

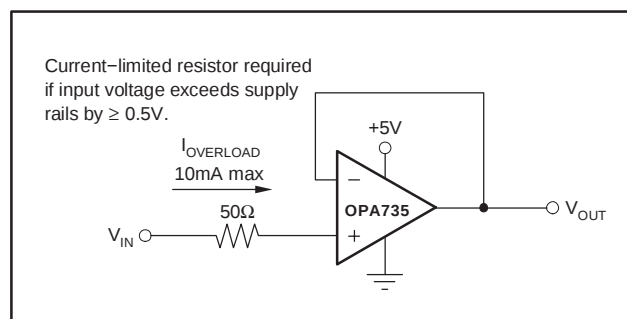


Figure 1. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA734 and OPA735 series of op amps use an auto-zero topology with a time-continuous 1.6MHz op amp in the signal path. This amplifier is zero-corrected every 100μs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100μs in addition to the start-up time for the bias circuitry to achieve specified V_{OS} accuracy. Prior to this time, the amplifier may function properly but with unspecified offset voltage.

Low-gain (< 20) operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.1% of a full-scale input step change, one calibration cycle (100 μ s) can be required to achieve full accuracy.

The term *clock feedthrough* describes the presence of the clock frequency in the output spectrum. In auto-zeroed op amps, clock feedthrough may result from the settling of the internal sampling capacitor, or from the small amount of charge injection that occurs during the sample-and-hold of the op amp offset voltage. Feedthrough can be minimized by keeping the source impedance relatively low ($< 1\text{k}\Omega$) and matching the source impedance on both input terminals. If the source resistance is high ($> 1\text{k}\Omega$) feedthrough can generally be reduced with a capacitor of 1nF or greater in parallel with the source or feedback resistors. See the circuit application examples.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1 μ F capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

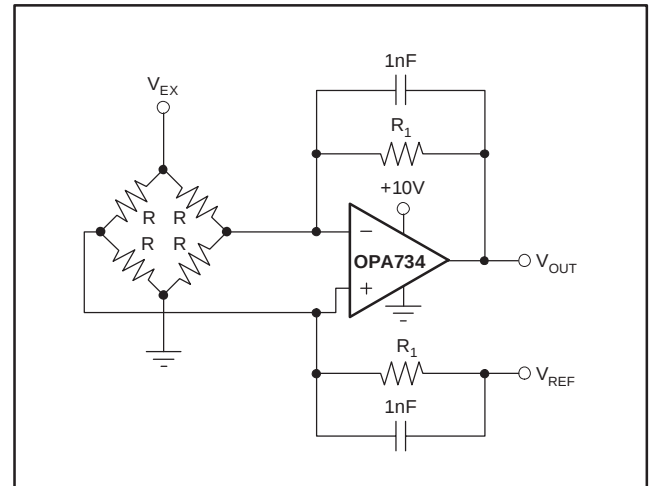


Figure 2. Single Op Amp Bridge Amplifier Circuit

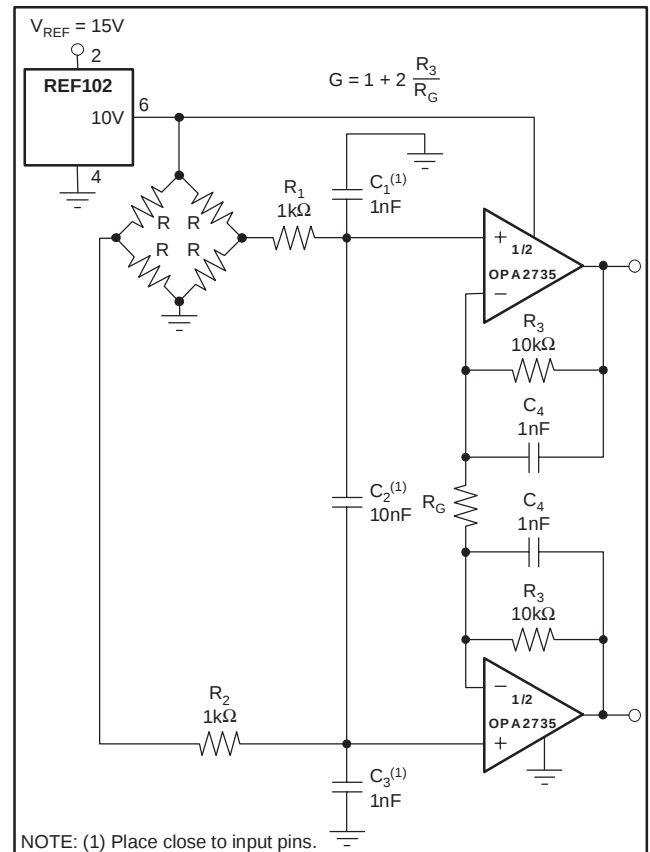


Figure 3. Differential Output Bridge Amplifier

[illegible]

10

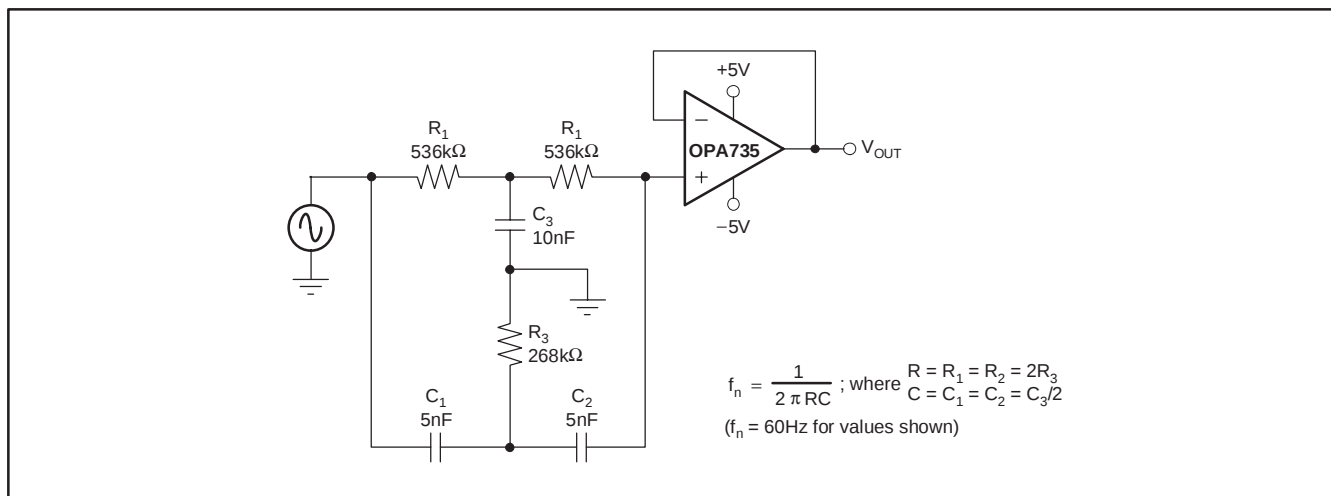


Figure 6. Twin-T Notch Filter

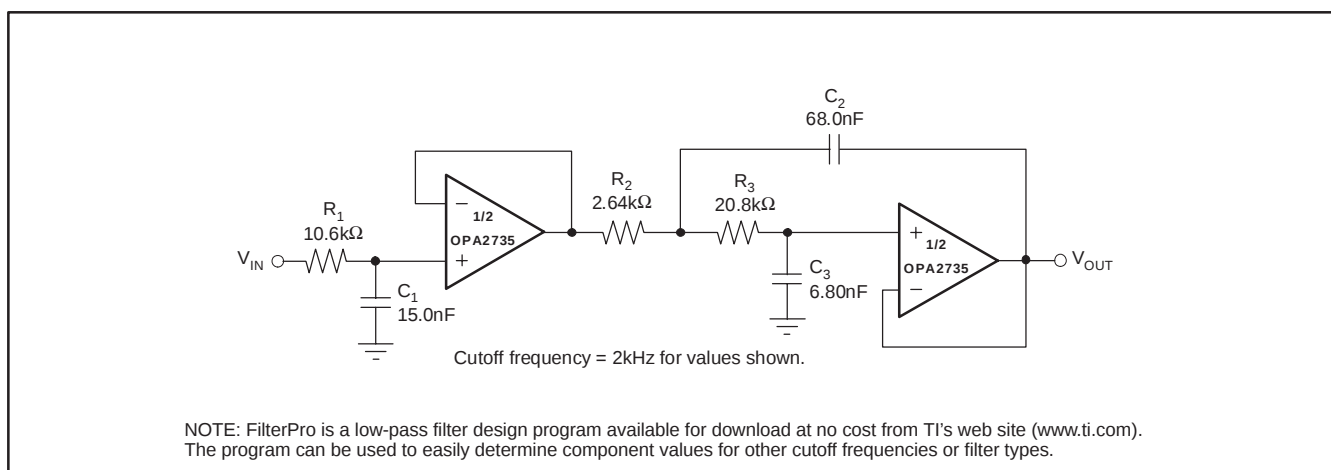


Figure 7. High DC Accuracy, 3-Pole Low-Pass Filter

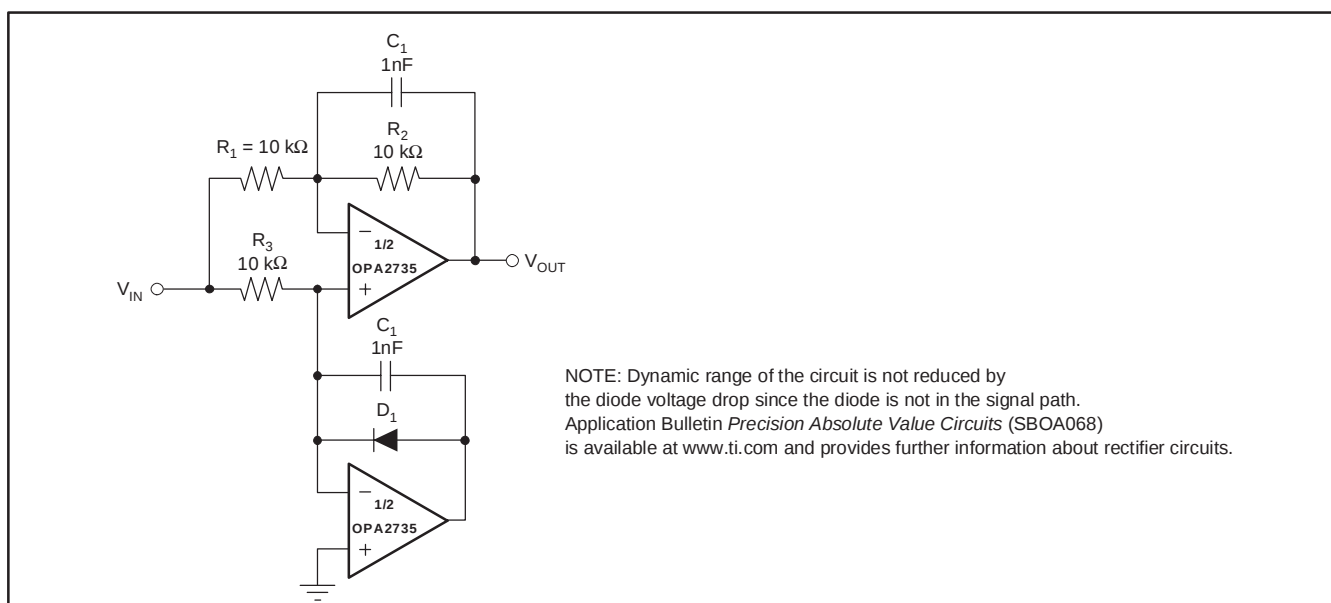
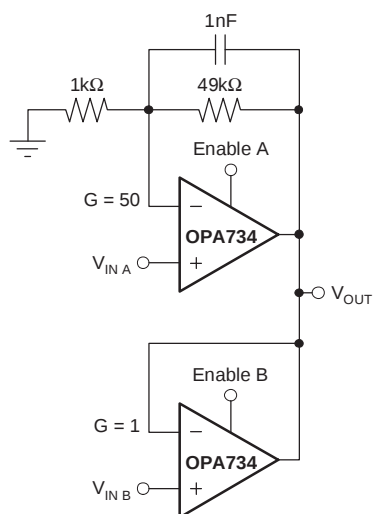


Figure 8. Precision Full-Wave Rectifier with Full Dynamic Range



Enable inputs are CMOS logic compatible.

Figure 9. High-Precision 2-Input MUX for Programmable Gain

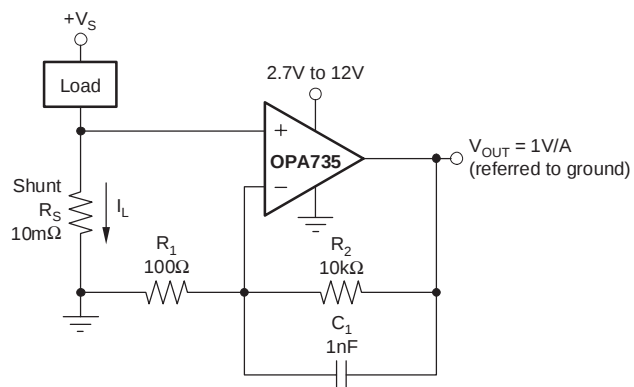


Figure 10. Low-Side Power-Supply Current Sensing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2734AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2734AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2734AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGO	Samples
OPA2735AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BGN	Samples
OPA2735AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA2735AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2735A	Samples
OPA734AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A	Samples
OPA734AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSB	Samples
OPA734AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 734A	Samples
OPA735AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA735AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSC	Samples
OPA735AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples
OPA735AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 735A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2734AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2734AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA735AIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA735AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA735AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

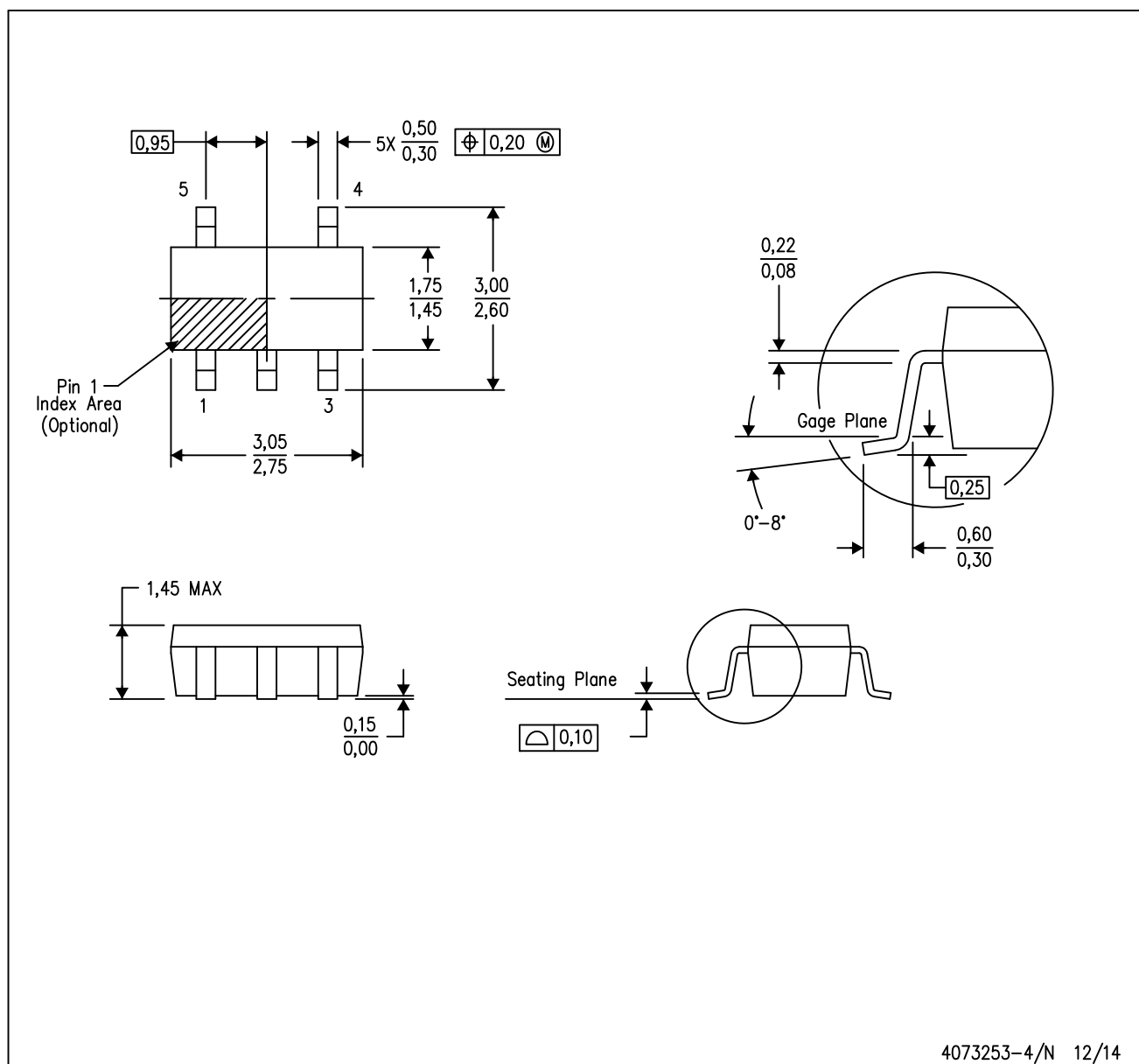


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2734AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2734AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA2735AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2735AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2735AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA735AIDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA735AIDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA735AIDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R-PDSO-G5)

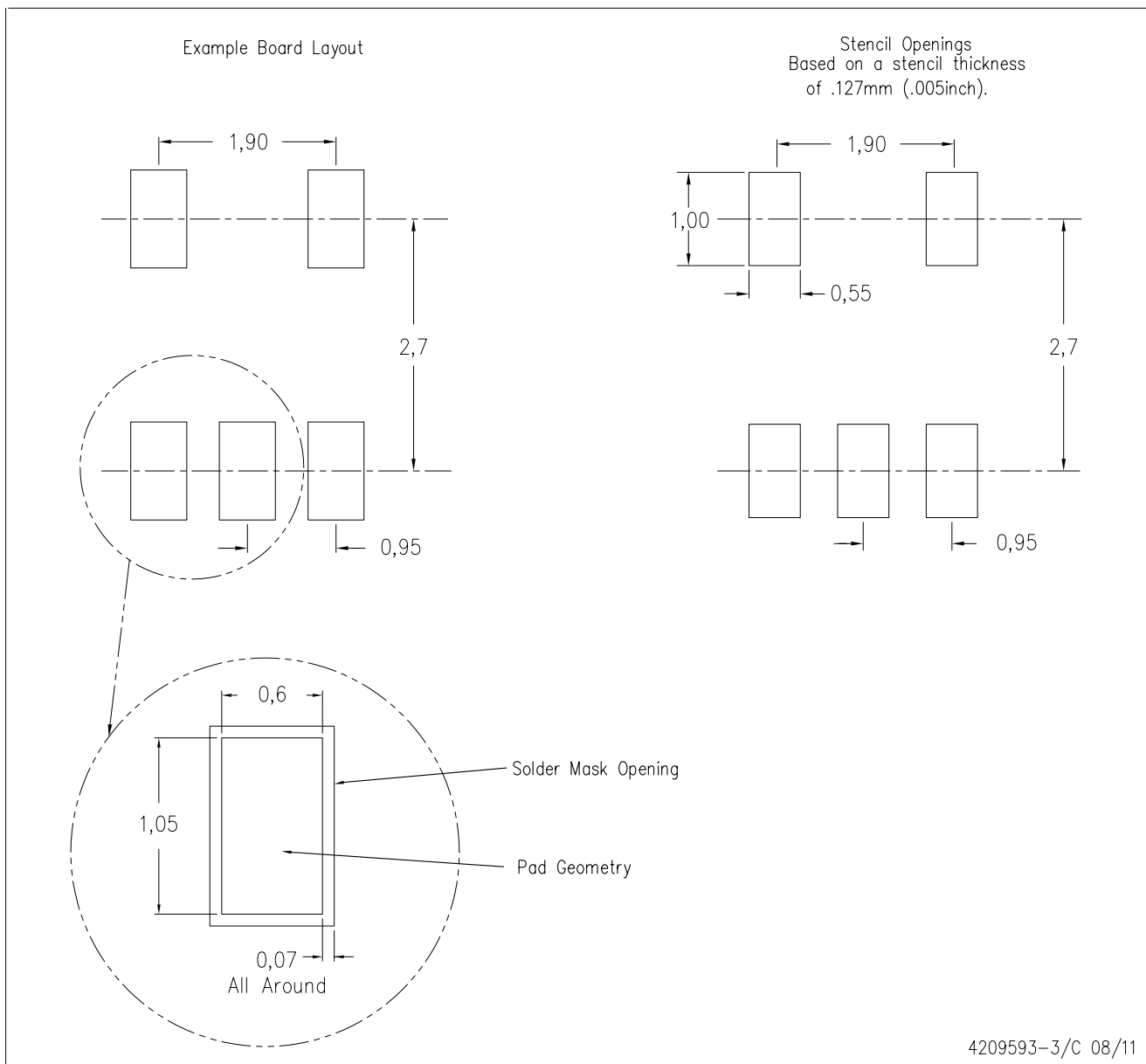
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

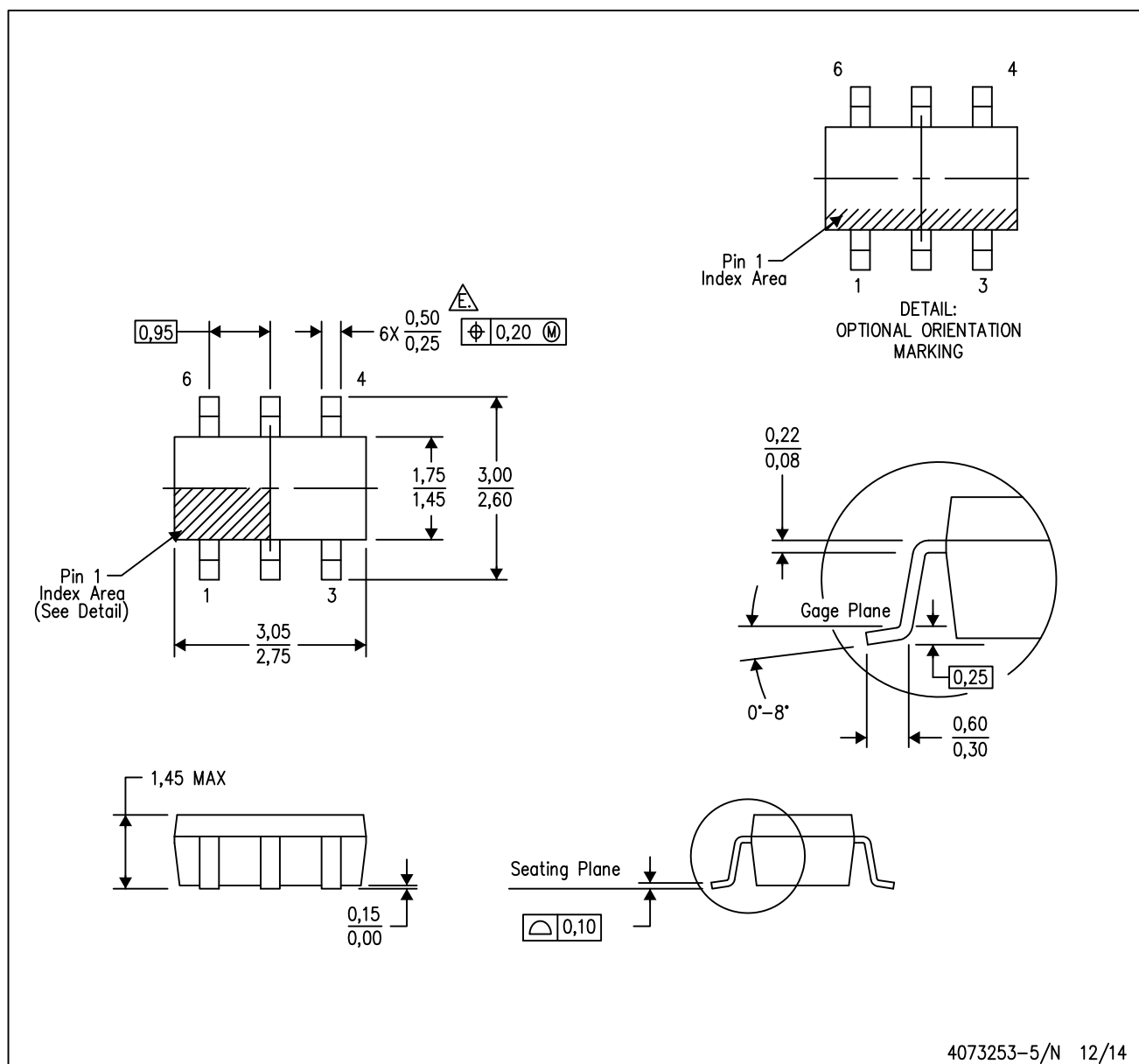
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV (R-PDSO-G6)

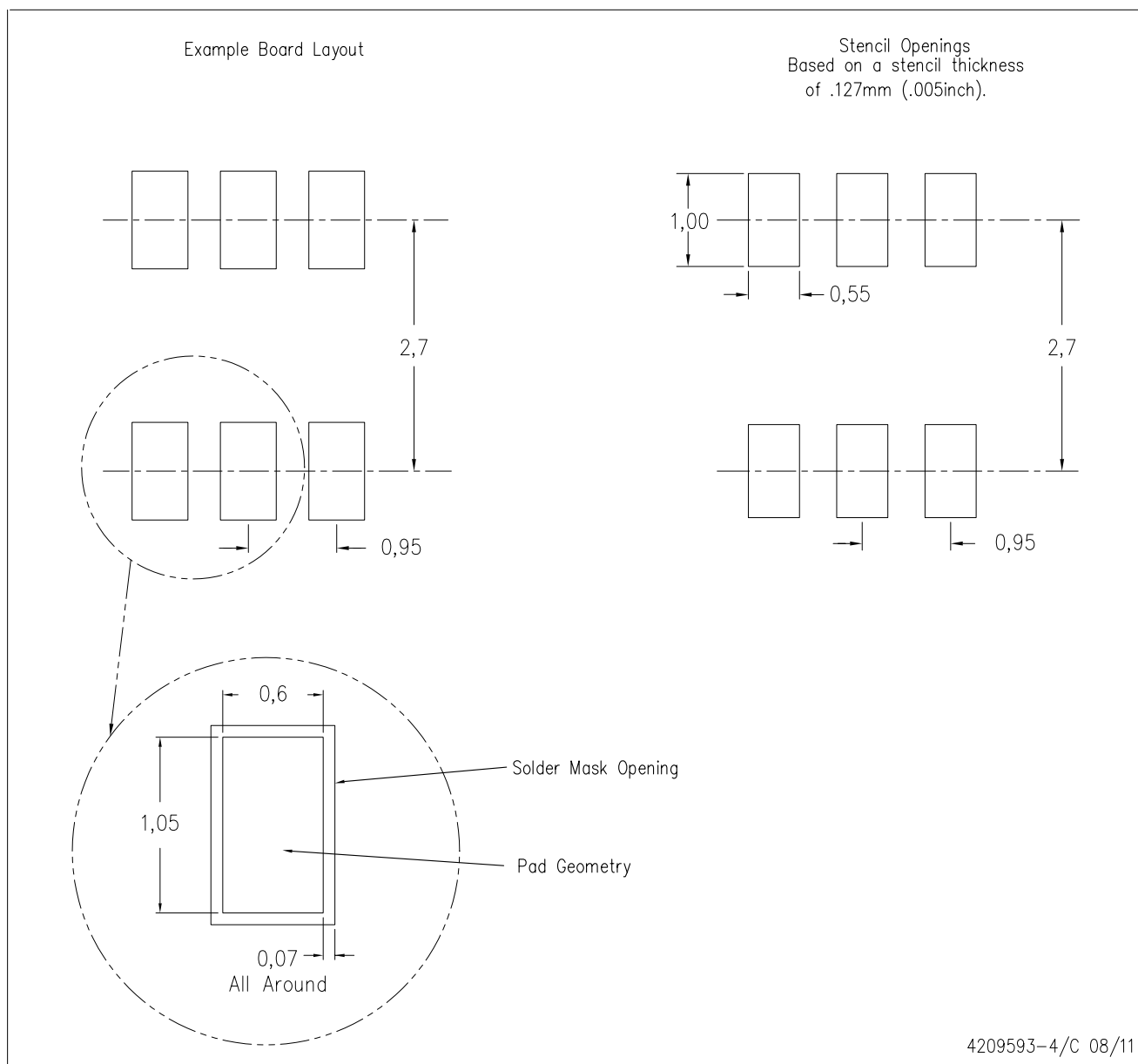
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

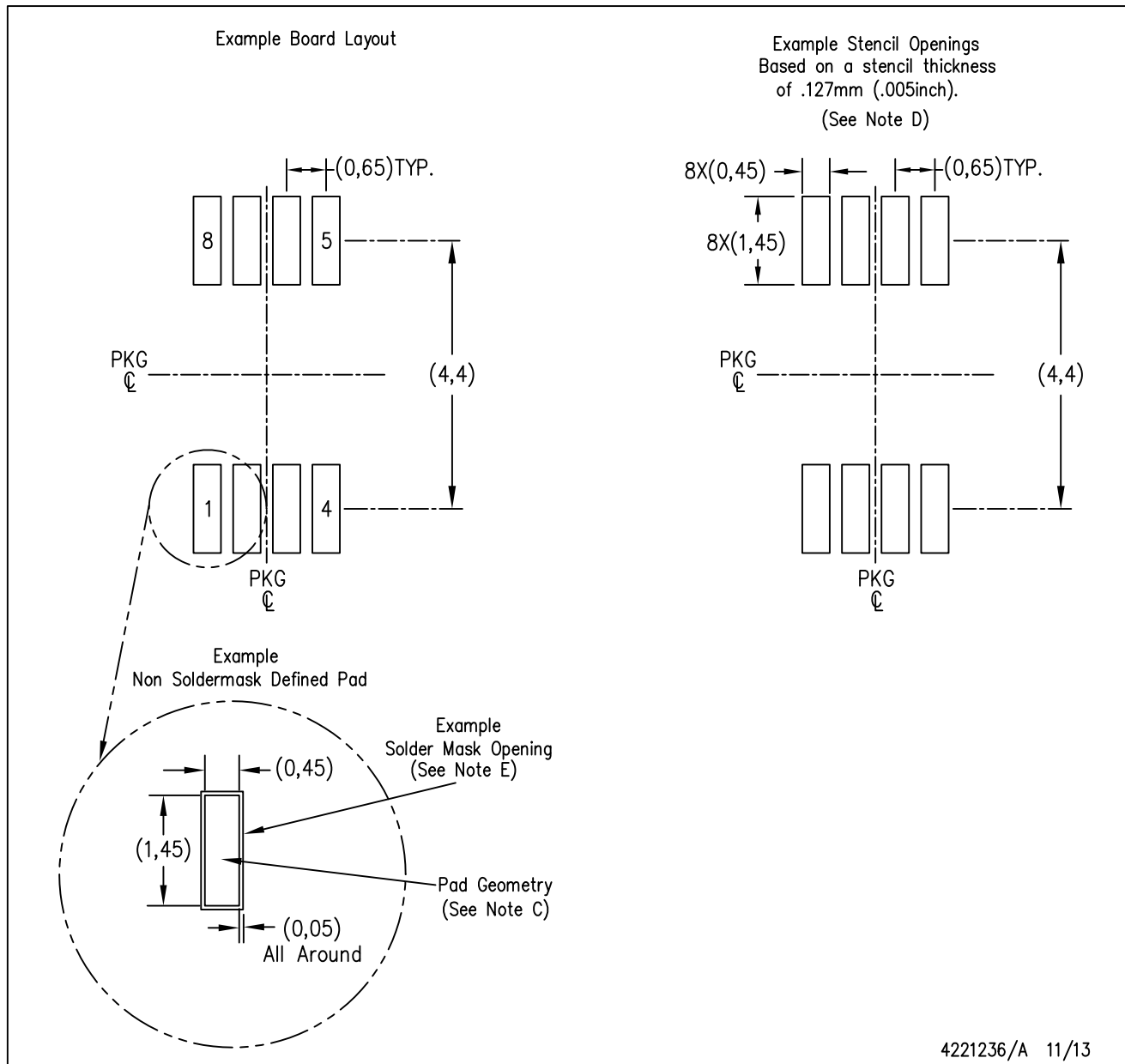
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

DGK (S-PDSO-G8)

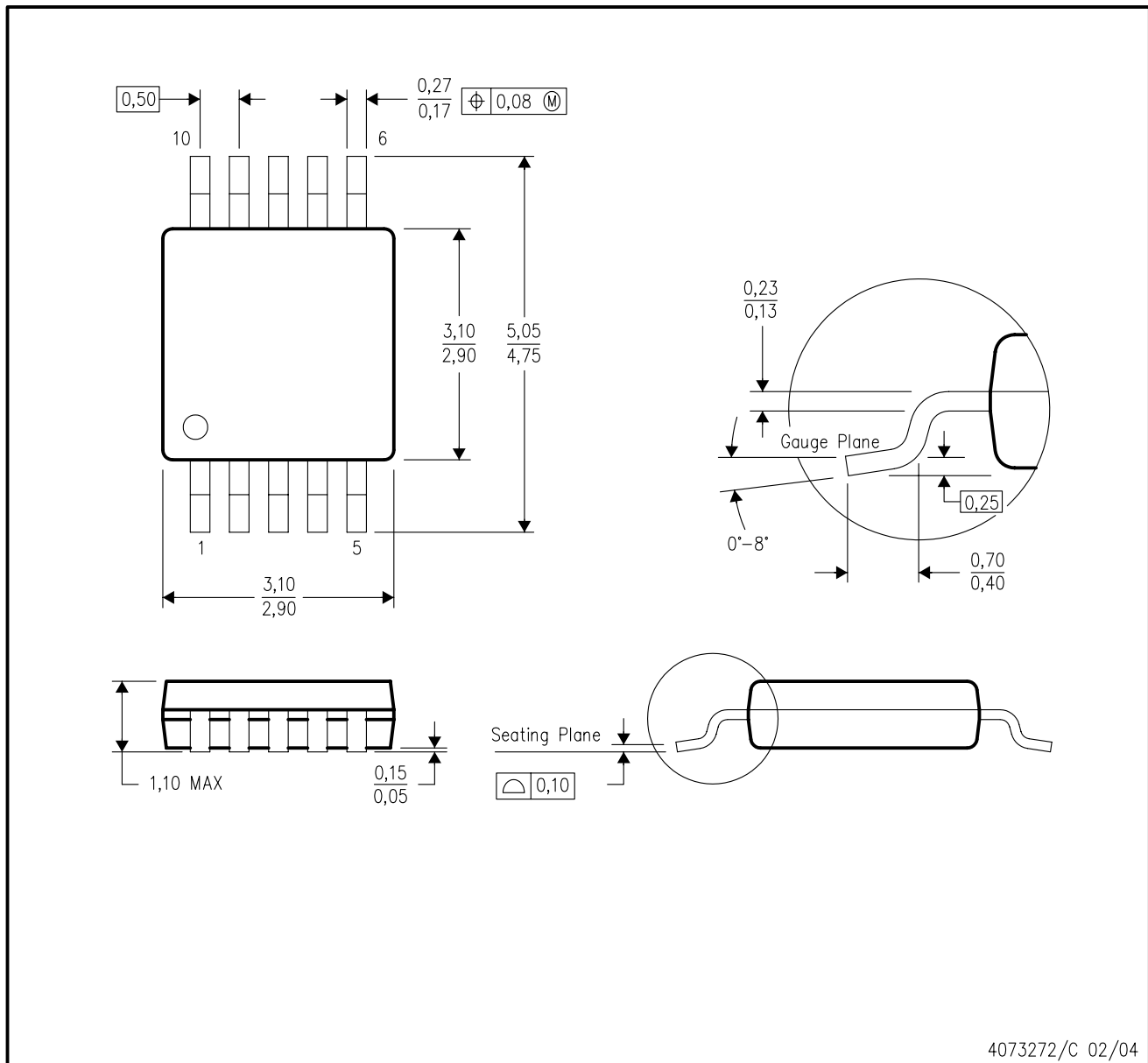
PLASTIC SMALL OUTLINE PACKAGE



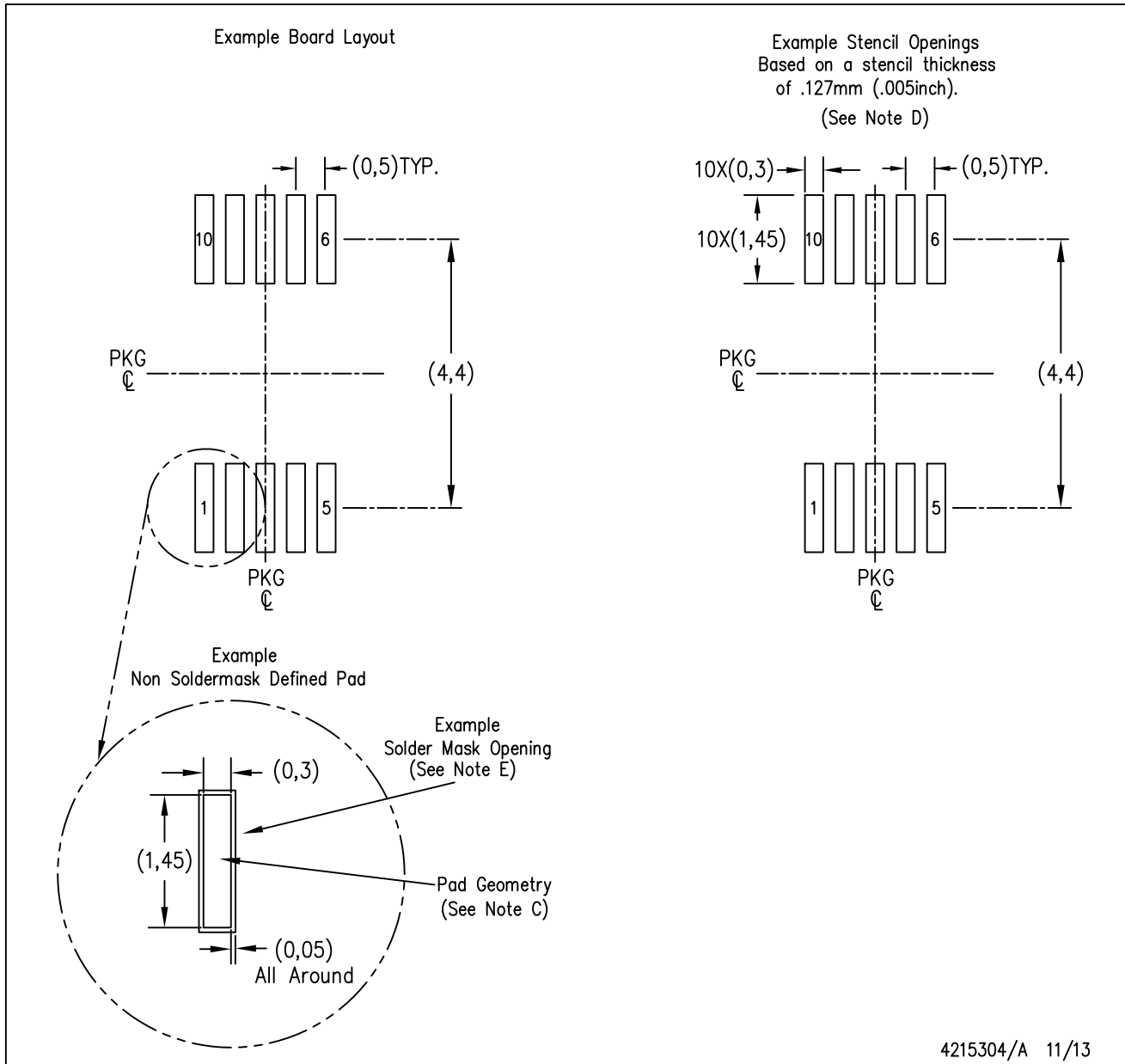
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



4073272/C 02/04



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com