# ROHM

| | |
|---|---|
| STRUCTURE | Silicon Monolithic Integrated Circuit |
| TYPE | Single Channel Series Regulator Driver IC |
| PRODUCT SERIES | **BD3504FVM** |
| FEATURES | •Non Rush Current on Start up (NRCS) |
| | •N channel MOSFET driver |

## O ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Supply Voltage | VCC | 7 *1 | V |
| Drain Voltage (VIN) | VD | 7 | V |
| Enable Input Voltage | Ven | 7 | V |
| Power Dissipation | Pd | 437.5 *2 | mW |
| Operating Temperature Range | Topr | −10~+100 | °C |
| Storage Temperature Range | Tstg | −55~+150 | °C |
| Maximum Junction Temperature | Tjmax | +150 | °C |

*1 Operating temperature range should not exceed $T_{jmax}$=150°C

*2 Pd derating at 3.5mW/°C for temperature above Ta=25°C

## O RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | 4.5 | 5.5 | V |
| Drain Voltage (VIN) | VD | 0.65 | 5.5 | V |
| Enable Input Voltage | Ven | −0.3 | 5.5 | V |
| Capacitor on NRCS Terminal | CNRCS | 0.001 | 1 | uF |
| Capacitor on SCP Terminal | VOUT | 0.65 | 2.5 | V |

★ This product is not designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the official specification.

This translated version is intended only as a reference, to aid in understanding the official version.

If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

O ELECTRICAL CHARACTERISTICS
(Unless otherwise specified,Ta=25°C  VCC=5V  VIN=3.3V  Ven=3V.  R1=R1'=∞ Ω, R2=R2'=0 Ω )

| PARAMETER | SYMBOL | LIMIT | | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Bias Current | ICC | – | 0.85 | 1.7 | mA | |
| Shut Down Mode Current | IST | – | 0 | 10 | uA | Ven=0V |
| Feed Back Voltage 1 | VFB1 | 0.643 | 0.650 | 0.657 | V | Io=50mA |
| Feed Back Voltage 2 | VFB2 | 0.630 | 0.650 | 0.670 | V | Vcc=4.5V to 5.5V , Ta=-10°C to 100°C(※) |
| Output Voltage | Vo | – | 1.20 | – | V | R1=R1'=3.9kΩ, R2=R2'=3.3KΩ |
| Line Regulation | Reg.l | – | 0.1 | 0.5 | %/V | VCC=4.5V to 5.5V |
| Load Regulation | Reg.L | – | 0.5 | 10 | mV | Io=0 to 3A |
| [Enable] | | | | | | |
| High Level Enable Input Voltage | Enhi | 2 | – | Vcc | V | |
| Low Level Enable Input Voltage | Enlow | -0.3 | – | 0.8 | V | |
| Enable pin Input Current | Ien | – | 7 | 10 | uA | Ven=3V |
| [Voltage Feed Back] | | | | | | |
| VFB Input Bias Current | IFB | – | 80 | – | nA | |
| [Source Voltage] | | | | | | |
| VS Input Bias Current | ISBIAS | – | 1.2 | 2.4 | mA | |
| VS Standby Current | ISSTB | 150 | – | – | mA | VS=1V Ven=0V |
| [Output MOSFET Driver] | | | | | | |
| MOSFET Driver Source Current | IGSO | 2 | 3 | 4 | mA | VFB=0.6V,VGATE=2.5V |
| MOSFET Driver Sink Current | IGSI | 2 | 3 | 4 | mA | VFB=0.7V,VGATE=2.5V |
| [UVLO] | | | | | | |
| VCC UVLO | VccUVLO | 4.20 | 4.35 | 4.50 | V | Vcc:Sweep up |
| VCC UVLO Hysterisis | Vcchys | 100 | 160 | 220 | mV | Vcc:Sweep down |
| VD UVLO | VDUVLO | Vo×0.6 | Vo×0.7 | Vo×0.8 | V | VD:Sweep up |
| [Drain Voltage Sensing] | | | | | | |
| VD Input bias Current | Ivd | – | 0 | – | nA | |
| [NRCS/SCP] | | | | | | |
| NRCS Charge Current | Inrcs | 14 | 20 | 26 | uA | VNRCS=0.5V |
| SCP Charge Current | Iscpch | 14 | 20 | 26 | uA | VNRCS=0.5V |
| SCP Discharge Current | IscpDi | 0.3 | – | – | mA | VNRCS=0.5V |
| SCP Threshold Voltage | Vscp | 1.2 | 1.3 | 1.4 | V | |
| Short Detect Voltage | Voscp | Vo×0.3 | Vo×0.35 | Vo×0.4 | V | |
| NRCS Stand-by Voltage | VSTB | – | – | 50 | mV | |

(※) Design Guarantee

Rev.B

○ PHYSICAL DIMENSIONS



(UNIT:mm)
**MSOP8**
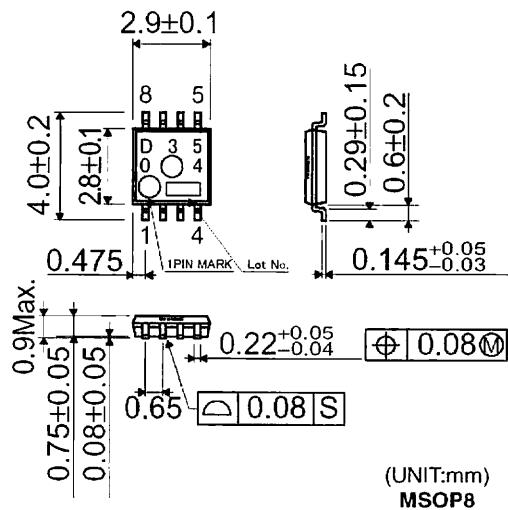
○ BLOCK DIAGRAM
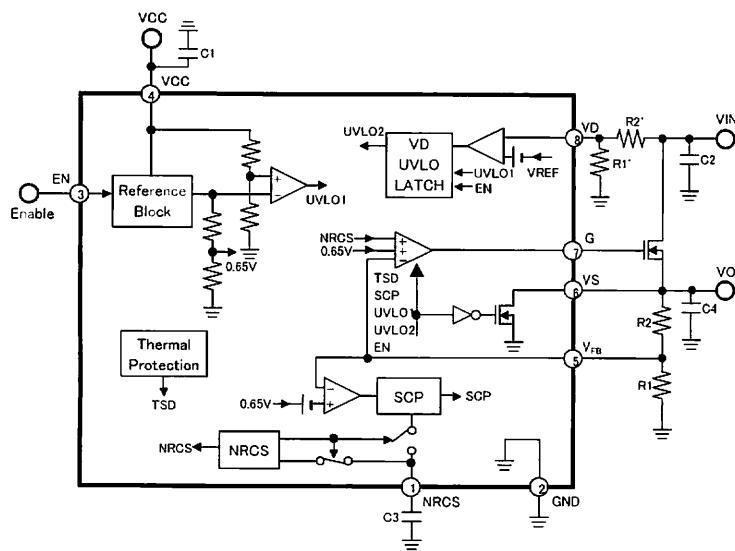


○ Pin number　Pin name

| PIN No. | Pin name |
|---------|----------|
| 1 | NRCS |
| 2 | GND |
| 3 | EN |
| 4 | VCC |
| 5 | VFB |
| 6 | VS |
| 7 | G |
| 8 | VD |

○NOTES FOR USE
(1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.
(2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.
(3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.
(4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.
(5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.
(6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions.  It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

| TSD ON temperature [°C]   (typ.) | Hysteresis temperature [°C]   (typ.) |
|---|---|
| 175 | 15 |

(7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.
(8) Output Voltage Setting (R1, R2)
Output volage is adjusted with resistor R1 and R2. output voltage is calculated as VFBx(R1+R2)/R1. Total 10kohm resistor (R1+R2) is recommended so that the output voltage is not affected by the VFB bias current (Typ. 80nA).
(9) Output Capacitor (C5)
Mount an output capacitor between VFB and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A 220uF polymer capacitor is recommended. However, the stability depends on the characteristics of temperature, load, the gate capacitance of the external MOSFET, and the mutual conductance (gm). And if a small ESR capacitor such as a ceramic capacitor is utilized (several kind of capacitors are utilized in parallel), the output voltage may oscillate due to lack of phase margin. In this case, measures can be taken by adding a capacitor and a resistor in series with this capacitor between the gate of MOSFET and GND. Please confirm operation across a variety of temperature, load conditions, and MOSFET characteristics.
(10) Input Capacitor (C1, C2)
The input capacitor reduces the output impedance of the voltage supply source connected in the VCC and VIN. If the output impedence of this power supply increases, the input voltage (VCC,VIN) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 10uF capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics, the substrate wiring pattern, and the parasitic capacitor between Gate and Drain of MOSFET. Please confirm operation across a variety of temperature, load, and MOSFET conditions.
(11) NRCS (Non Rush Current on Start-up) Setting(C3)
The NRCS function is built in this IC to prevent rush current from going through the load (VIN to Vo) for start-up. The constant current comes from the NRCS pin when EN is high or UVLO function is deactivated. Temporary reference voltage is made proportional to time due to current charge the NRCS pin capacitor and make output voltage start up proportional to this reference volatge.
Timer latch short circuit protection function is built in this IC (NRCS is also working at the same time.) to protect the breakdown of the power MOSFET caused by rush current when the output is shorted to GND. This function becomes active when the output voltage level goes under by 30% of specified Vout. The constant current comes from the NRCS pin in this case. When the reference voltage made by the current charge of the NRCS pin hits 1.3V (Typ.), the gate voltage becomes low. To obtain a stable SCP delay time, a capacitor (X5R or X7R) with susceptiblity to temperature is recommended.
(12) Input Terminal (VCC,VD,EN)
The EN, VD, and VCC are isolatetd. The UVLO protects incorrect operation when the voltage level of VD and VCC are low. The output becomes high when these pins reach the individual threshold level independent of the start-up pin order. However, if VIN shut down while the IC works under the normal operation, SCP function becomes active and latches the status. And the output does not come back active even though VIN goes up high again. In this case, start VCC or EN up again to deactivate this latch function.
(13) Maximum Output Current (Maximum Load)
The maximum output current of the power supply utilizing the IC depends on external MOSFET. The MOSFET should be chosen based on a required power supply characteristics for an actual application.
(14) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Example)
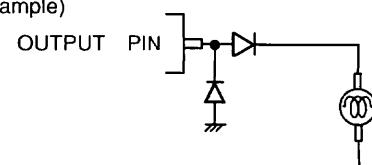
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Japan /
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Tokyo       2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082
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                  TEL : +81(75)311-2121      FAX : +81(75)314-6559

(Contact address for overseas customers in Japan)

Yokohama              TEL : +81(45)476-9270      FAX : +81(045)476-9271

As of 18th. April 2005